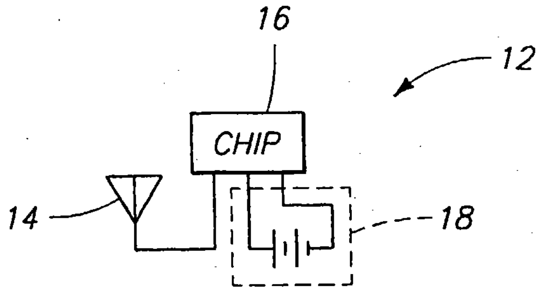


Fig. 1

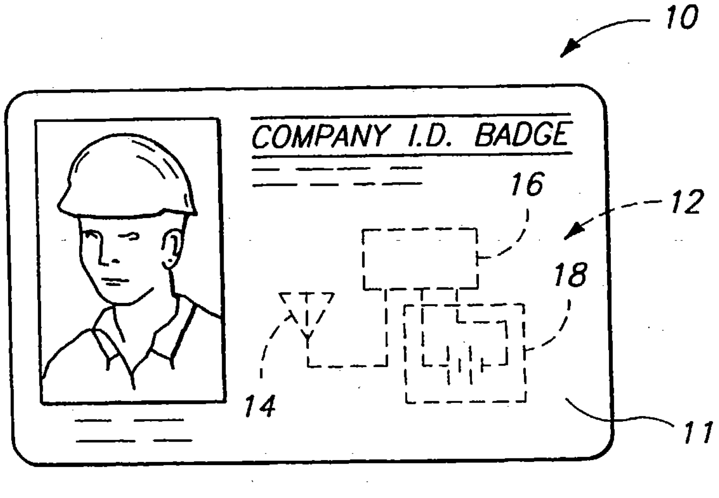


Fig. 2

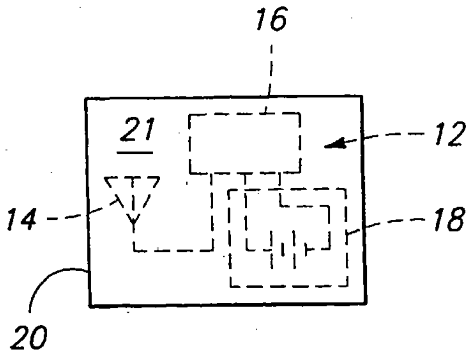

16
21
12
14
18
20

Fig 3

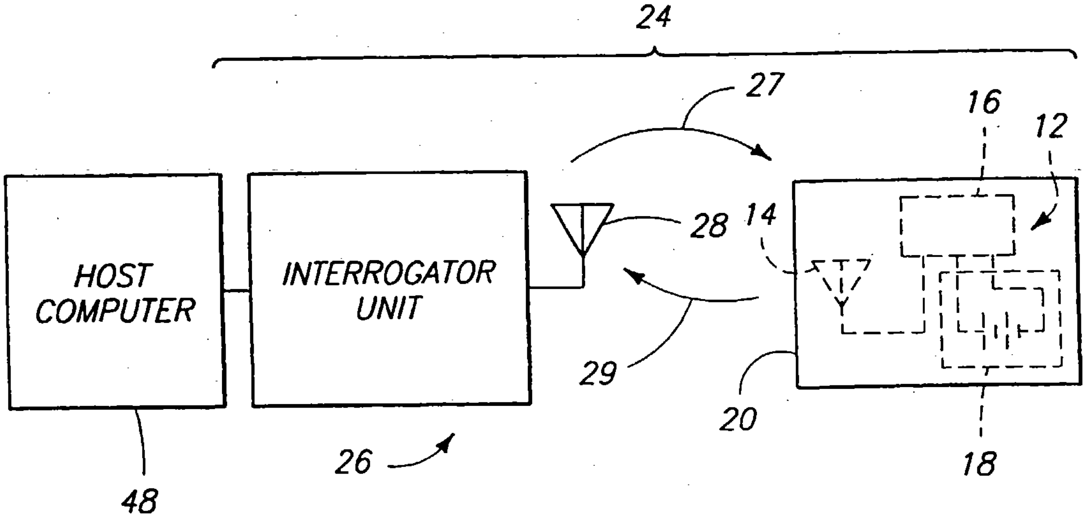

24
27
16
12
HOST COMPUTER
INTERROGATOR UNIT
28
14
29
20
18
26
48

Fig 4

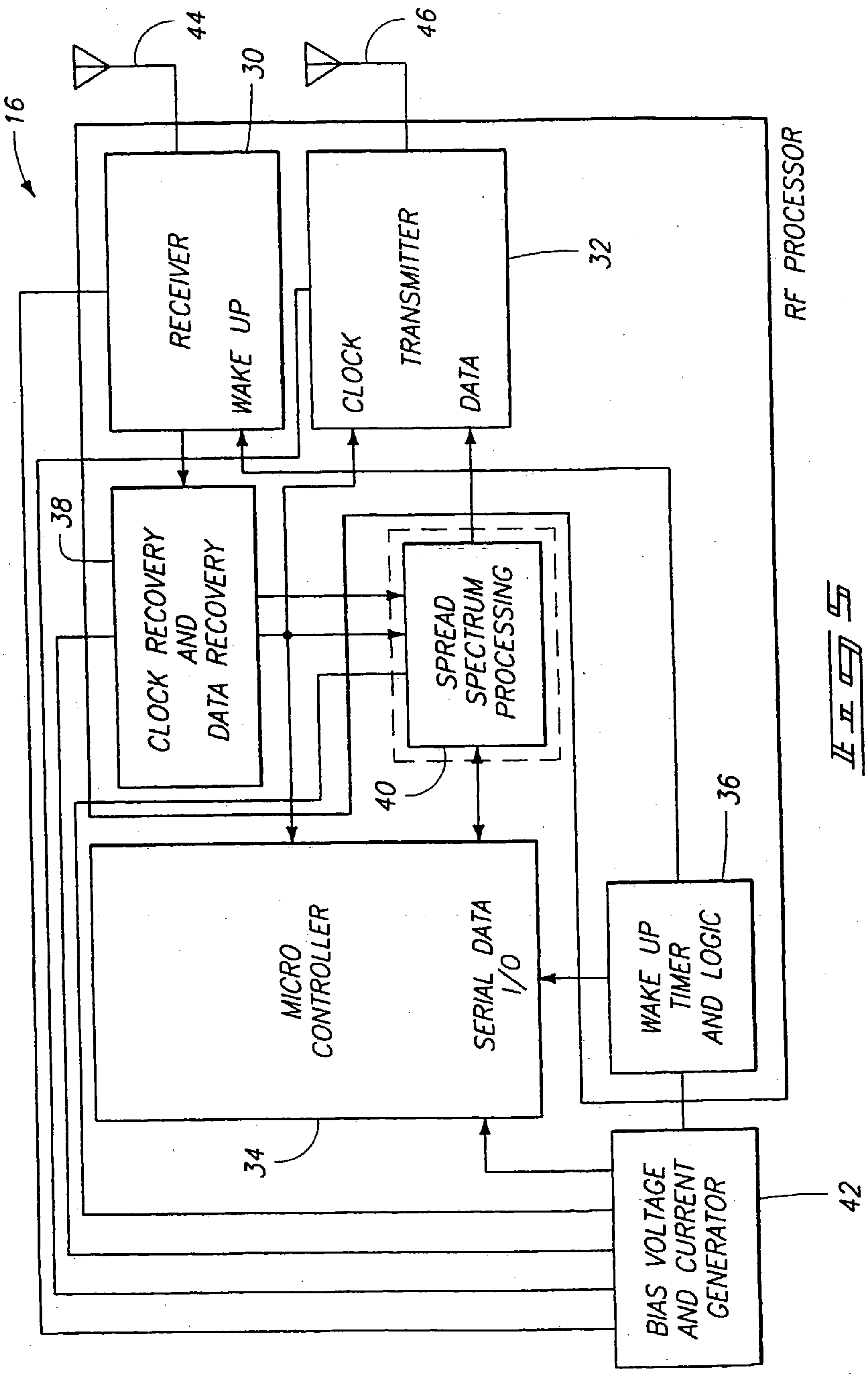

16
44
30
46
RECEIVER
WAKE UP
CLOCK
TRANSMITTER
DATA
32
RF PROCESSOR
38
CLOCK RECOVERY AND DATA RECOVERY
SPREAD SPECTRUM PROCESSING
40
MICRO CONTROLLER
SERIAL DATA I/O
34
WAKE UP TIMER AND LOGIC
36
BIAS VOLTAGE AND CURRENT GENERATOR
42

Fig. 5

6AA	6AB	6AC	6AD	6AE	6AF	6AG	6AH	6AI	6AJ	6AK
6BA	6BB	6BC	6BD	6BE	6BF	6BG	6BH	6BI	6BJ	6BK
6CA	6CB	6CC	6CD	6CE	6CF	6CG	6CH	6CI	6CJ	6CK
6DA	6DB	6DC	6DD	6DE	6DF	6DG	6DH	6DI	6DJ	6DK
6EA	6EB	6EC	6ED	6EE	6EF	6EG	6EH	6EI	6EJ	6EK

Fig 6

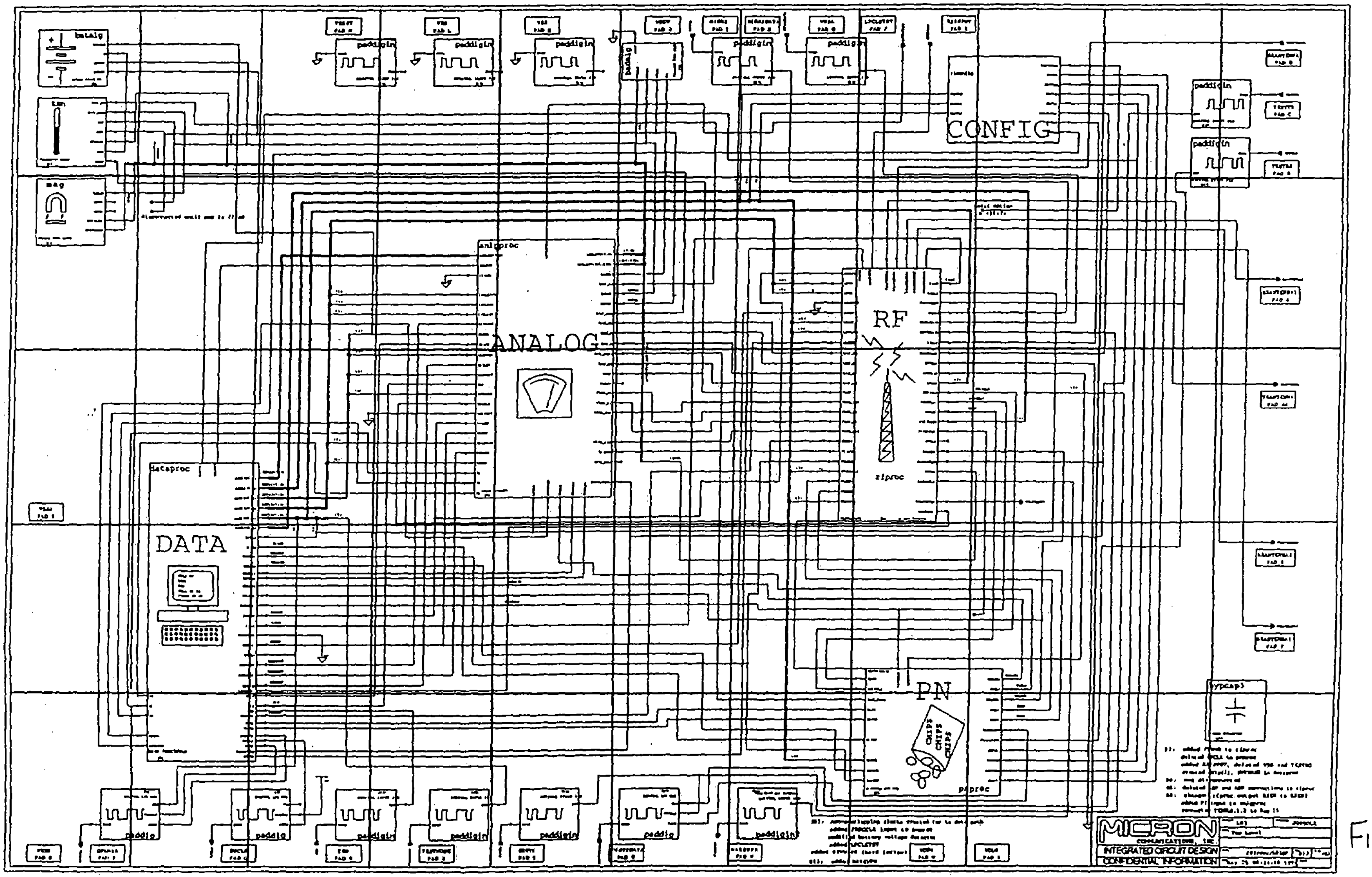

batalg
tsn
mag
paddigin
paddig
padalg
CONFIG
ANALOG
anlgproc
RF
rfproc
DATA
dataproc
PN
pnproc
CHIPS
CHIPS
CHIPS
bypcap3
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

FIG. 6AA-EK

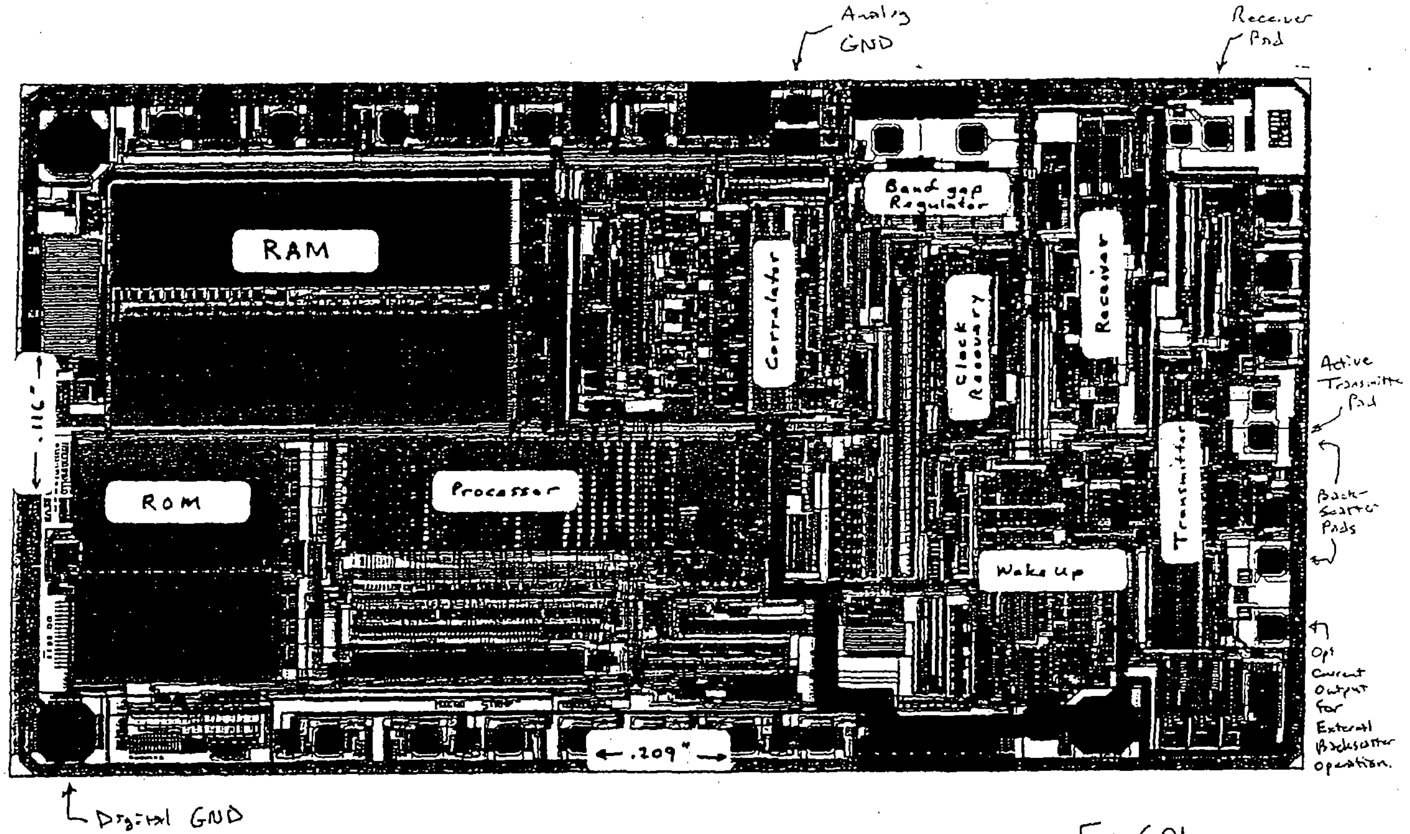
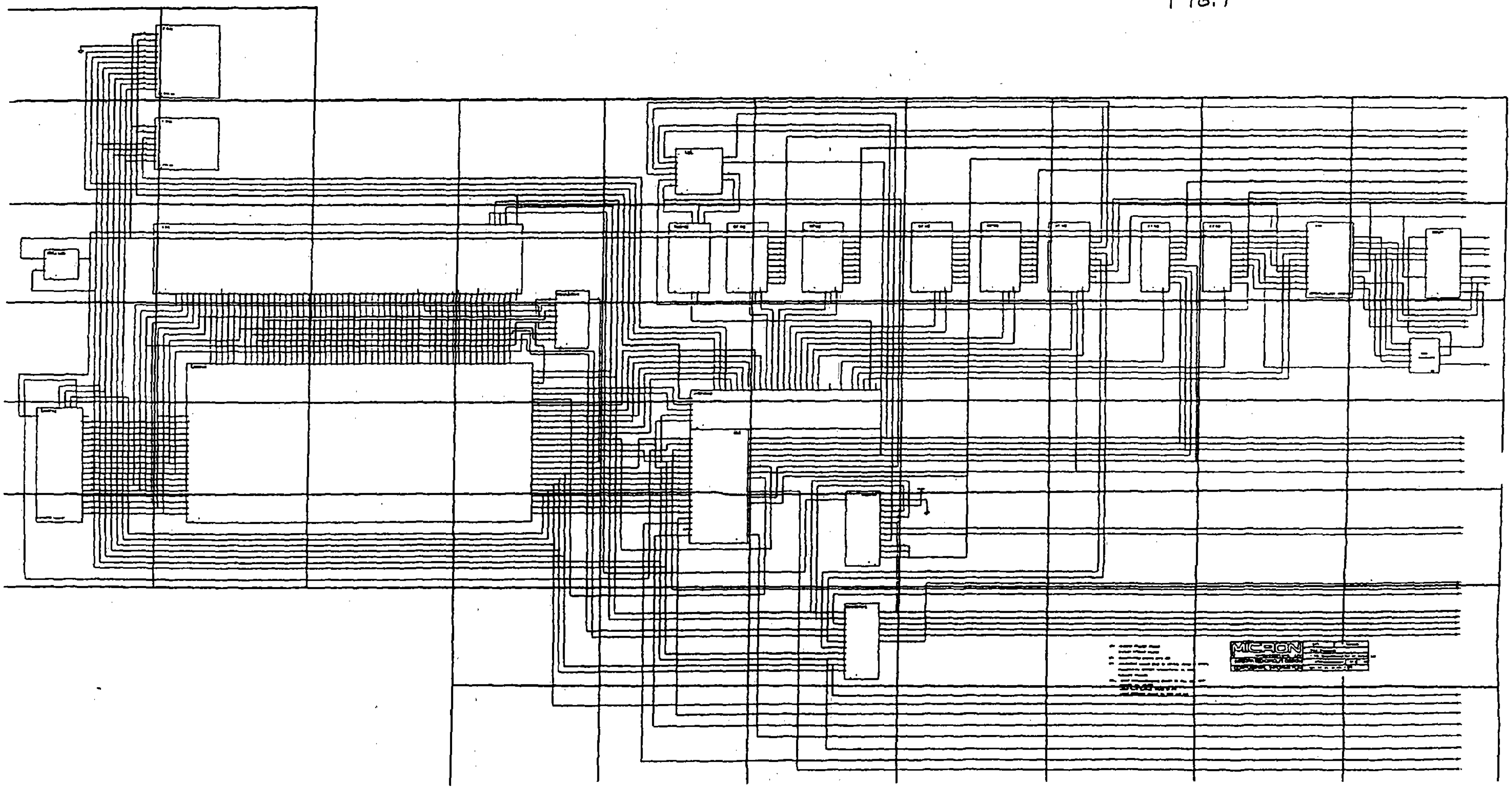

Analog GND
Receiver Pad
RAM
Band gap Regulator
Correlator
Clock Recovery
Receiver
Active Transmitter Pad
.116"
ROM
Processor
Transmitter
Back-Scatter Pads
Wake Up
Opt Current Output for External Backscatter operation.
.209"
Digital GND

FIG. 6.01

7AA	7AB								
7BA	7BB	7BC	7BD	7BE	7BF	7BG	7BH	7BI	7BJ
7CA	7CB	7CC	7CD	7CE	7CF	7CG	7CH	7CI	7CJ
7DA	7DB	7DC	7DD	7DE	7DF	7DG	7DH	7DI	7DJ
7EA	7EB	7EC	7ED	7EE	7EF	7EG	7EH	7EI	7EJ
7FA	7FB	7FC	7FD	7FE	7FF	7FG	7FH	7FI	7FJ
			7GD	7GE	7GF	7GG	7GH	7GI	7GJ
			7HD	7HE	7HF	7HG	7HH	7HI	7HJ

Fig 7

FIG. 7



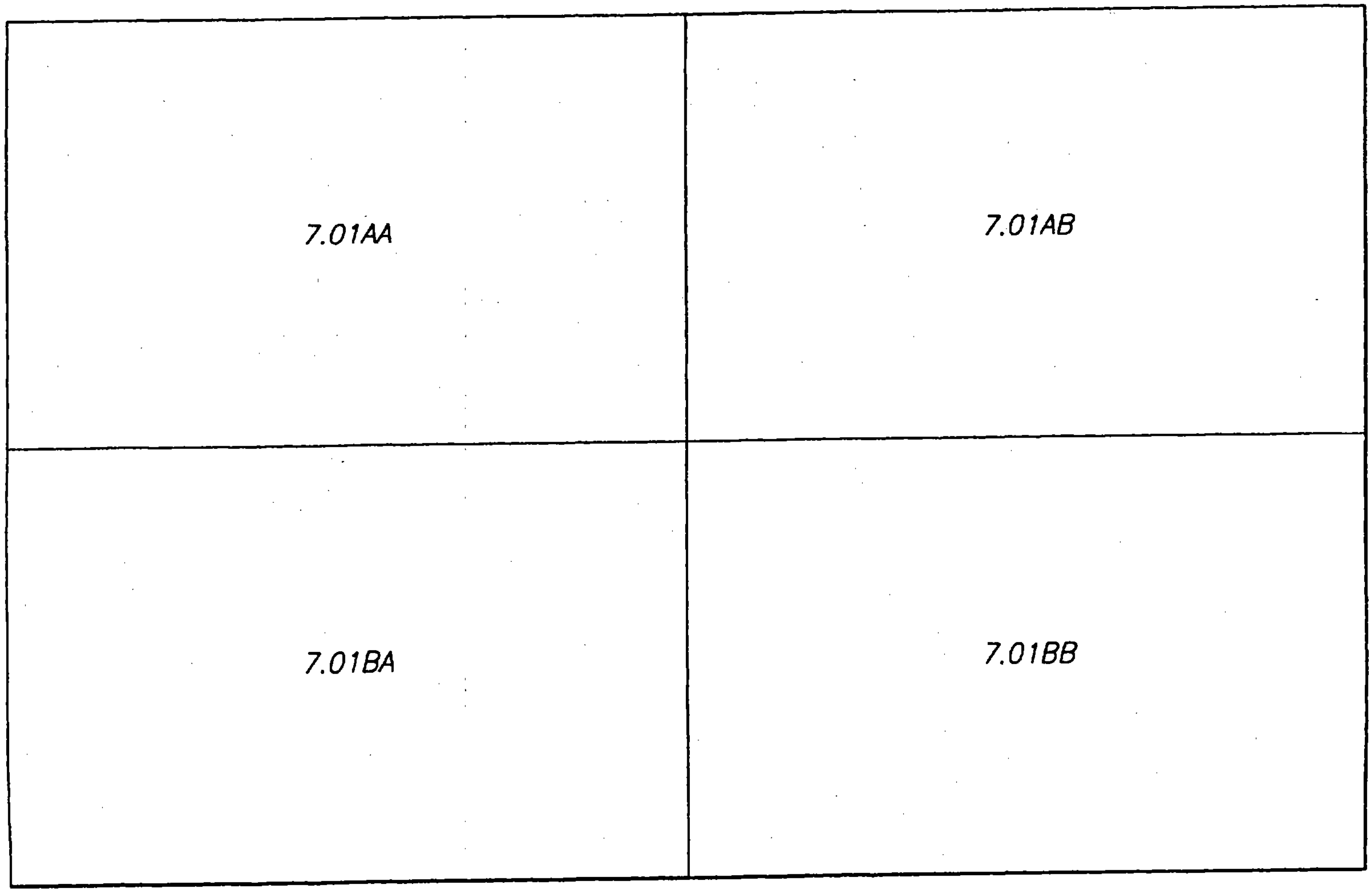


Fig 7.01

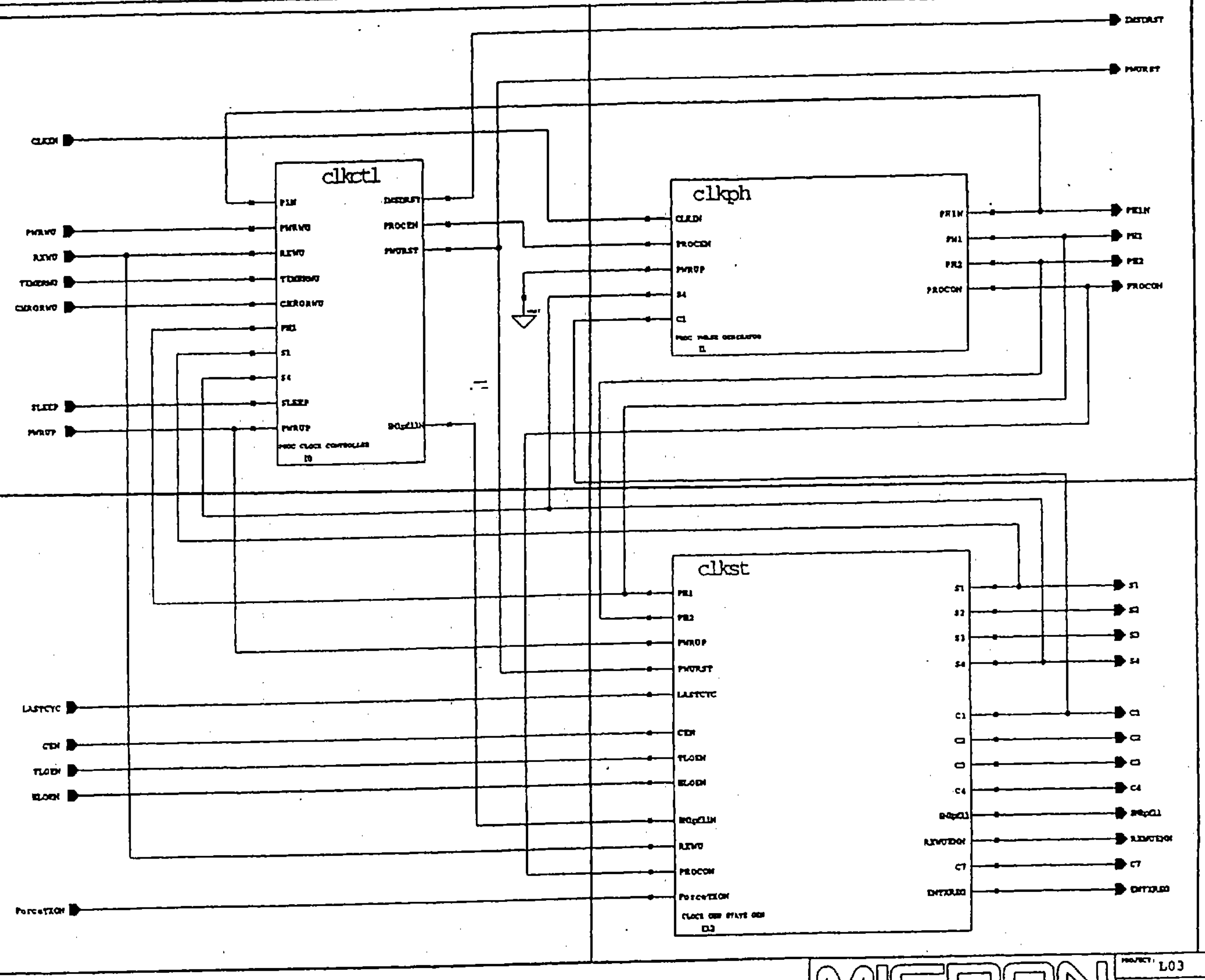


FIG. 7.01

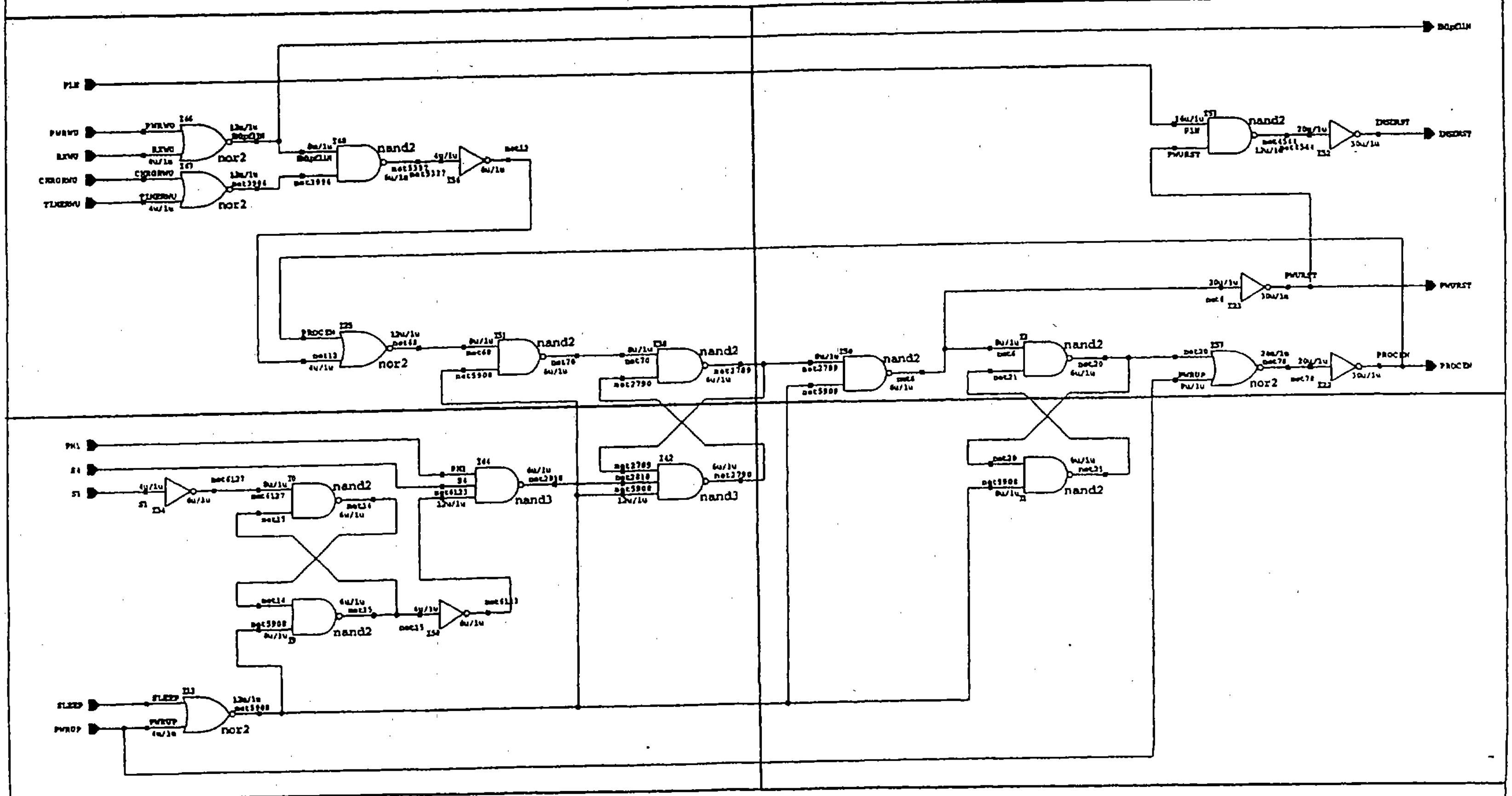
B2: created ENlpfll signal
added ENTXREG logic
B11: added hard lockout to clkst

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03	Roczoll
Processor Clock Generator	
2-Phase/4-State/8-Cycle	
103reva/clk	B11 ml
Apr 13 09:58:52 1996	

7.0101AA	7.0101AB
7.0101BA	7.0101BB

FIG. 7.0101



B2: created ENIpflIN signal

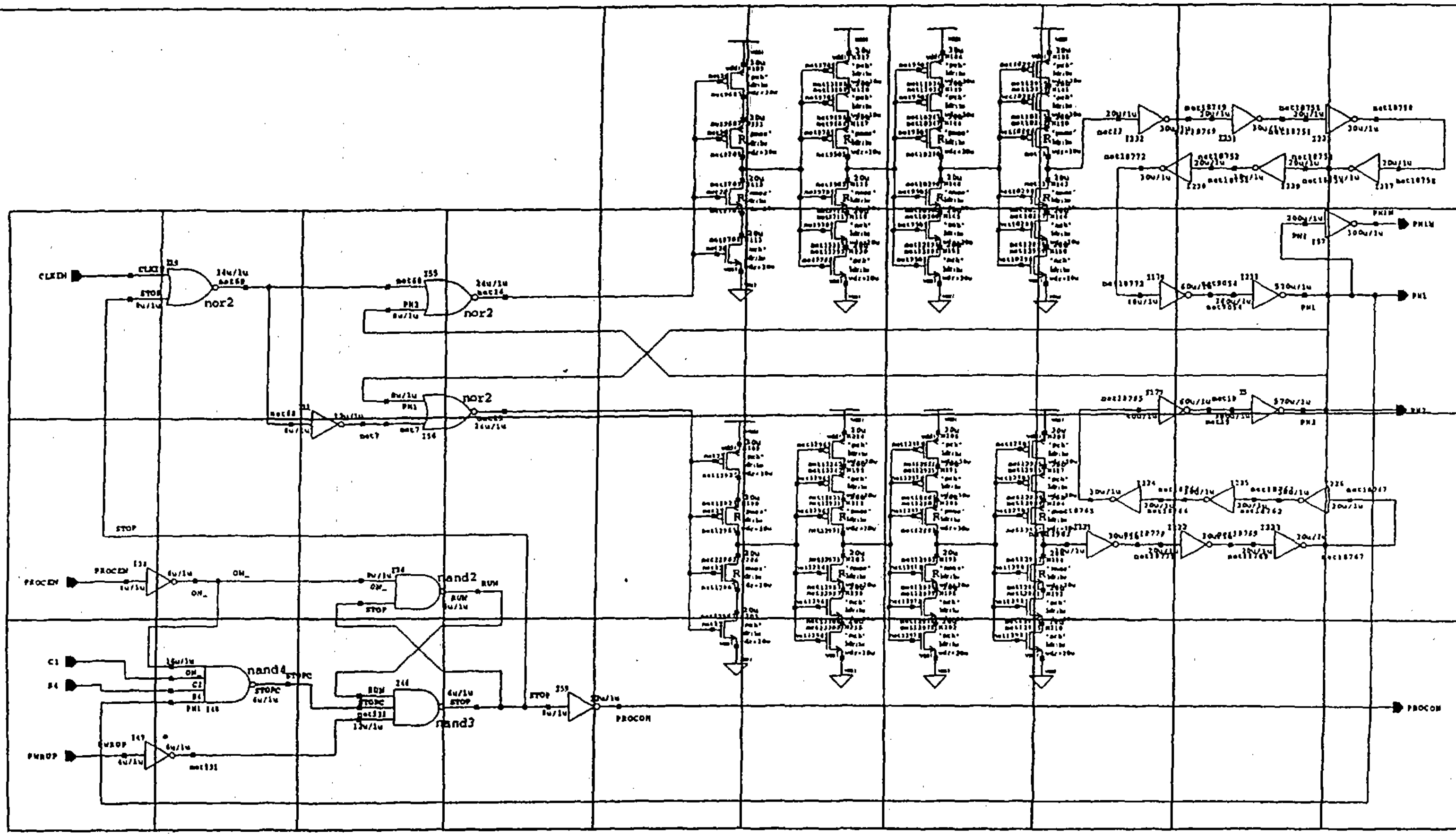
Fig. 7.0101

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT L03			DESIGNER Rotzoll		
TITLE Processor Clock Controller					
NAME l03reva/clkctl		REV B2		CELL nil	
DATE Jul 26 11:15:27 1995			SHEET		

				7.0102AE	7.0102AF	7.0102AG	7.0102AH	7.0102AI	7.0102AJ
7.0102BA	7.0102BB	7.0102BC	7.0102BD	7.0102BE	7.0102BF	7.0102BG	7.0102BH	7.0102BI	7.0102BJ
7.0102CA	7.0102CB	7.0102CC	7.0102CD	7.0102CE	7.0102CF	7.0102CG	7.0102CH	7.0102CI	7.0102CJ
7.0102DA	7.0102DB	7.0102DC	7.0102DD	7.0102DE	7.0102DF	7.0102DG	7.0102DH	7.0102DI	7.0102DJ

Fig 7.0102



F1G. 7.0102

B2: Pin name changes

B8: Added 6 inverters to non-overlap time
Make the number of inverters adjustable on metal

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
Rotzoll
Processor Phase Generator
2-Phase Non-overlapping
103reva/clkph
B8
nil
Dec 5 17:55:56 1995

7.0103AA	7.0103AB	7.0103AC	7.0103AD
7.0103BA	7.0103BB	7.0103BC	7.0103BD

FIG 7.0103

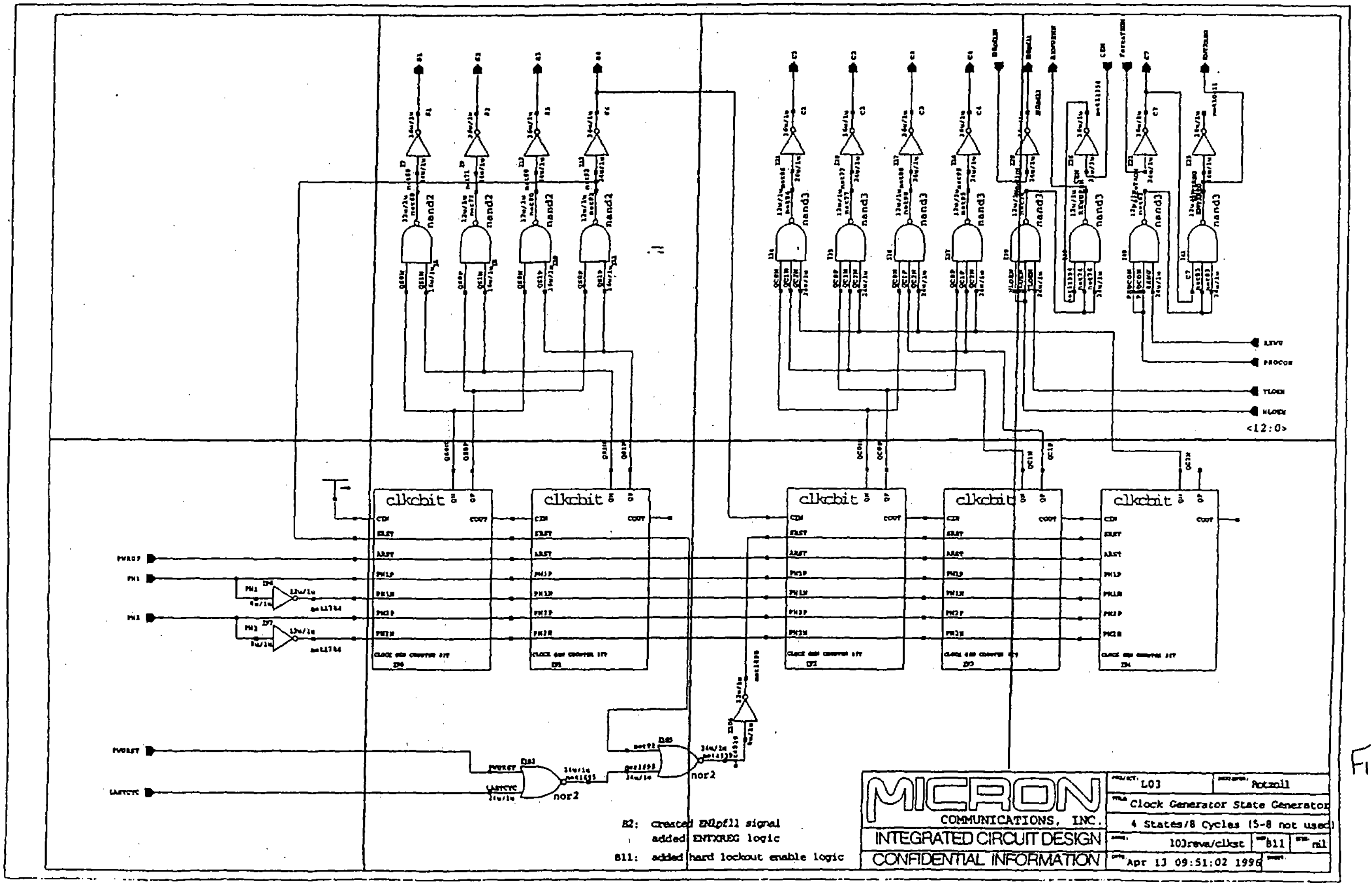

clkcbit
clkcbit
clkcbit
clkcbit
clkcbit
nand2
nand2
nand2
nand2
nand3
nand3
nand3
nand3
nand3
nand3
nand3
nand3
nor2
nor2
<12:0>
B2: created ENlpf11 signal
added ENTXREG logic
B11: added hard lockout enable logic
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
Rotzoll
Clock Generator State Generator
4 States/8 Cycles (5-8 not used)
103reva/clkst
B11
ml
Apr 13 09:51:02 1996

FIG. 7.0103

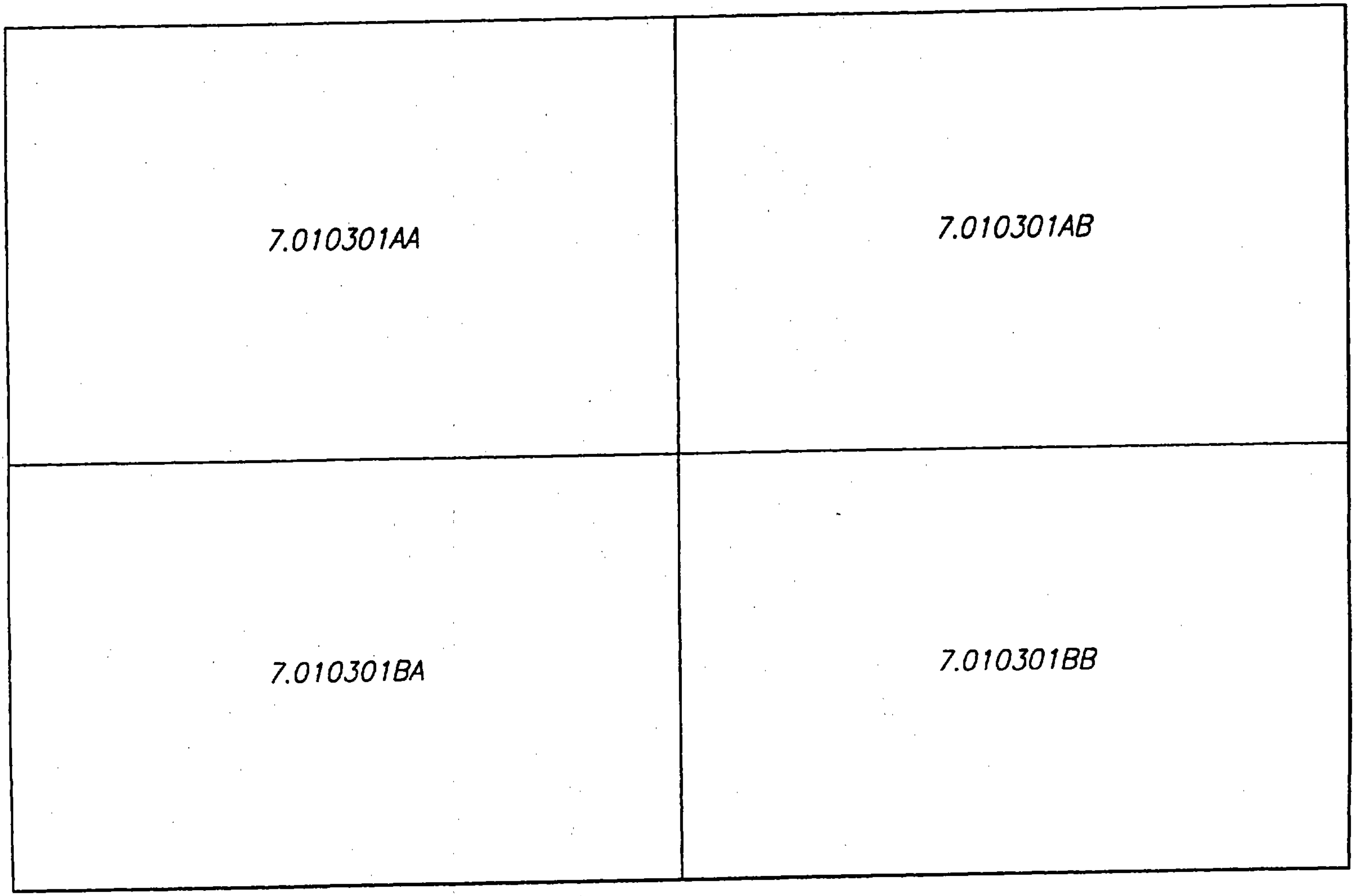


FIG. 7.010301

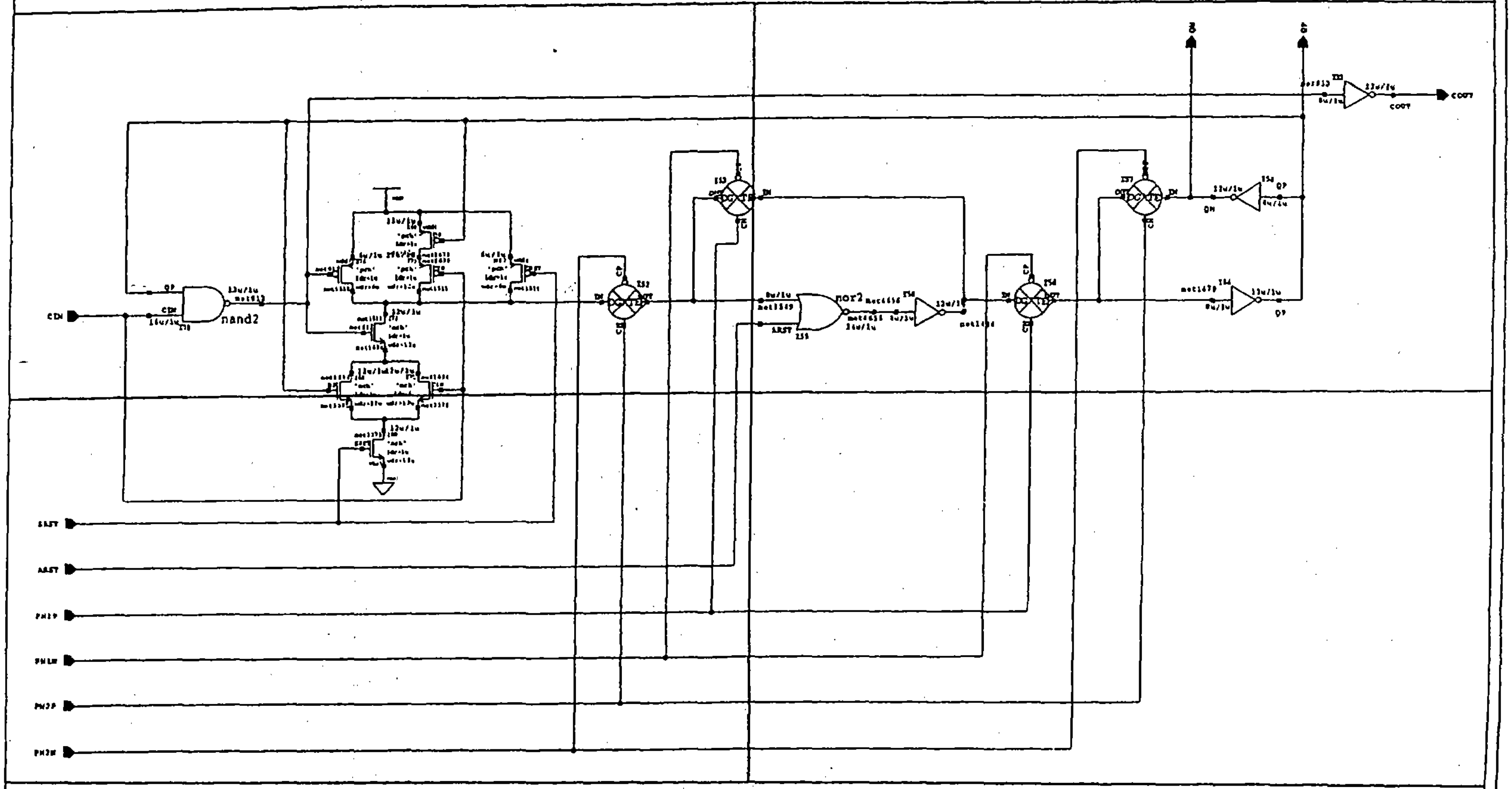


FIG. 7.010301

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
Rotzoll
Clock Generator Counter Bit
Sync/Async Resets
103reva/clkcbit
-
nil
Sep 29 16:14:06 1993

7.02AA	7.02AB	7.02AC	7.02AD	7.02AE	7.02AF
7.02BA	7.02BB	7.02BC	7.02BD	7.02BE	7.02BF

Fig 7.02

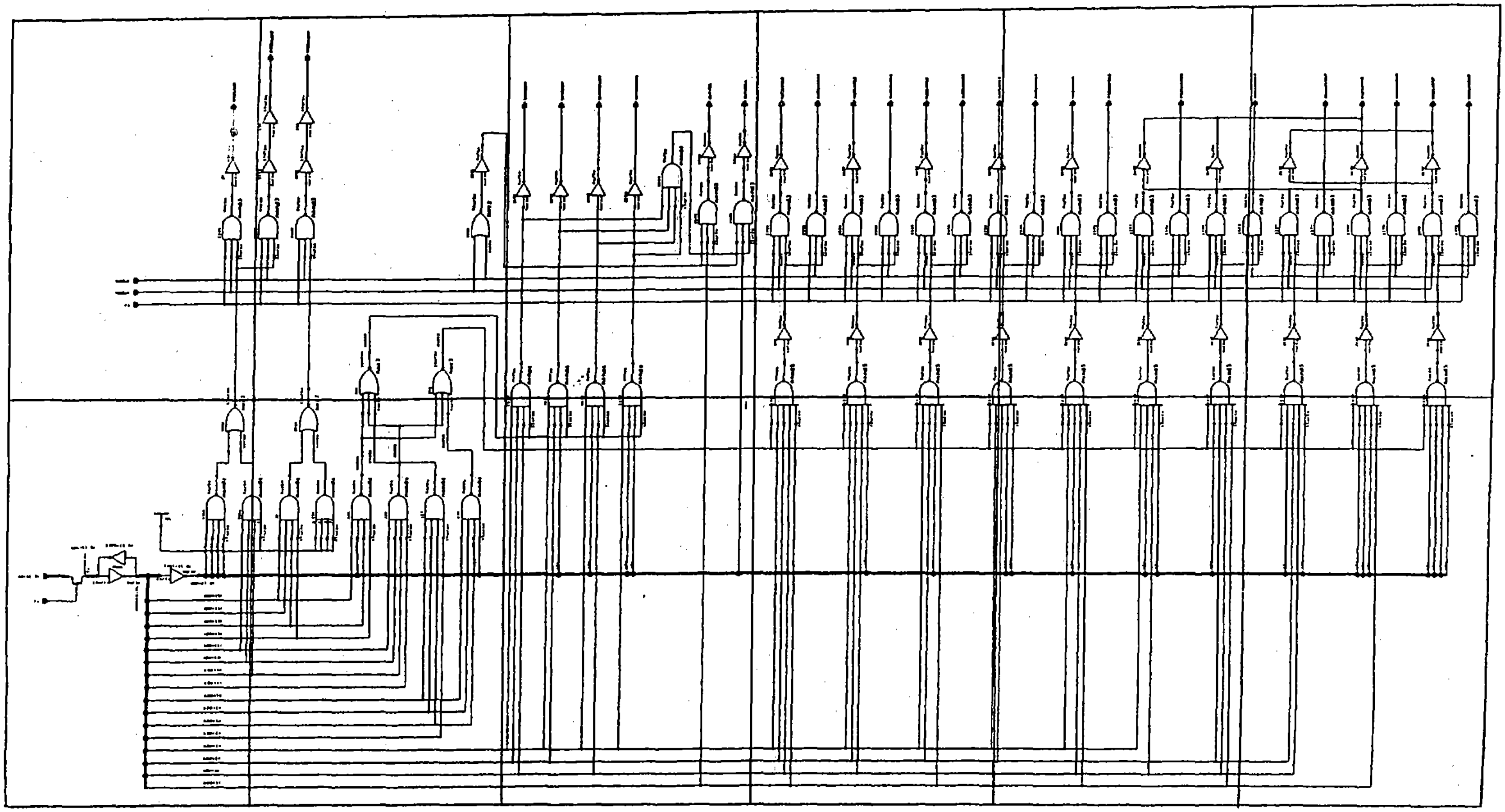


Fig. 7.02

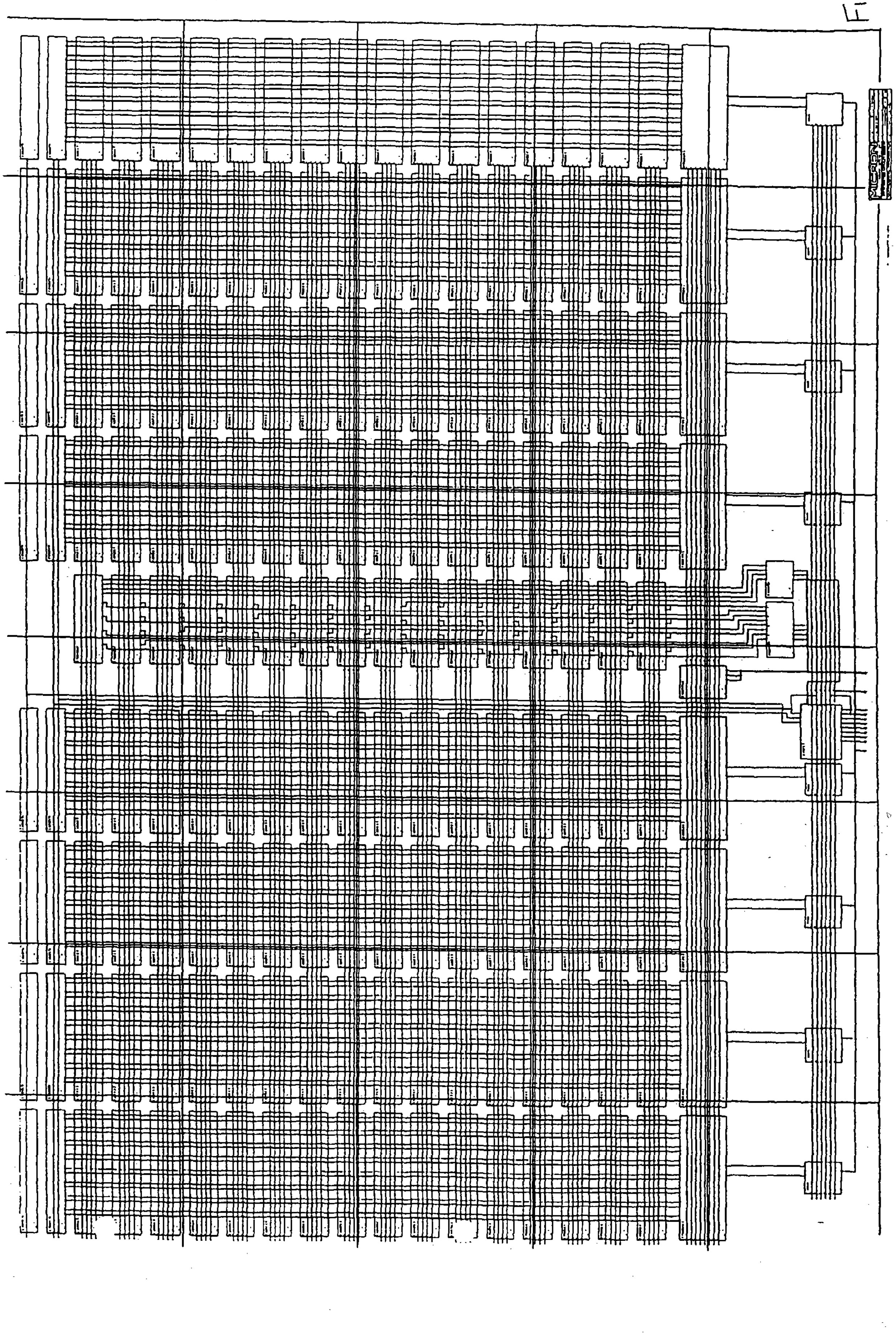
MICRON COMMUNICATIONS, INC
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

Address Decoder

7.03AA	7.03AB	7.03AC	7.03AD	7.03AE	7.03AF	7.03AG	7.03AH
7.03BA	7.03BB	7.03BC	7.03BD	7.03BE	7.03BF	7.03BG	7.03BH
7.03CA	7.03CB	7.03CC	7.03CD	7.03CE	7.03CF	7.03CG	7.03CH
7.03DA	7.03DB	7.03DC	7.03DD	7.03DE	7.03DF	7.03DG	7.03DH
7.03EA	7.03EB	7.03EC	7.03ED	7.03EE	7.03EF	7.03EG	7.03EH

FIG. 7.03

Fig 7.03



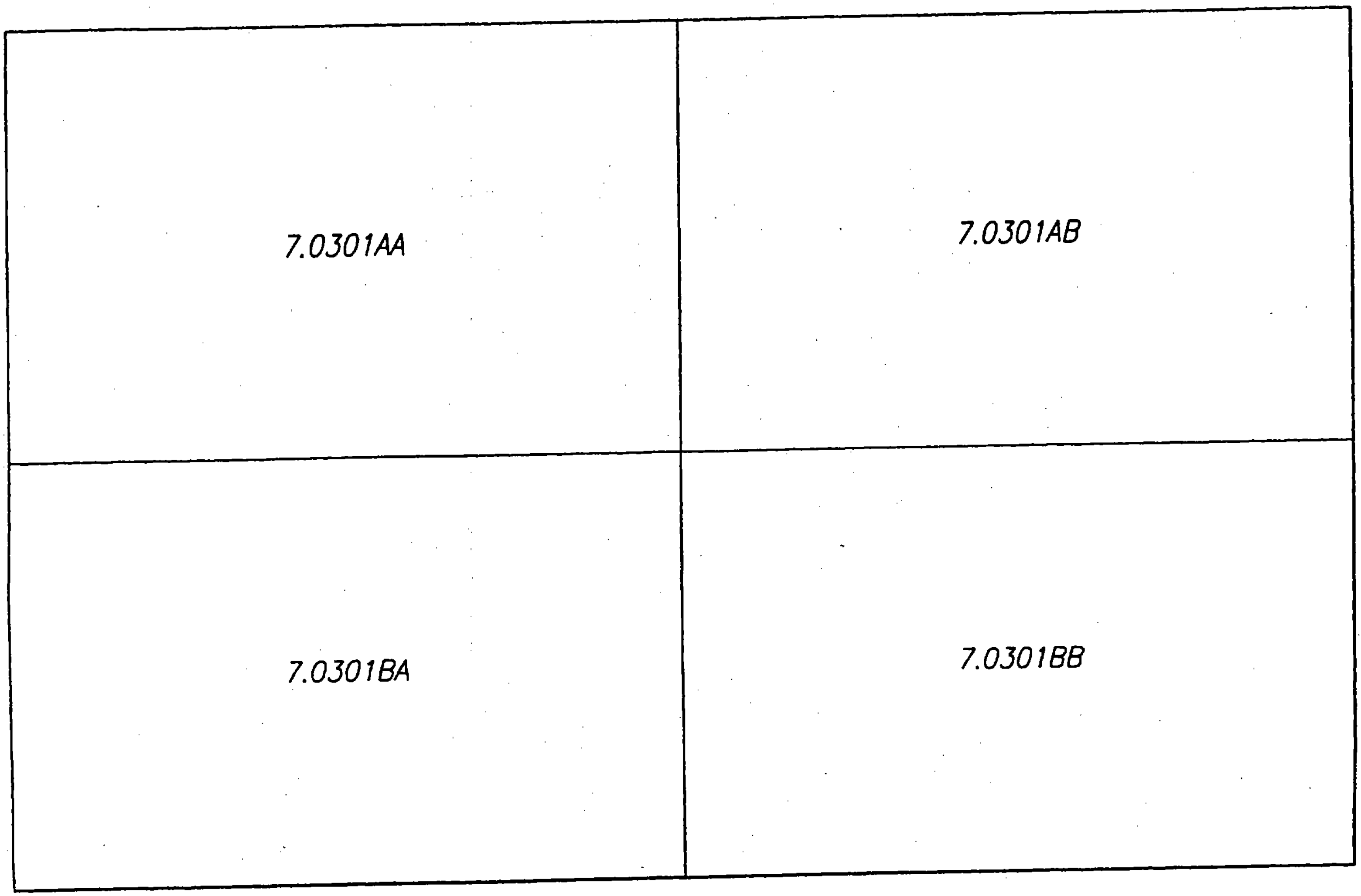


FIG. 7.0301

ramctl Nr 1

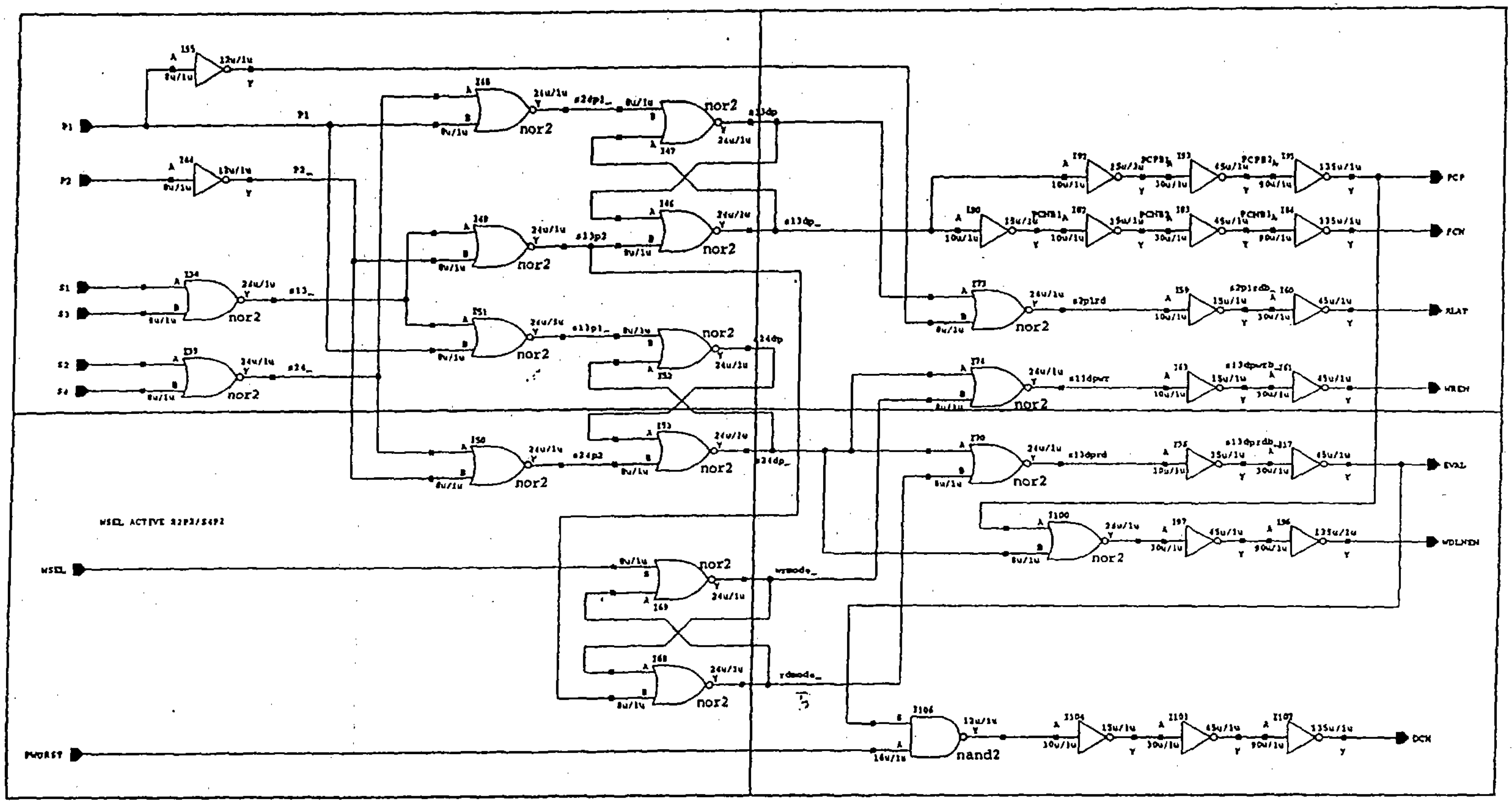


Fig. 7.0301

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03 A∅3
DESIGNER: Rotzoll
TITLE: RAM Control
NAME: 103reva/ramctl
REV: -
ICON: nil
DATE: Feb 11 16:47:36 1994
SHEET:

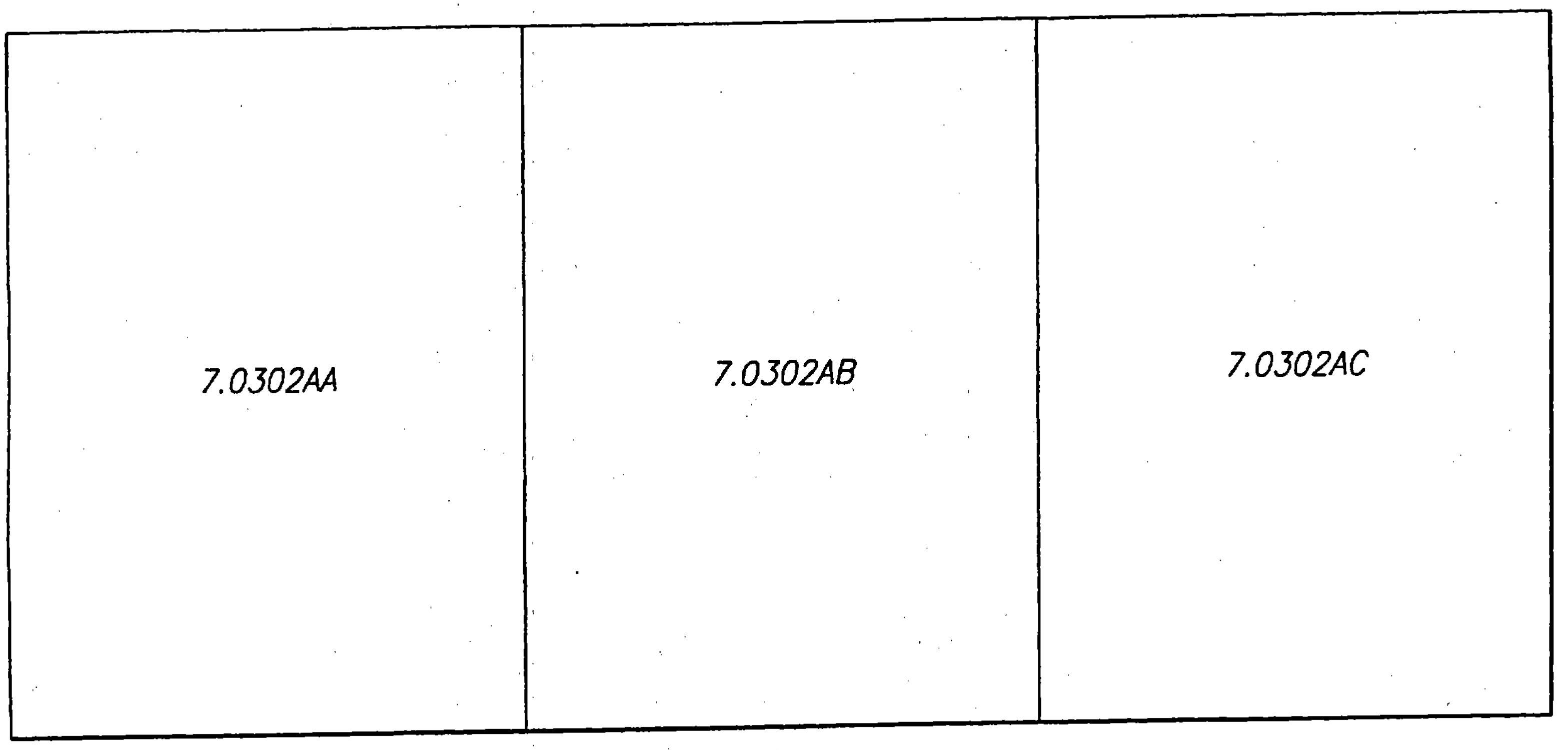


FIG 7.0302

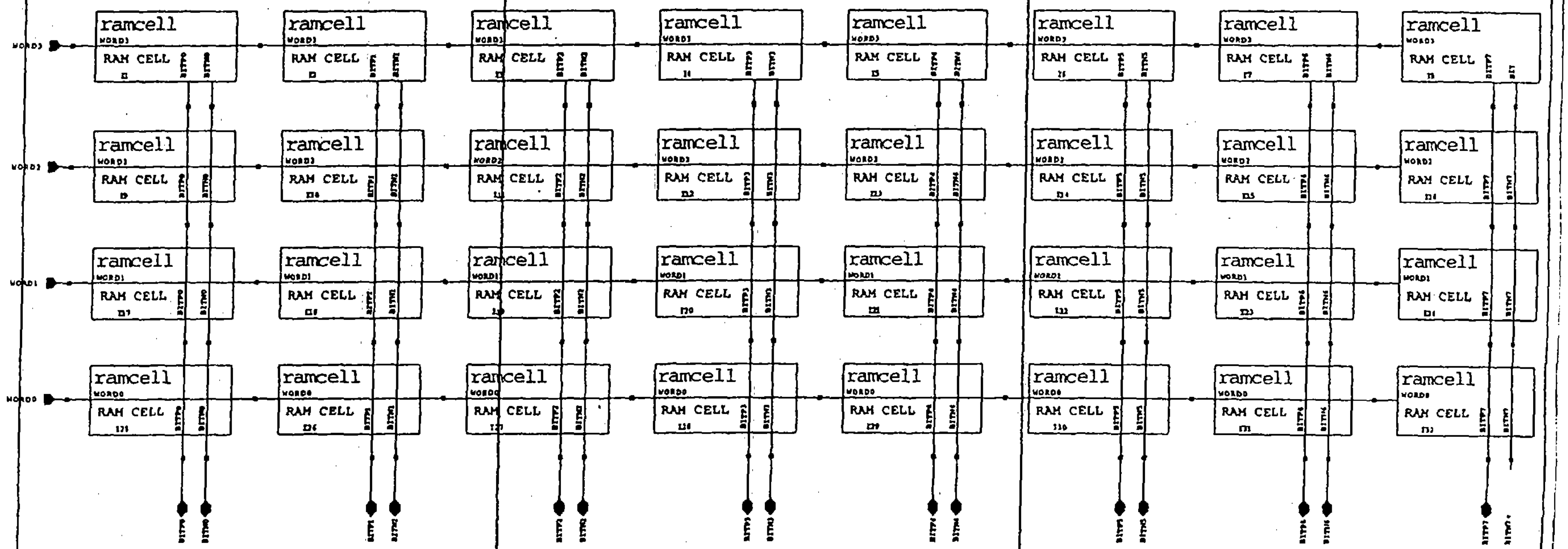


Fig. 7.0302

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
Rotzoll
8x4 RAM Array
103reva/ram8x4
-
mil
Nov 6 11:34:37 1993

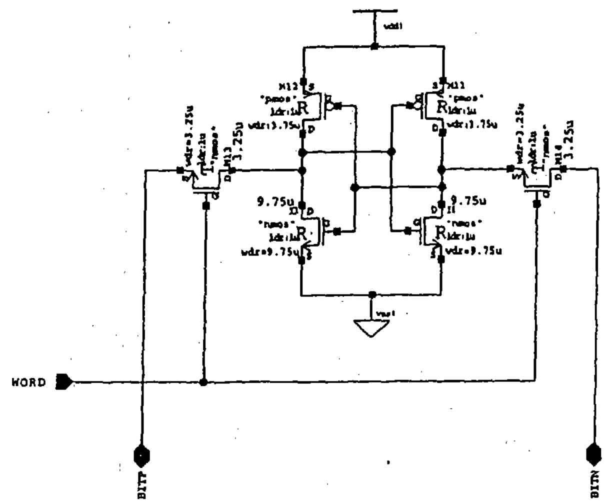


Fig. 7.030201

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: 6T RAM Cell
NAME: 103reva/ramcell
REV: -
SIZE: A
DATE: Nov 6 11:34:48 1993
SHEET:

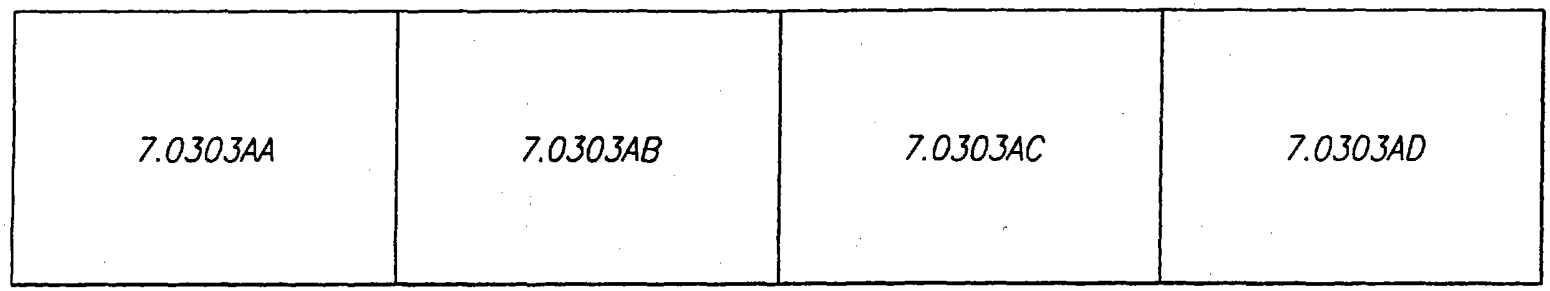


FIG. 7.0303

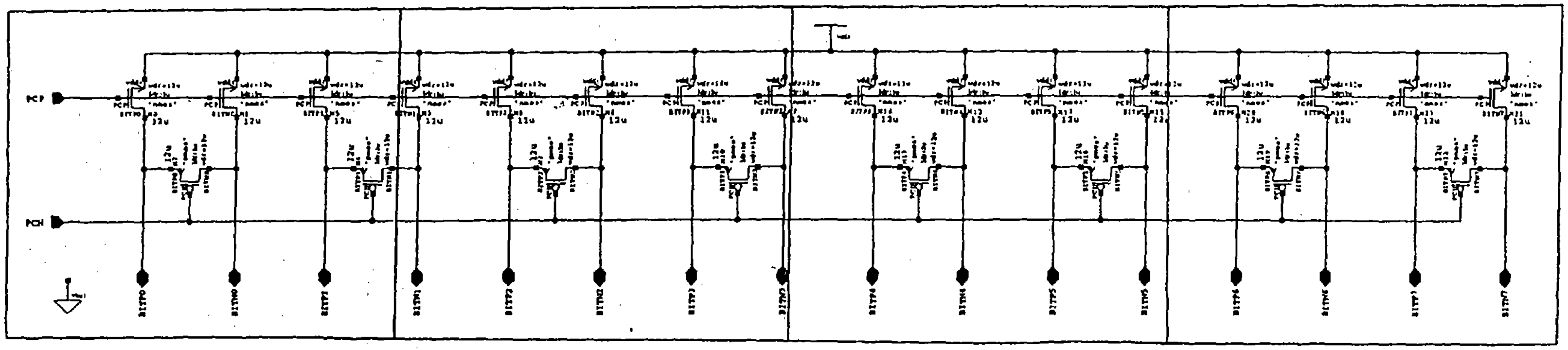


FIG. 7.0303

MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03	Rotzoll				
RAM Precharge					
103reva/rampch		-		m1	
Nov 12 02:58:36 1993					

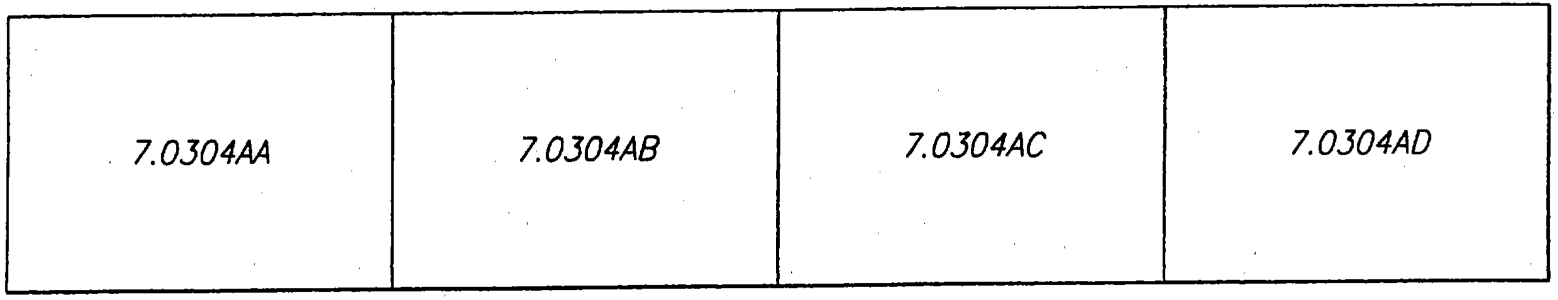


FIG. 7.0304

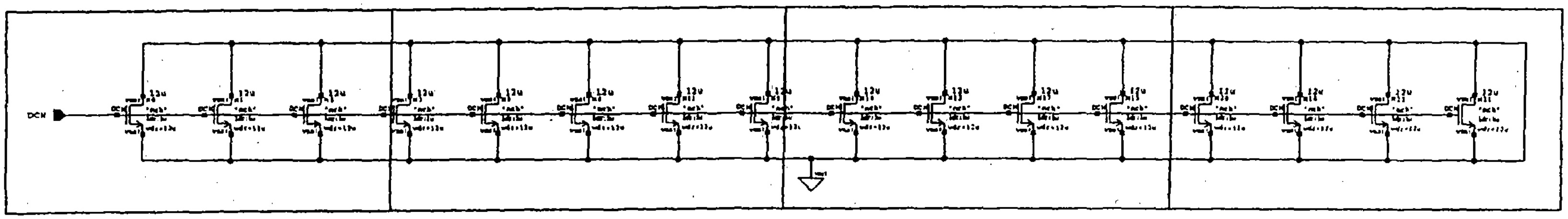
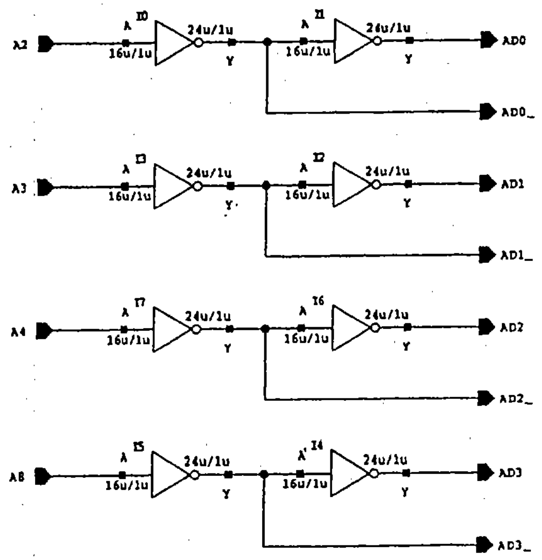


FIG. 7.0304

B8: disconnected dch devices from bit lines and tied to vss

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: RAM Precharge			
NAME: 103reva/ramdch		REV: B8	FILE: nl
DATE: Jan 28 09:51:27 1996		SHEET:	



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: RAM Address Buffer
NAME: 103reva/ramadb
REV: -
SIZE: A
DATE: Sep 29 16:04:01 1993
SHEET:

Fig. 7.0305

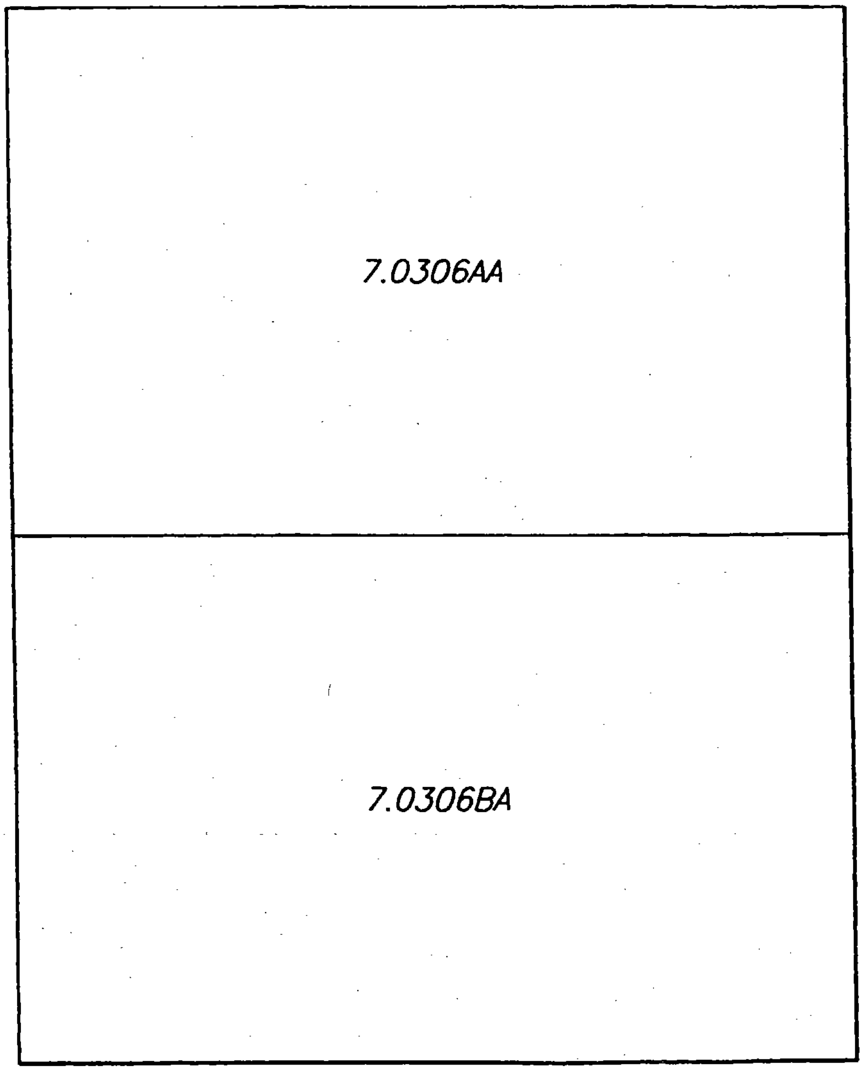


Fig 7.0306

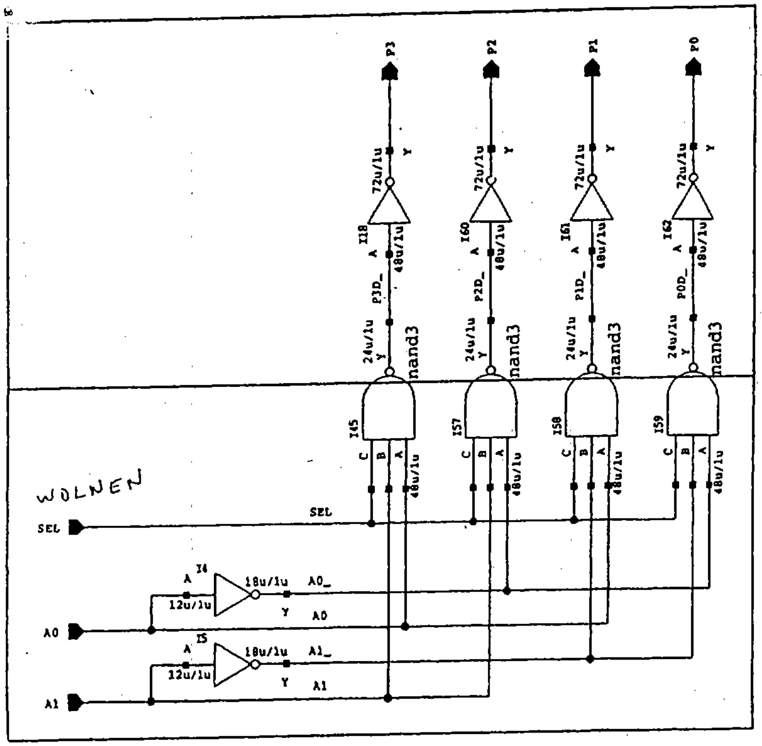


FIG. 7.0306

MICRON COMMUNICATIONS, INC.	PROJECT: L03	DESIGNER: Rotzoll	
INTEGRATED CIRCUIT DESIGN	TITLE: RAM Word Line Driver		
	NAME: 103reva/ramwdr	REV: -	SIZE: A
CONFIDENTIAL INFORMATION	DATE: Sep 29 16:04:16 1993	SHEET:	

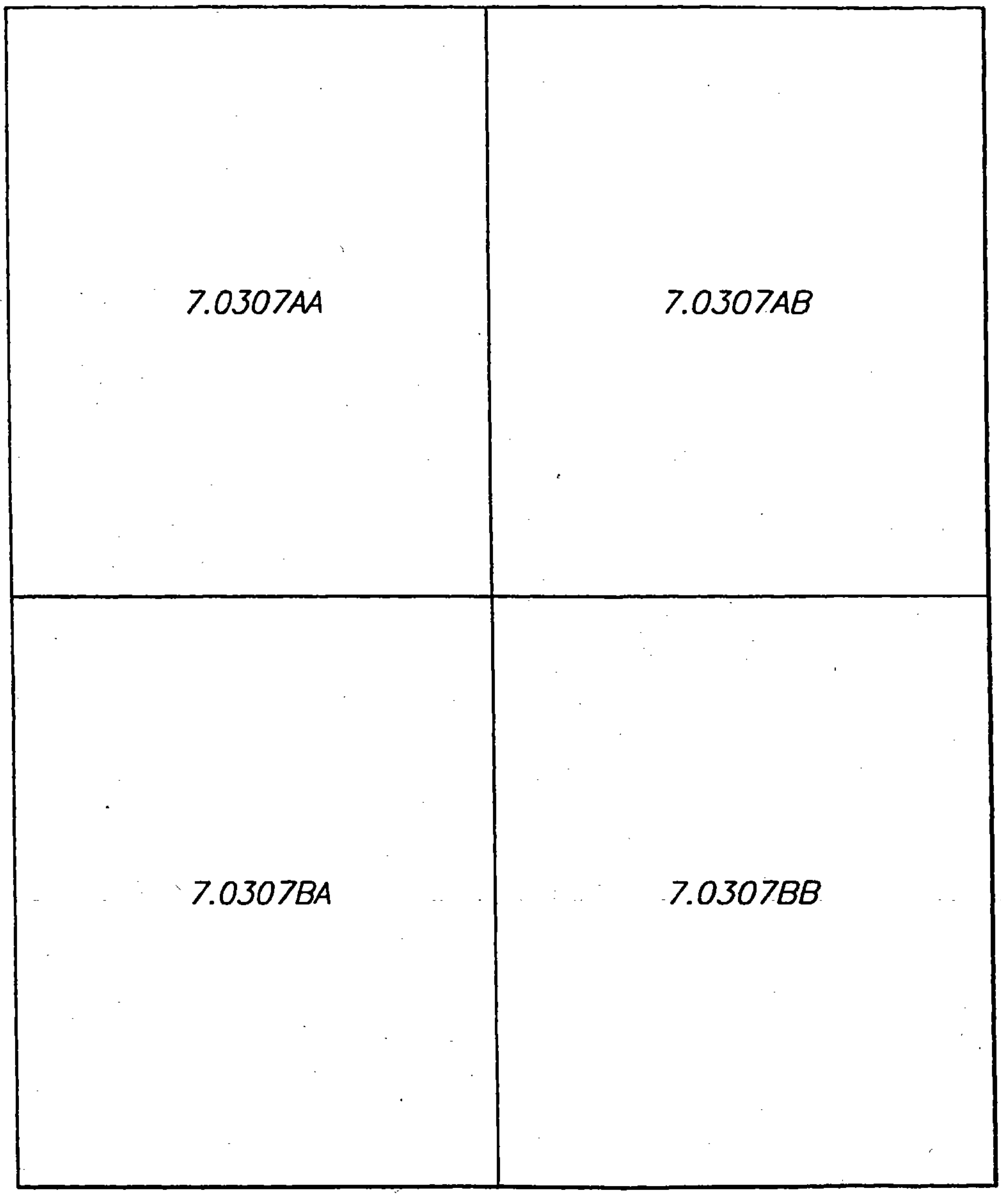
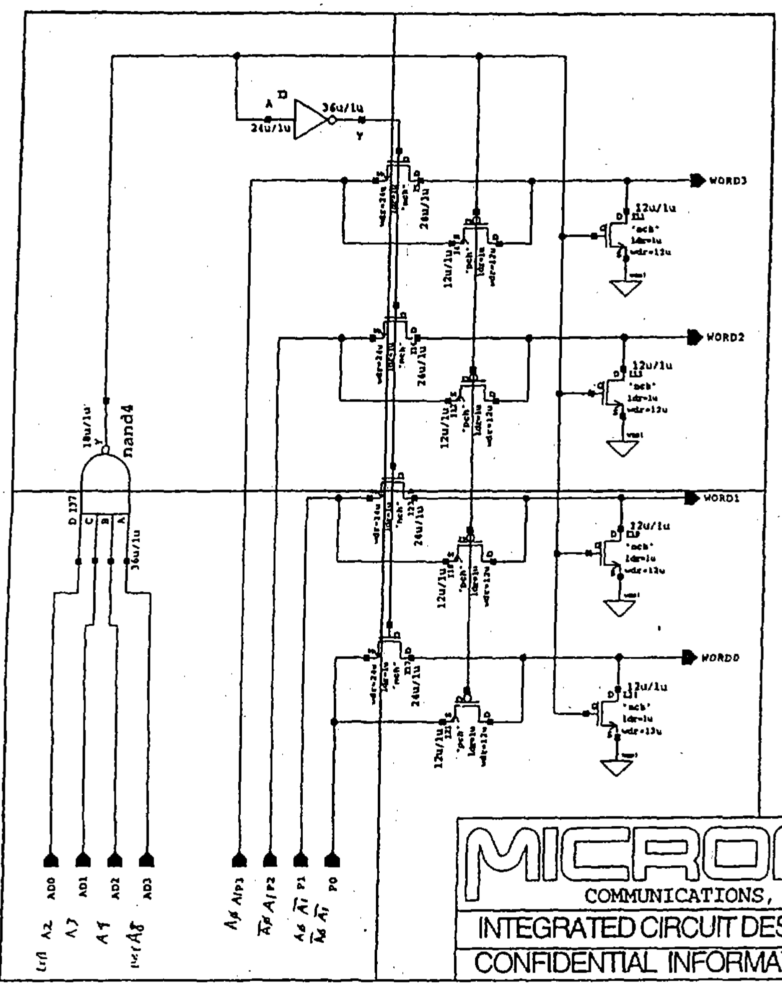


Fig 7.0307



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: RAM Word Line Decoder
NAME: 103reva/ramwdec
REV: -
SIZE: A
DATE: Sep 29 15:41:08 1993
SHEET:

FIG. 7.0307

7.0308AA	7.0308AB
7.0308BA	7.0308BB

Fig 7.0308

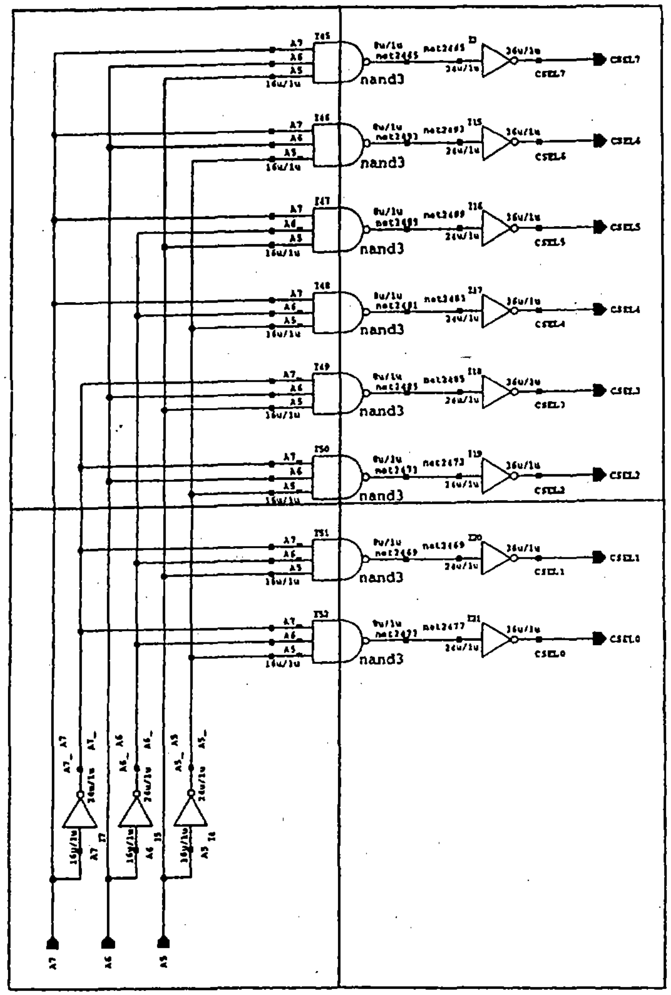


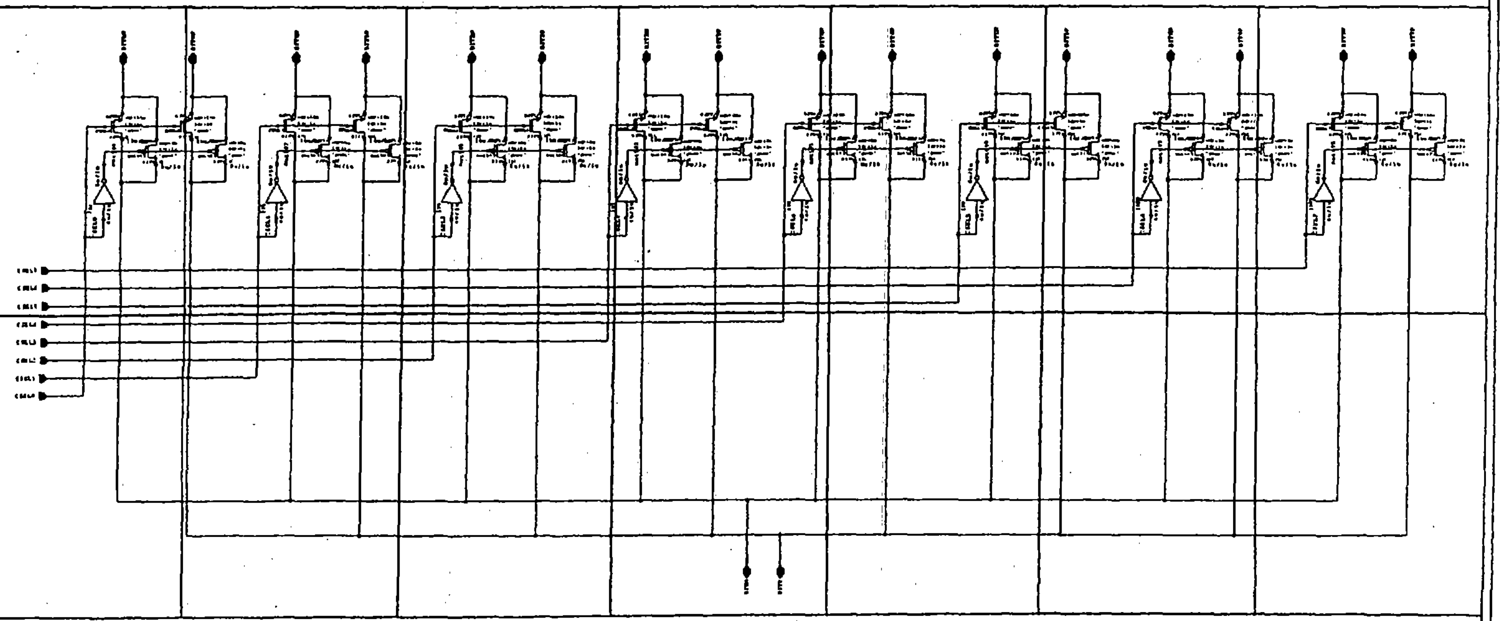
FIG. 7.0308

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03	Rotzoll
RAM Column Select Decode	
3 to 8	
103reva/ramcdec	- / nil
Nov 5 17:21:07 1993	

7.0309AA	7.0309AB	7.0309AC	7.0309AD	7.0309AE	7.0309AF	7.0309AG
7.0309BA	7.0309BB	7.0309BC	7.0309BD	7.0309BE	7.0309BF	7.0309BG

FIG 7.0309



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
[illegible]
RAM Column Selector
8 to 1 MUX
[illegible]
r42
Nov 5 17:19:31 199

FIG. 7.0309

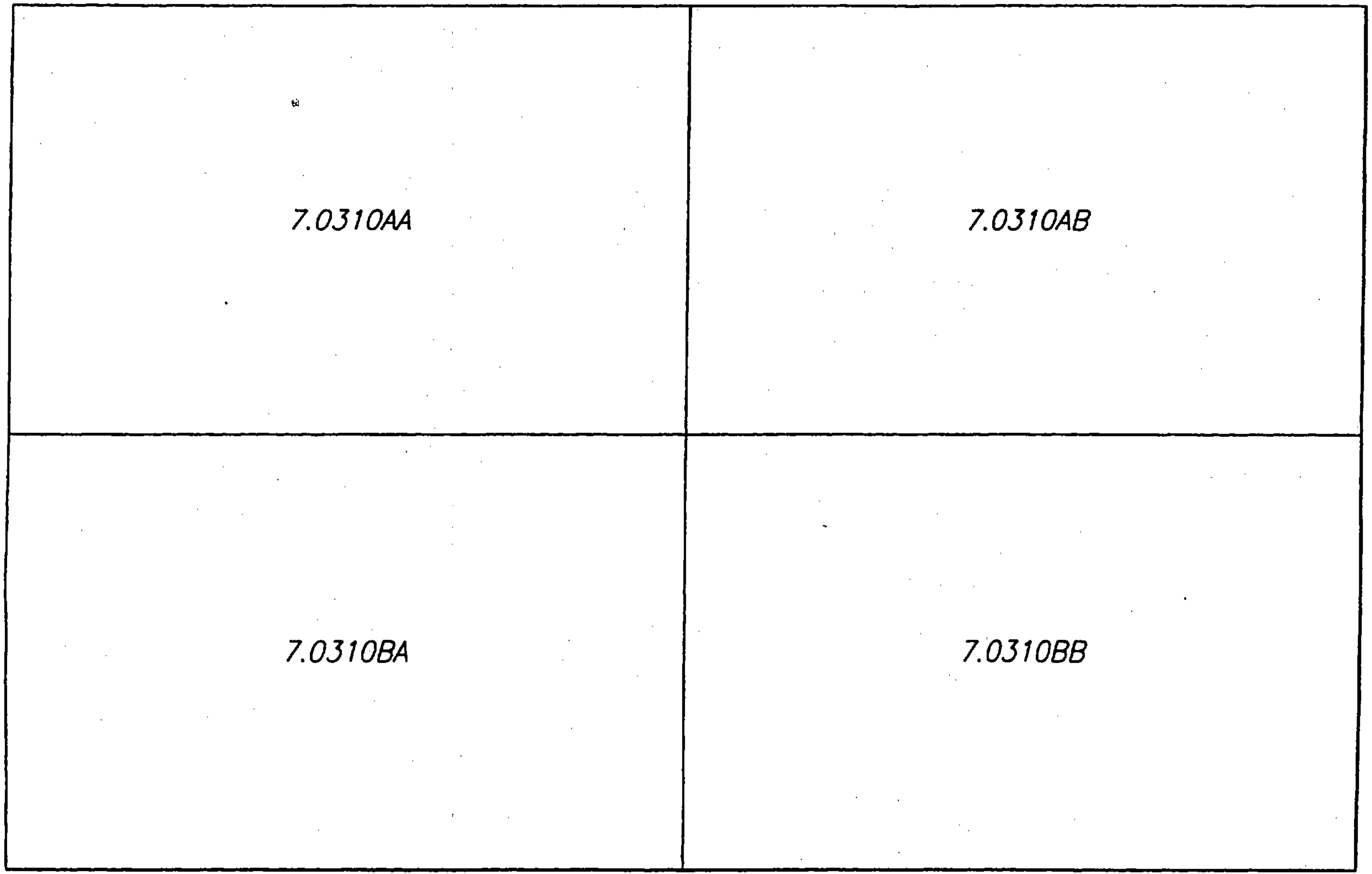


FIG. 7.0310

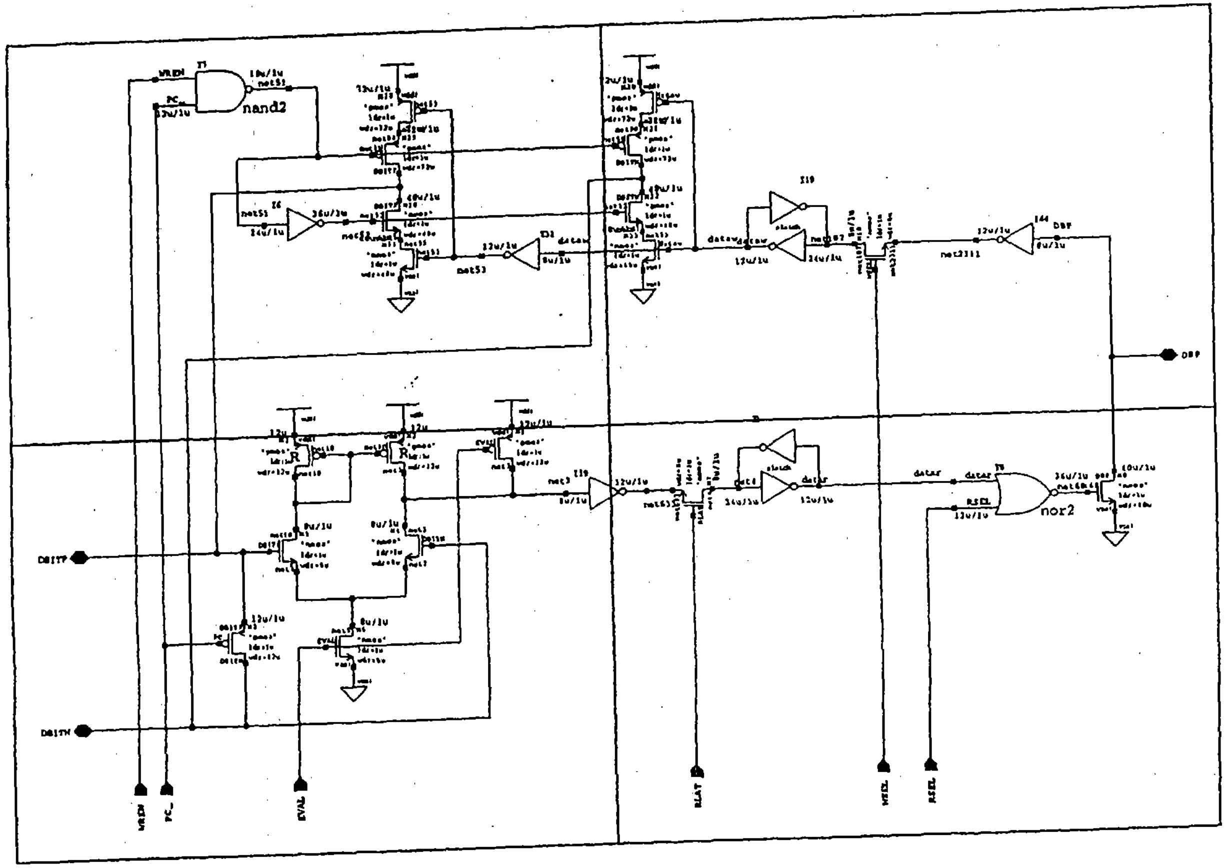


Fig. 7.0310

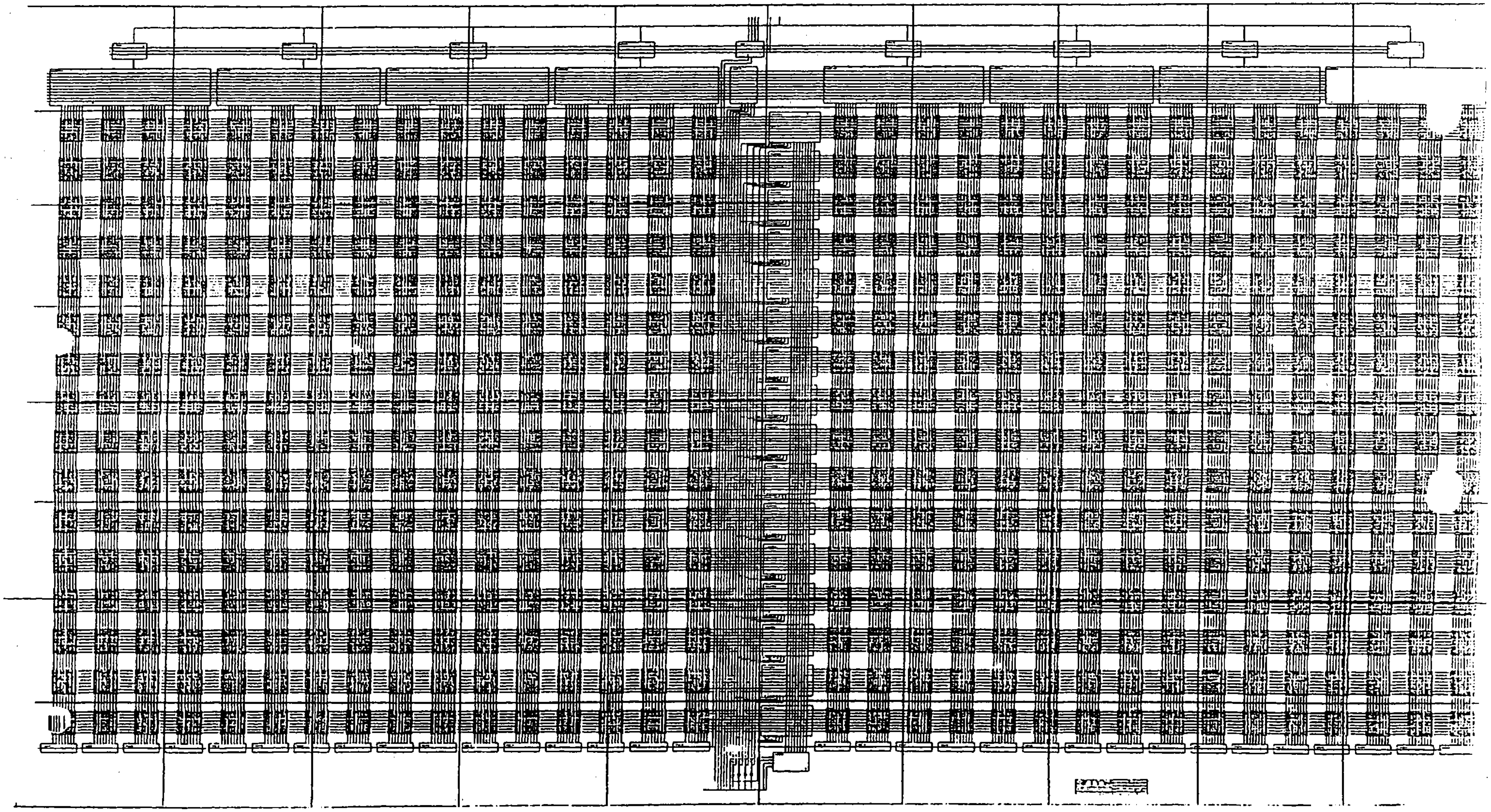
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03	Rotzoll
RAM Databus Interface	
103reva/ramdb	- rdl
Oct 6 12:08:33 1993	

7.04AA	7.04AB	7.04AC	7.04AD	7.04AE	7.04AF	7.04AG	7.04AH	7.04AI	7.04AJ
7.04BA	7.04BB	7.04BC	7.04BD	7.04BE	7.04BF	7.04BG	7.04BH	7.04BI	7.04BJ
7.04CA	7.04CB	7.04CC	7.04CD	7.04CE	7.04CF	7.04CG	7.04CH	7.04CI	7.04CJ
7.04DA	7.04DB	7.04DC	7.04DD	7.04DE	7.04DF	7.04DG	7.04DH	7.04DI	7.04DJ
7.04EA	7.04EB	7.04EC	7.04ED	7.04EE	7.04EF	7.04EG	7.04EH	7.04EI	7.04EJ
7.04FA	7.04FB	7.04FC	7.04FD	7.04FE	7.04FF	7.04FG	7.04FH	7.04FI	7.04FJ
7.04GA	7.04GB	7.04GC	7.04GD	7.04GE	7.04GF	7.04GG	7.04GH	7.04GI	7.04GJ
7.04HA	7.04HB	7.04HC	7.04HD	7.04HE	7.04HF	7.04HG	7.04HH	7.04HI	7.04HJ

Fig. 7.04

FIG. 7.04



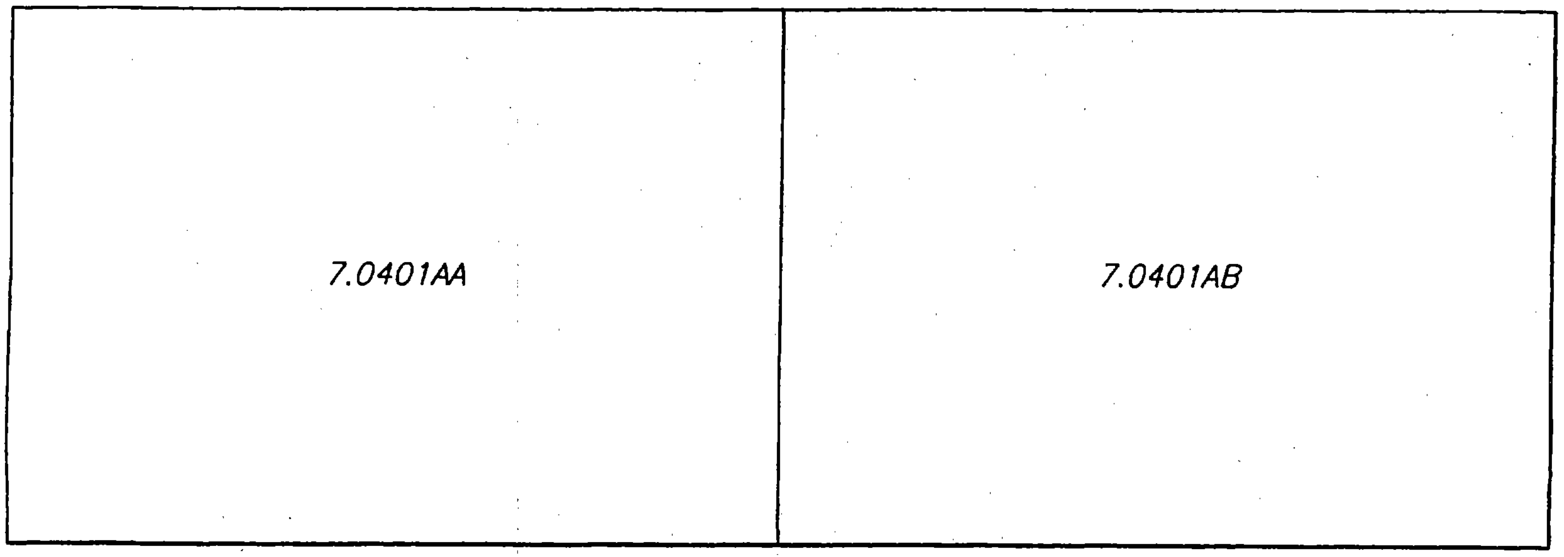
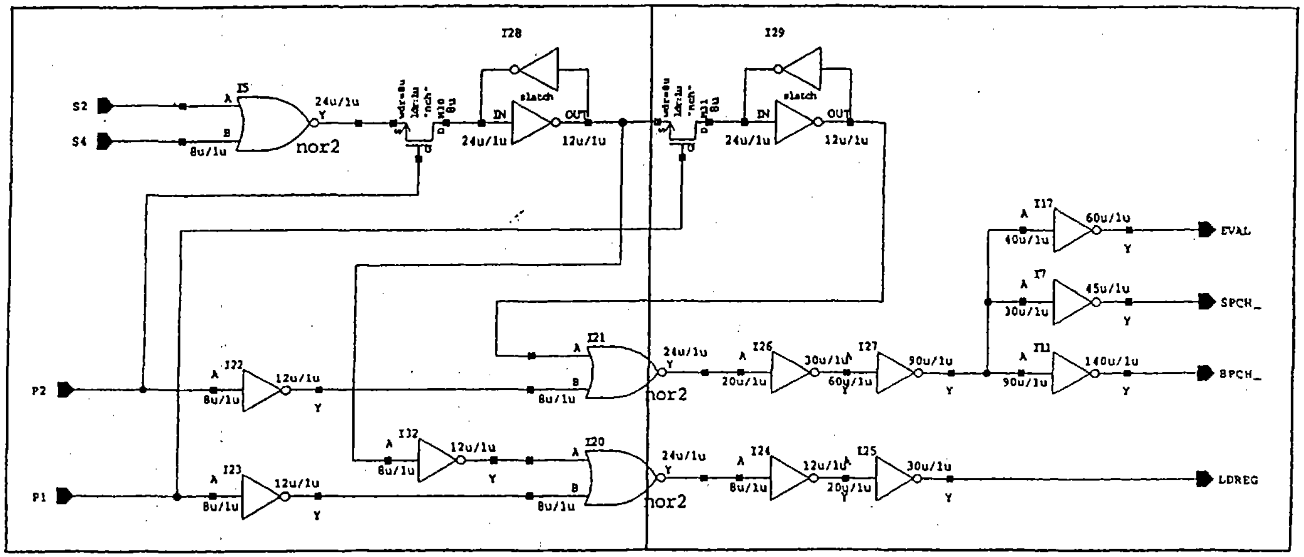


FIG. 7.0401



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03		DESIGNER: Rotzoll	
TITLE: ROM Control Logic			
NAME: 103reva/romctl	REV: -	SIZE: A	
DATE: Oct 3 13:16:28 1993	SHEET:		

FIG. 7.04C

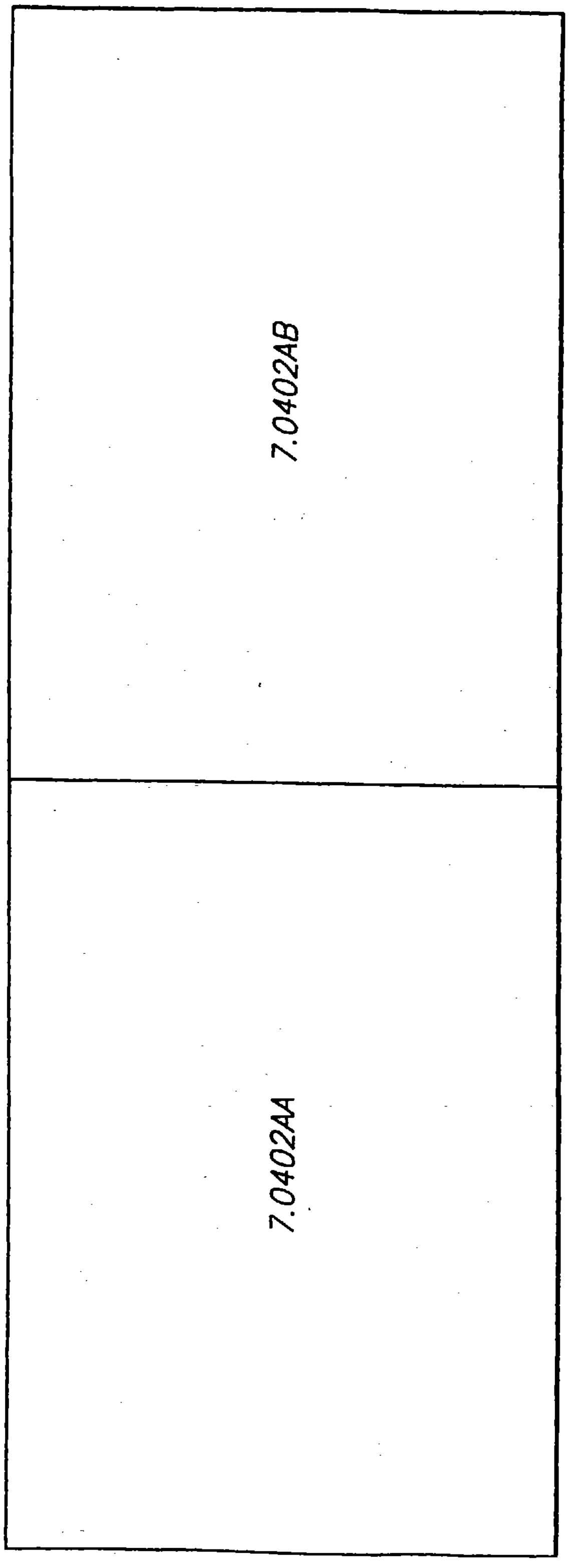
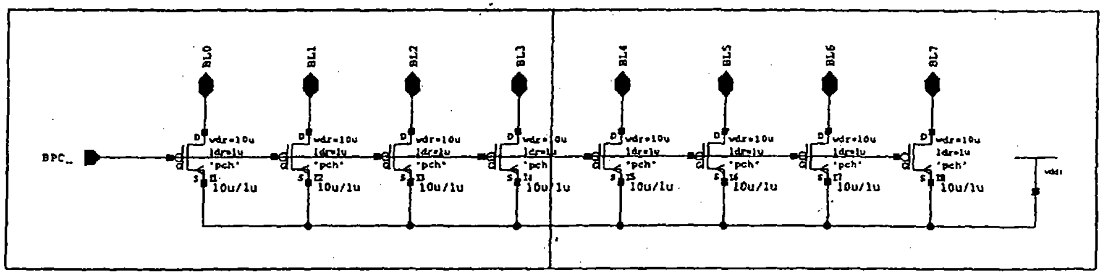


FIG. 7.0402



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: ROM Bit Line Precharge
NAME: 103reva/rompch
REV: -
SIZE: A
DATE: Oct 7 18:09:48 1993
SHEET:

FIG. 7.0902

MI40-030

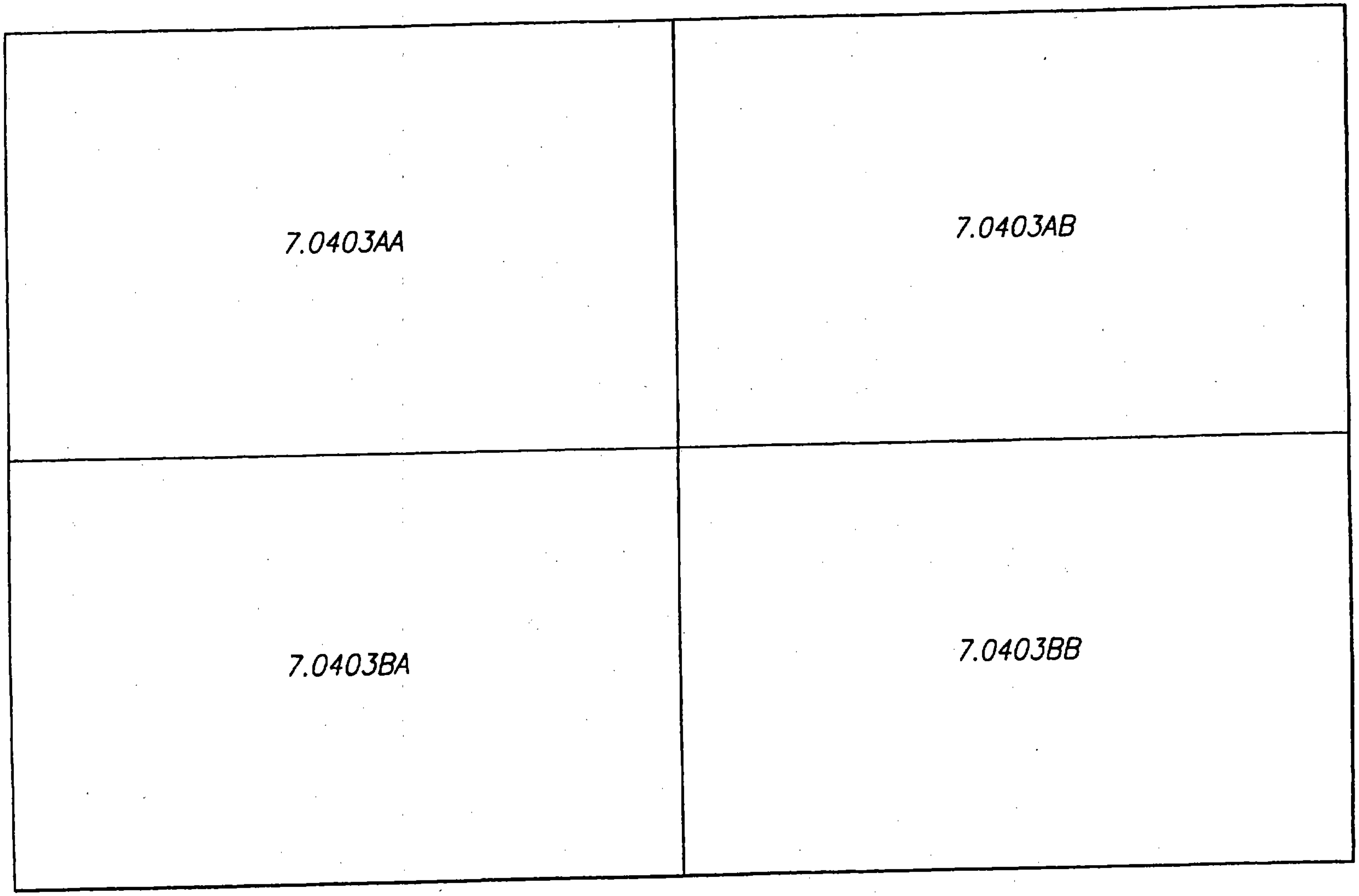
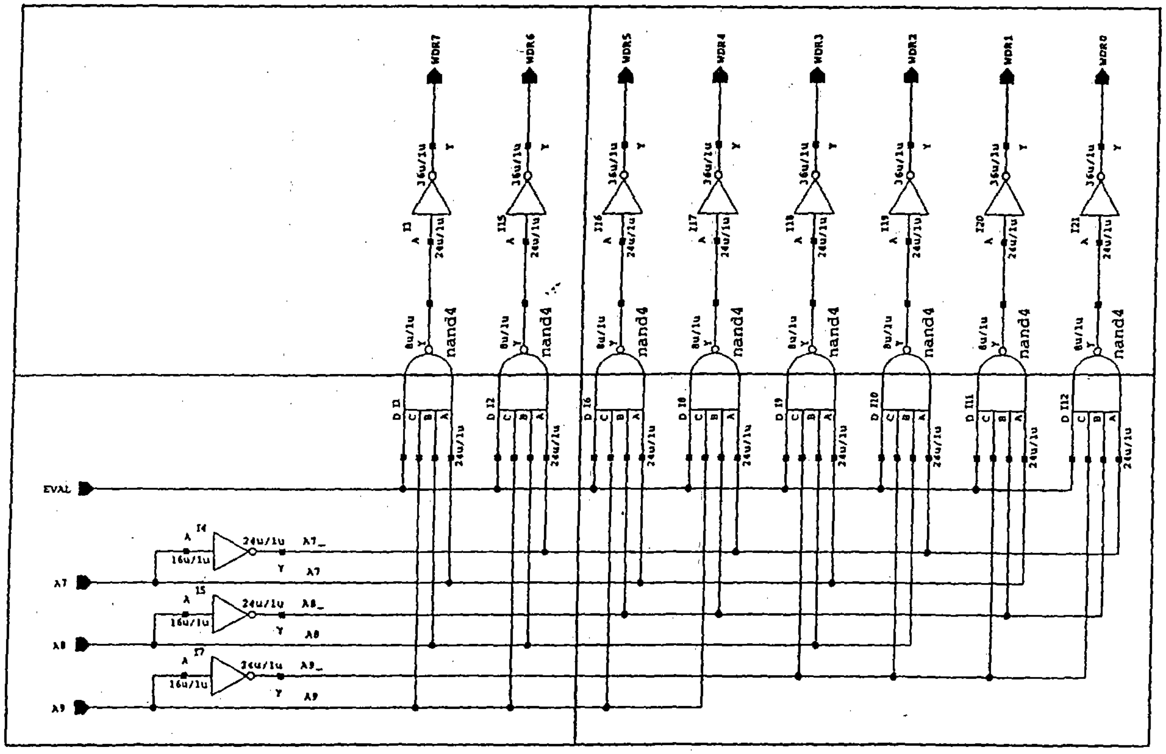


FIG. 7.0403



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: ROM Word Line Driver
NAME: 103reva/romwdr
REV: -
SIZE: A
DATE: Oct 7 18:11:34 1993
SHEET:

FIG. 7.0903

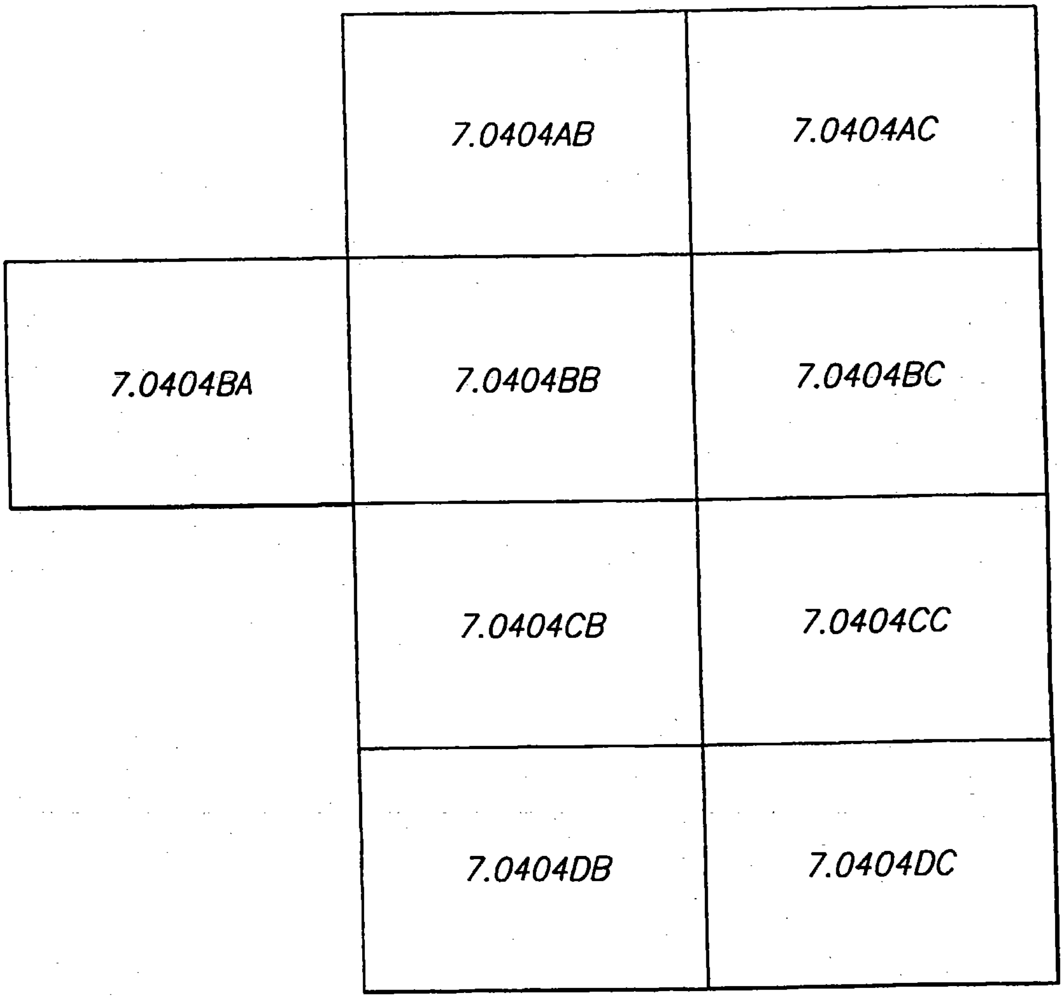

7.0404AB
7.0404AC
7.0404BA
7.0404BB
7.0404BC
7.0404CB
7.0404CC
7.0404DB
7.0404DC

FIG 7.0404

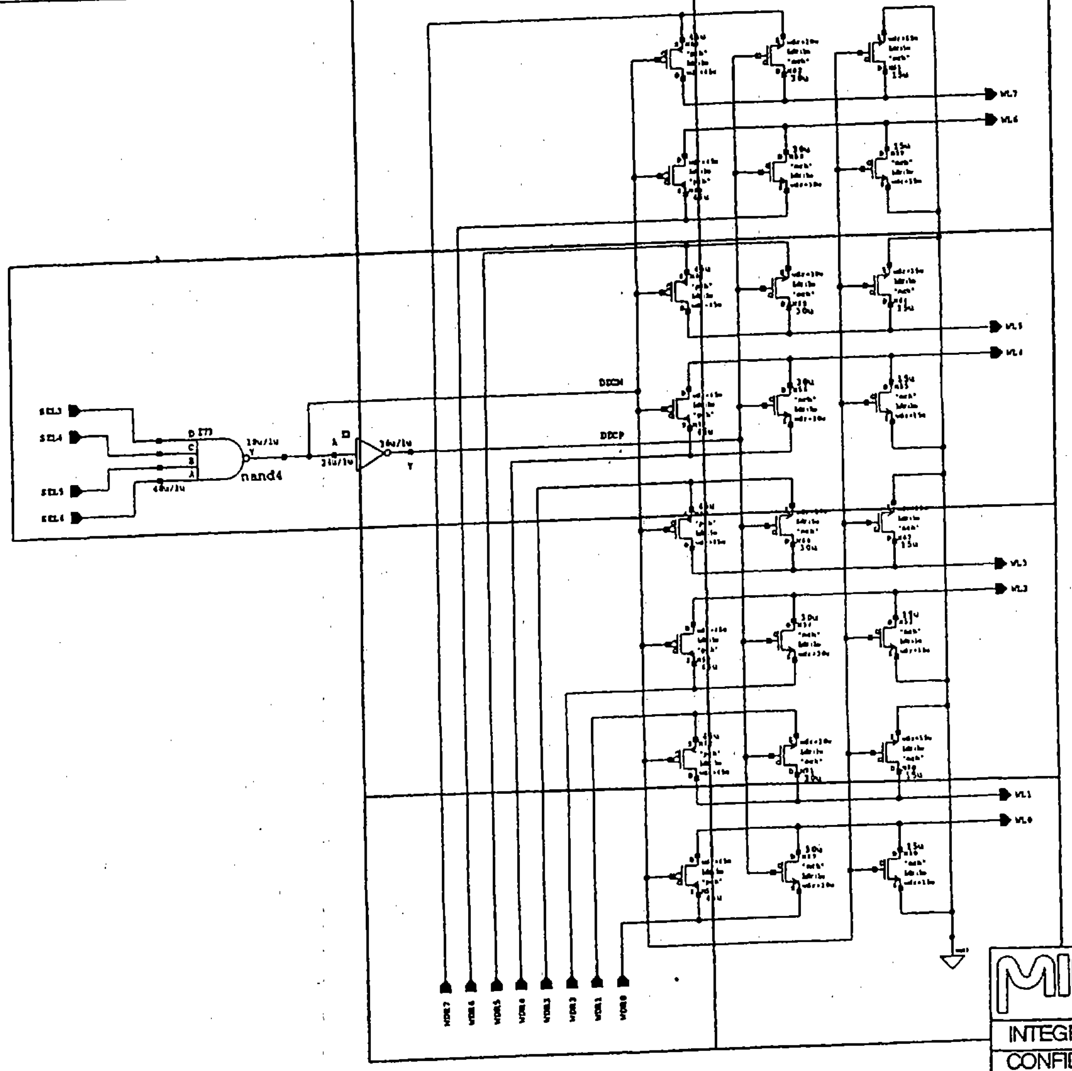


FIG. 7.0404

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03	Rotzoll
Word Block Decoder	
l03reva/romwdec_rev	- | rdl
Nov 5 17:38:09 1993	

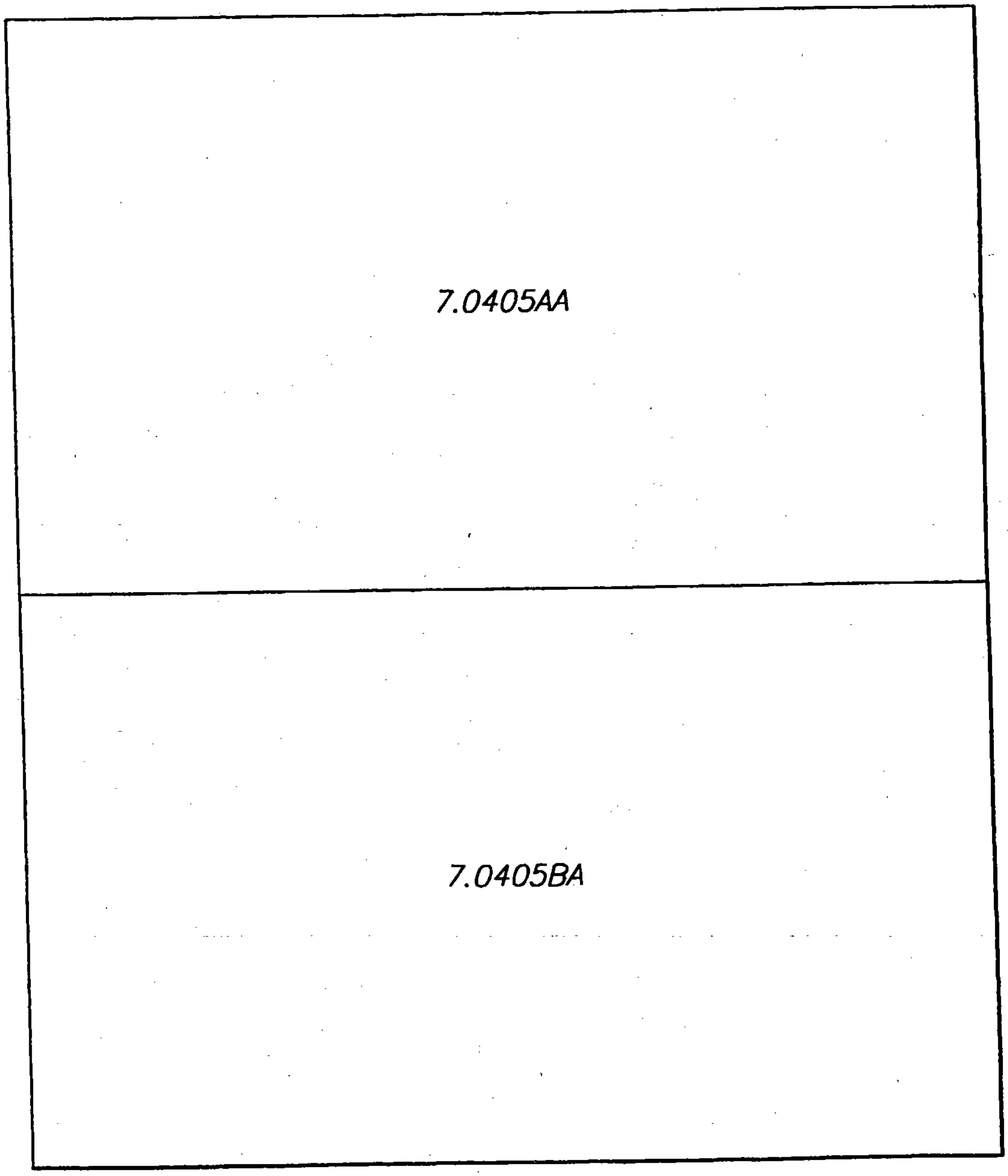


FIG 7.0405

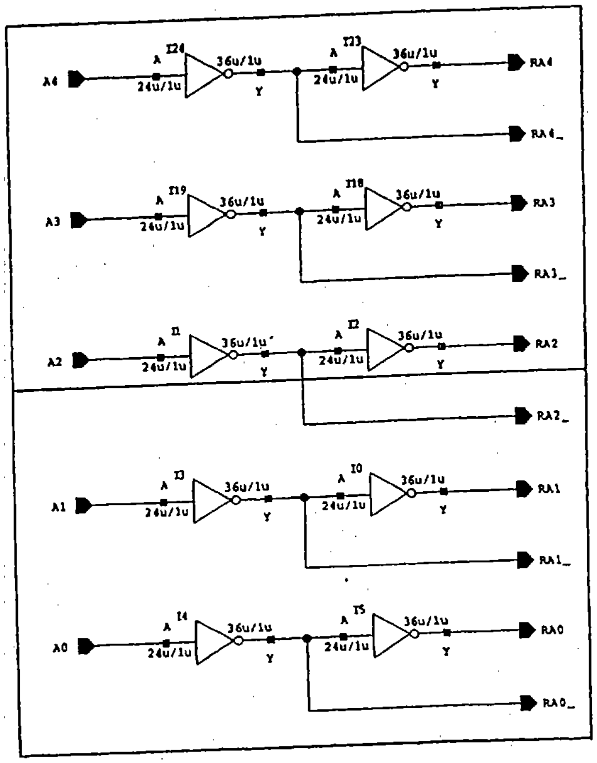


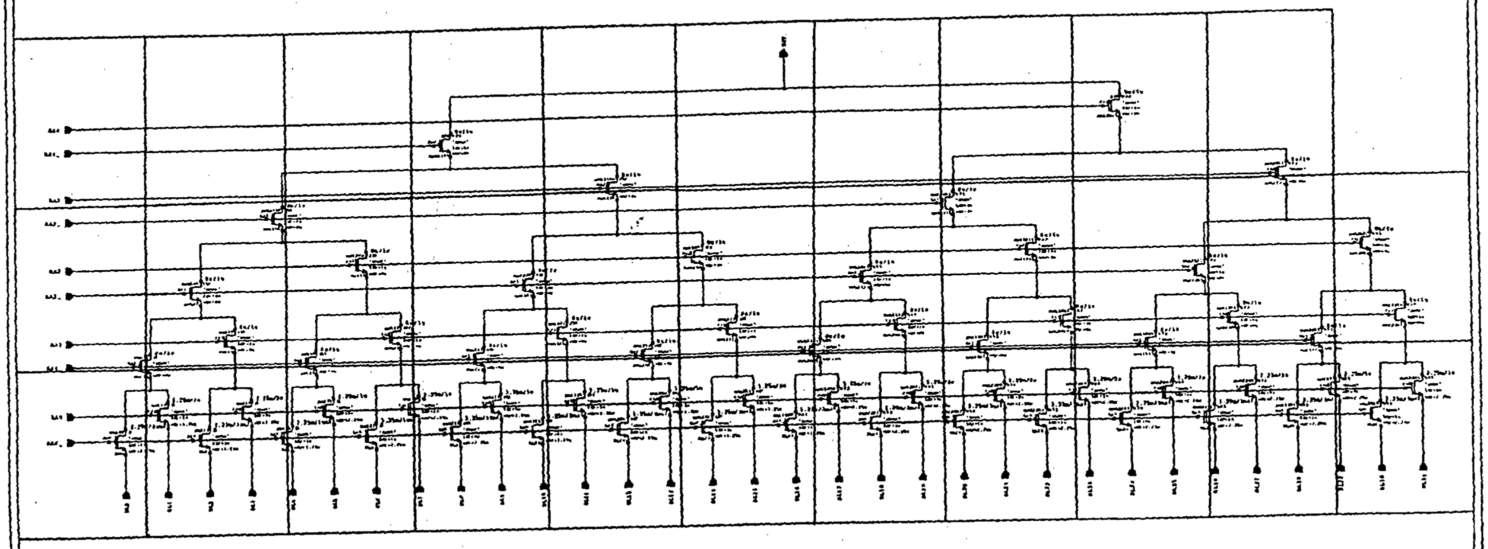
Fig. 7.0905

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: Rotzoll
TITLE: ROM Bit Line Address Driver	
NAME: 103reva/rombldr	REV: - SIZE: A
DATE: Oct 7 12:08:42 1993	SHEET:

7.0406AA	7.0406AB	7.0406AC	7.0406AD	7.0406AE	7.0406AF	7.0406AG	7.0406AH	7.0406AI	7.0406AJ	
7.0406BA	7.0406BB	7.0406BC	7.0406BD	7.0406BE	7.0406BF	7.0406BG	7.0406BH	7.0406BI	7.0406BJ	7.0406BK
7.0406CA	7.0406CB	7.0406CC	7.0406CD	7.0406CE	7.0406CF	7.0406CG	7.0406CH	7.0406CI	7.0406CJ	7.0406CK

Fig 7.0406



MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
Rotoli
ROM Bit Line Decoder
[0]reva/rombldec
-
nl
Oct 7 11:52:02 1995

FIG. 7.040G

MI40-030

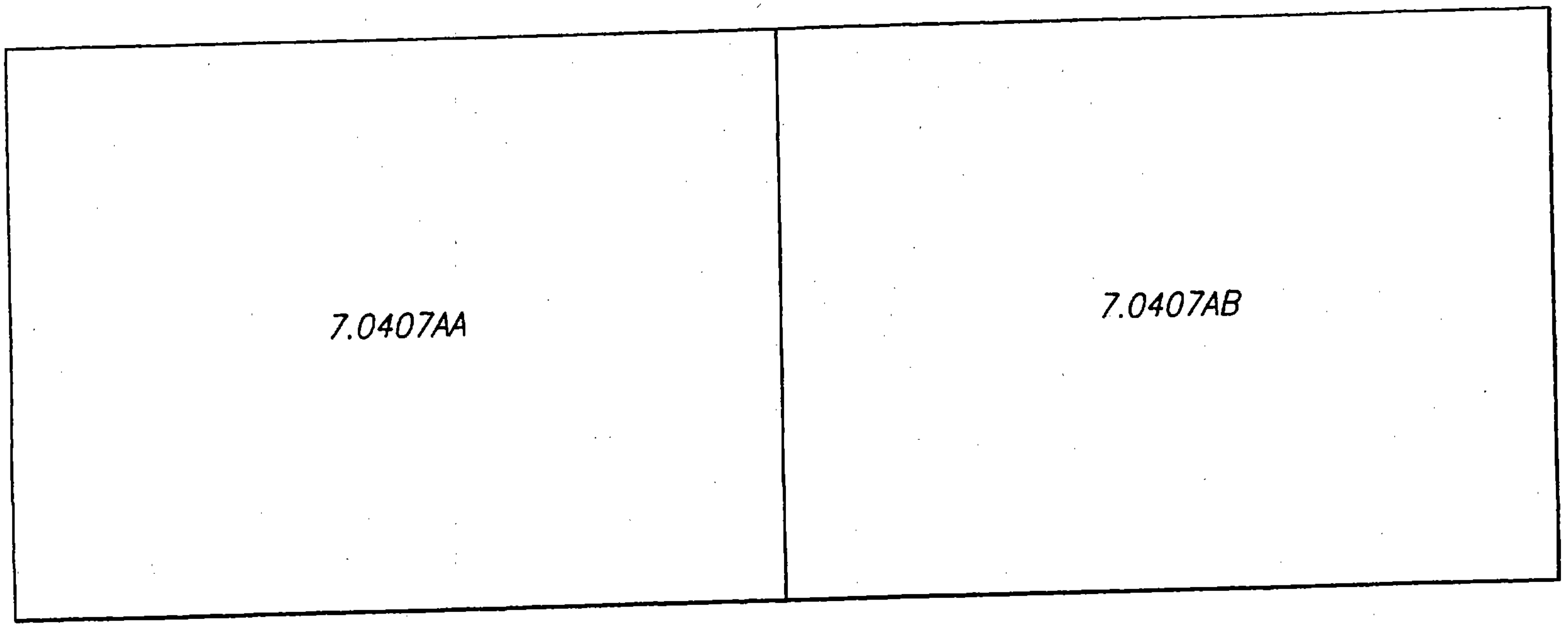
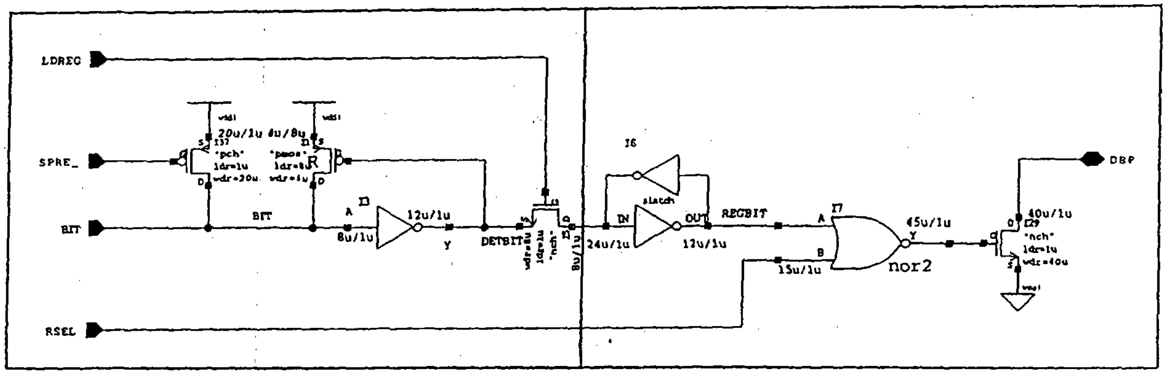


FIG. 7.0407



MICRON COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: ROM Sense Amplifier
NAME: 103reva/romsns
REV: -
SIZE: A
DATE: Oct 7 18:12:58 1993
SHEET:

Fig. 7.0407

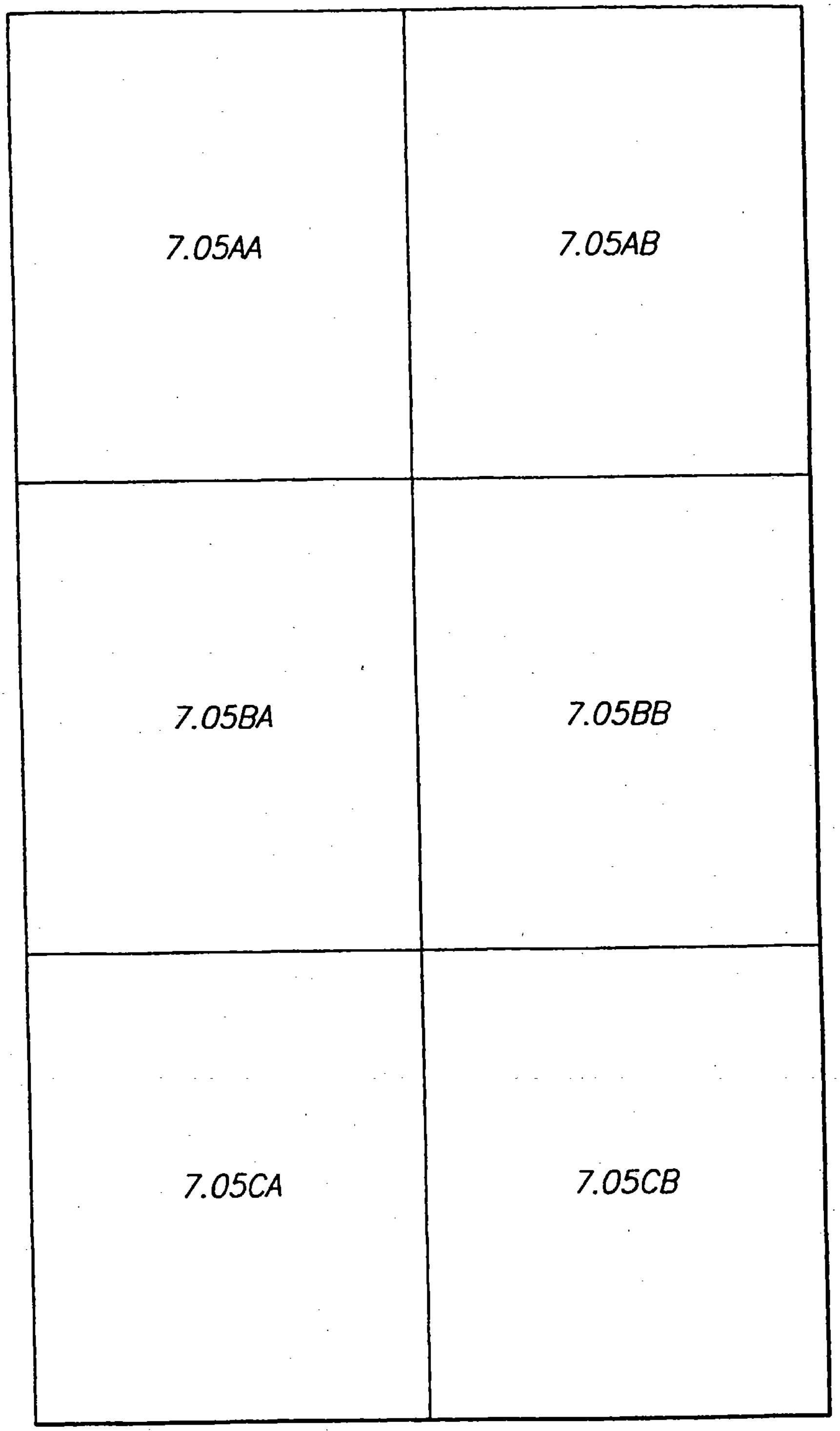


Fig 7.05

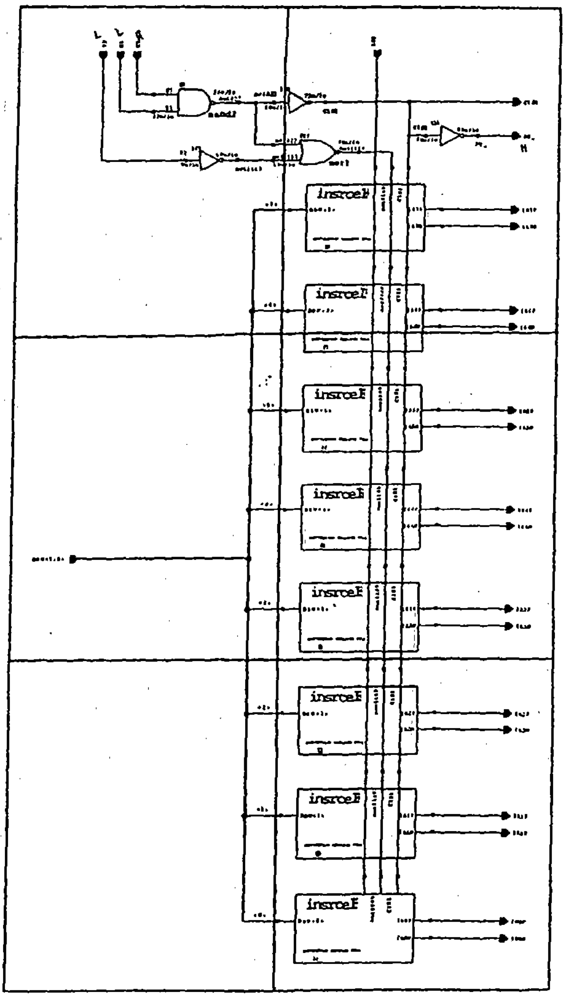


Fig. 7.05

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

LQ3 Rotzoll
Instruction Register
10)revs/insreg - nl
Oct 3 13:17:05 1993

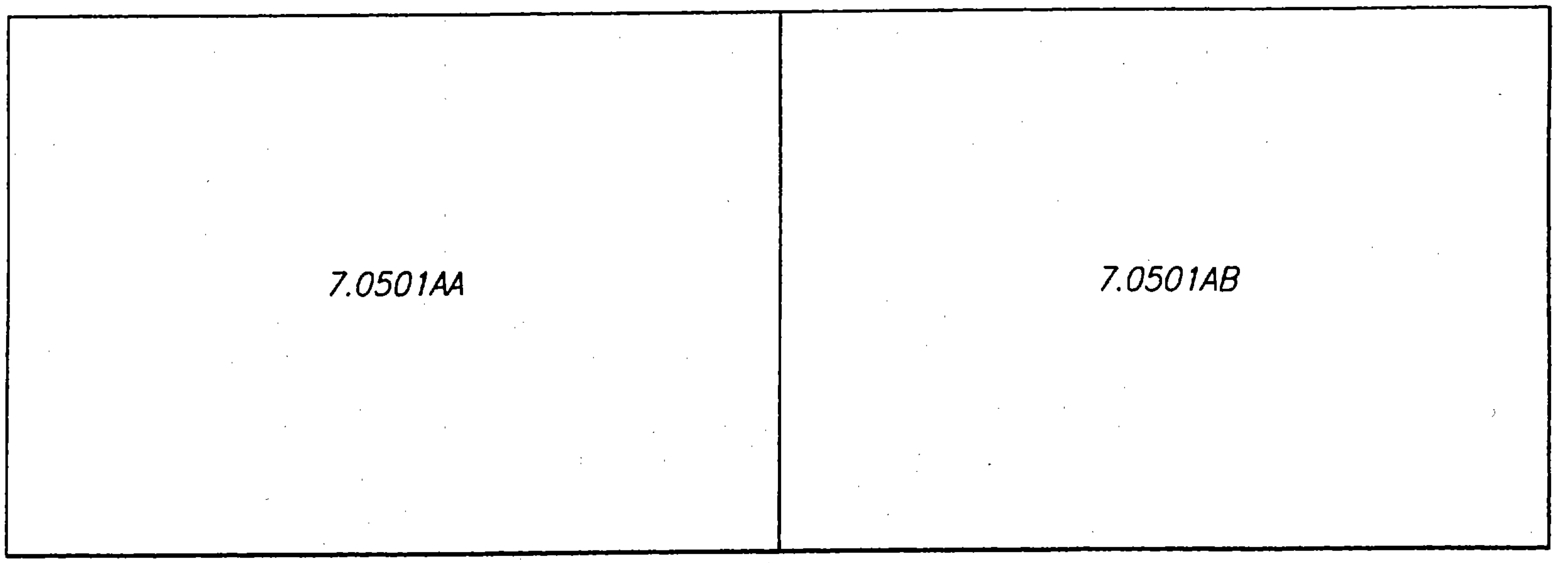


Fig 7.0501

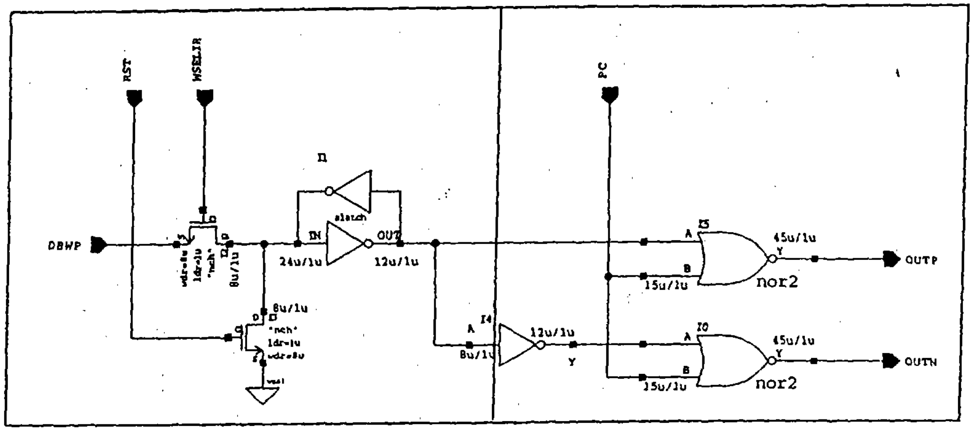


FIG. 7.0501

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: Instruction Register Cell
NAME: 103reva/insrcel
REV: -
SIZE: A
DATE: Oct 5 20:12:49 1993
SHEET:

7.06AA	7.06AB	7.06AC	7.06AD	7.06AE	7.06AF	7.06AG	7.06AH	7.06AI	7.06AJ	7.06AK	7.06AL	7.06AM	7.06AN
	7.06BB	7.06BC	7.06BD	7.06BE	7.06BF	7.06BG	7.06BH	7.06BI	7.06BJ	7.06BK	7.06BL	7.06BM	7.06BN
7.06CA	7.06CB	7.06CC	7.06CD	7.06CE	7.06CF	7.06CG	7.06CH	7.06CI	7.06CJ	7.06CK	7.06CL	7.06CM	7.06CN

Fig 7.06

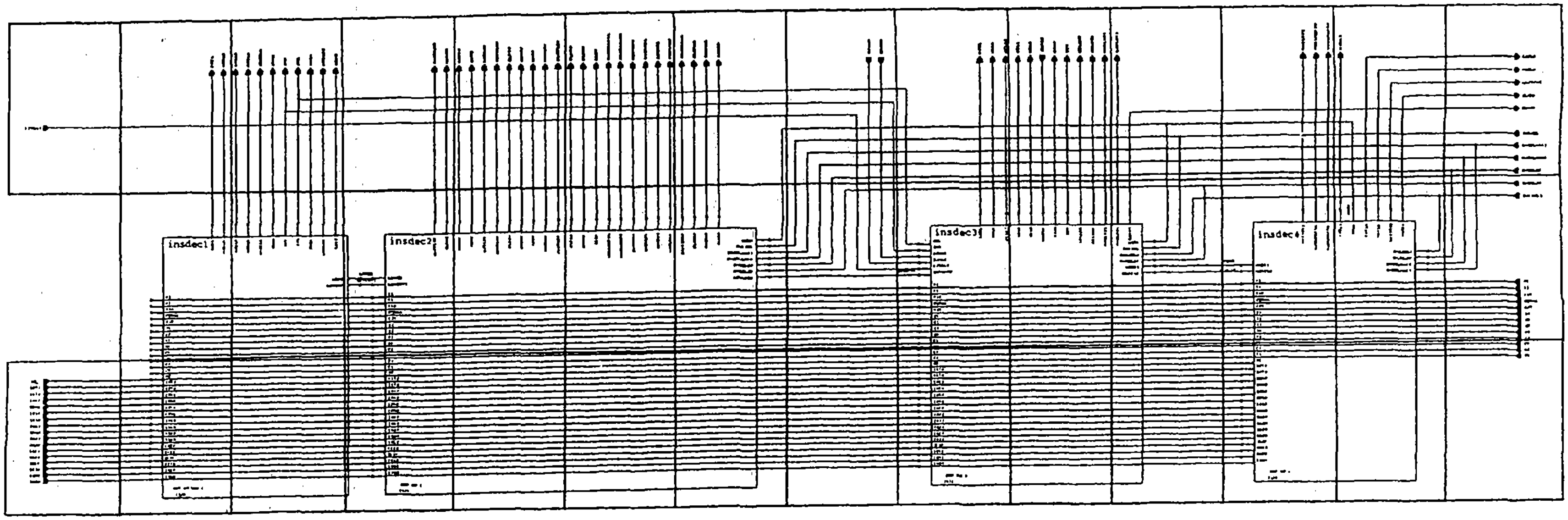


FIG. 7.06

MICRON
COMMUNICATIONS, INC
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

Instruction Decoder PLA

7.0601AA	7.0601AB	7.0601AC	7.0601AD	7.0601AE	7.0601AF	7.0601AG	7.0601AH	7.0601AI
7.0601BA	7.0601BB	7.0601BC	7.0601BD	7.0601BE	7.0601BF	7.0601BG	7.0601BH	7.0601BI
7.0601CA	7.0601CB	7.0601CC	7.0601CD	7.0601CE	7.0601CF	7.0601CG	7.0601CH	7.0601CI
7.0601DA	7.0601DB	7.0601DC	7.0601DD	7.0601DE	7.0601DF	7.0601DG	7.0601DH	7.0601DI
7.0601EA	7.0601EB	7.0601EC	7.0601ED	7.0601EE	7.0601EF	7.0601EG	7.0601EH	7.0601EI
7.0601FA	7.0601FB	7.0601FC	7.0601FD	7.0601FE	7.0601FF	7.0601FG	7.0601FH	7.0601FI
7.0601GA	7.0601GB	7.0601GC	7.0601GD	7.0601GE	7.0601GF	7.0601GG	7.0601GH	7.0601GI
7.0601HA	7.0601HB	7.0601HC	7.0601HD	7.0601HE	7.0601HF	7.0601HG	7.0601HH	7.0601HI

Fig 7.0601

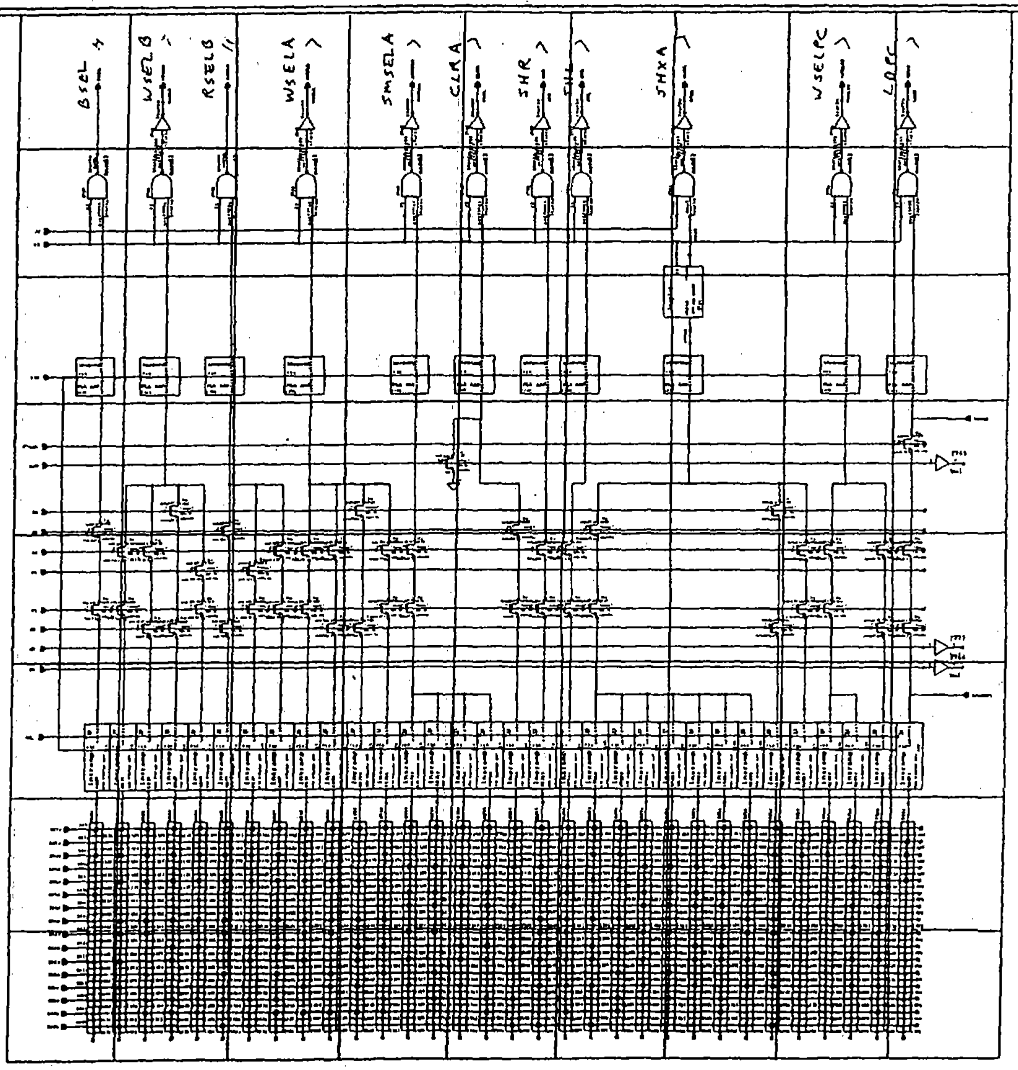
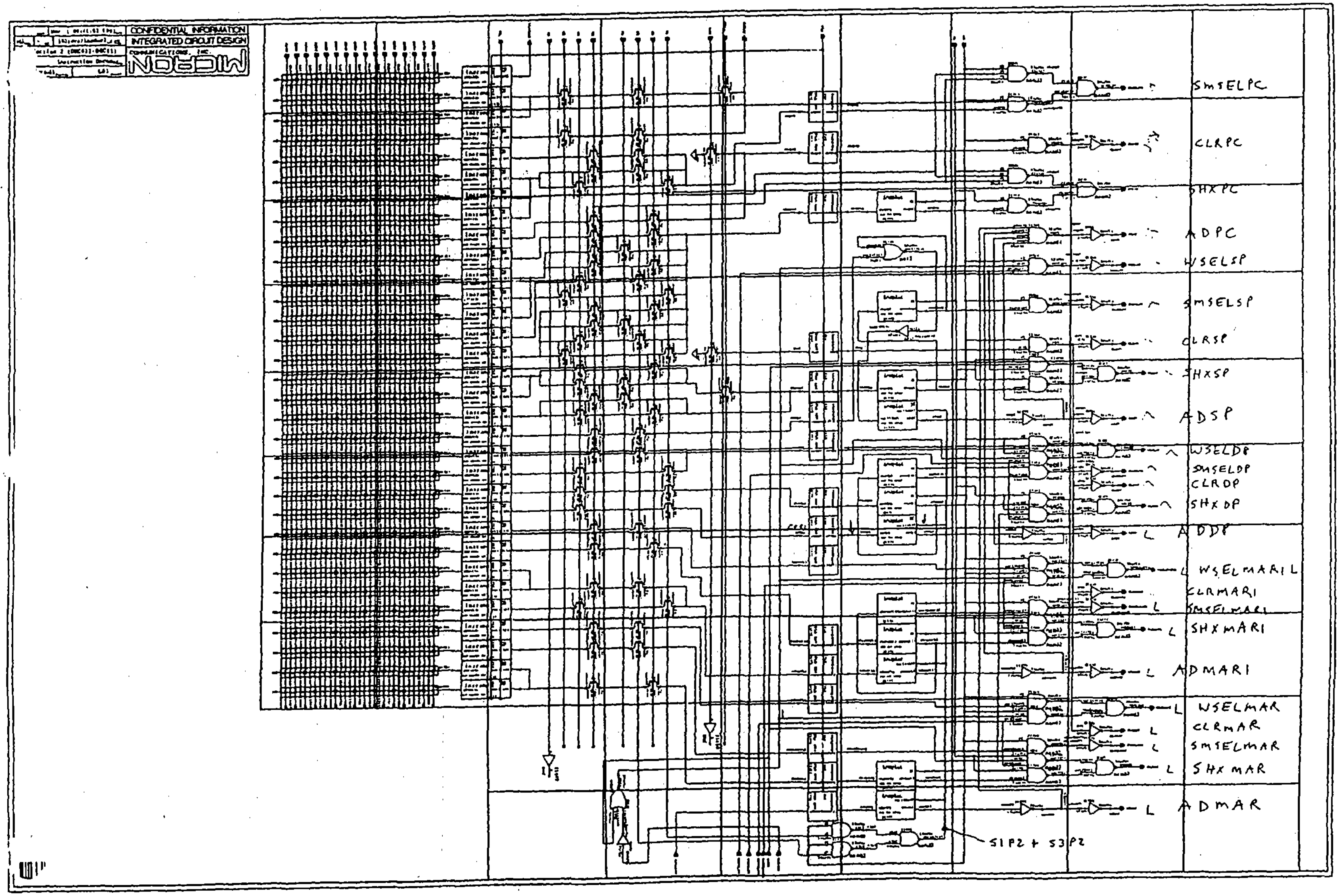


FIG. 7.0601

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

7.0602AA	7.0602AB	7.0602AC	7.0602AD	7.0602AE	7.0602AF	7.0602AG	7.0602AH
7.0602BA	7.0602BB	7.0602BC	7.0602BD	7.0602BE	7.0602BF	7.0602BG	7.0602BH
7.0602CA	7.0602CB	7.0602CC	7.0602CD	7.0602CE	7.0602CF	7.0602CG	7.0602CH
7.0602DA	7.0602DB	7.0602DC	7.0602DD	7.0602DE	7.0602DF	7.0602DG	7.0602DH
7.0602EA	7.0602EB	7.0602EC	7.0602ED	7.0602EE	7.0602EF	7.0602EG	7.0602EH
7.0602FA	7.0602FB	7.0602FC	7.0602FD	7.0602FE	7.0602FF	7.0602FG	7.0602FH
7.0602GA	7.0602GB	7.0602GC	7.0602GD	7.0602GE	7.0602GF	7.0602GG	7.0602GH
7.0602HA	7.0602HB	7.0602HC	7.0602HD	7.0602HE	7.0602HF	7.0602HG	7.0602HH
		7.0602IC	7.0602ID	7.0602IE	7.0602IF	7.0602IG	7.0602IH
		7.0602JC	7.0602JD	7.0602JE	7.0602JF	7.0602JG	7.0602JH

Fig 7.0602



- ADPC is hig [illegible]
one of these is asg
ADSP, ADDP, ADMAR
ADMARI

FIG. 7.0602

7.0603AA	7.0603AB	7.0603AC	7.0603AD	7.0603AE	7.0603AF		7.0603AH	7.0603AI	7.0603AJ	
7.0603BA	7.0603BB	7.0603BC	7.0603BD	7.0603BE	7.0603BF	7.0603BG	7.0603BH	7.0603BI	7.0603BJ	7.0603BK
7.0603CA	7.0603CB	7.0603CC	7.0603CD	7.0603CE	7.0603CF	7.0603CG	7.0603CH	7.0603CI	7.0603CJ	
7.0603DA	7.0603DB	7.0603DC	7.0603DD	7.0603DE	7.0603DF	7.0603DG	7.0603DH	7.0603DI	7.0603DJ	
7.0603EA	7.0603EB	7.0603EC	7.0603ED	7.0603EE	7.0603EF	7.0603EG	7.0603EH	7.0603EI	7.0603EJ	
7.0603FA	7.0603FB	7.0603FC	7.0603FD	7.0603FE	7.0603FF	7.0603FG	7.0603FH	7.0603FI	7.0603FJ	
7.0603GA	7.0603GB	7.0603GC	7.0603GD	7.0603GE	7.0603GF	7.0603GG	7.0603GH	7.0603GI	7.0603GJ	
7.0603HA	7.0603HB	7.0603HC	7.0603HD	7.0603HE	7.0603HF	7.0603HG	7.0603HH	7.0603HI	7.0603HJ	
7.0603IA	7.0603IB	7.0603IC	7.0603ID	7.0603IE	7.0603IF	7.0603IG	7.0603IH	7.0603II	7.0603IJ	
		7.0603JC	7.0603JD	7.0603JE	7.0603JF	7.0603JG		7.0603JI		

FIG. 7.0603

0 0 – – 0 – – 0

CBC clear carry

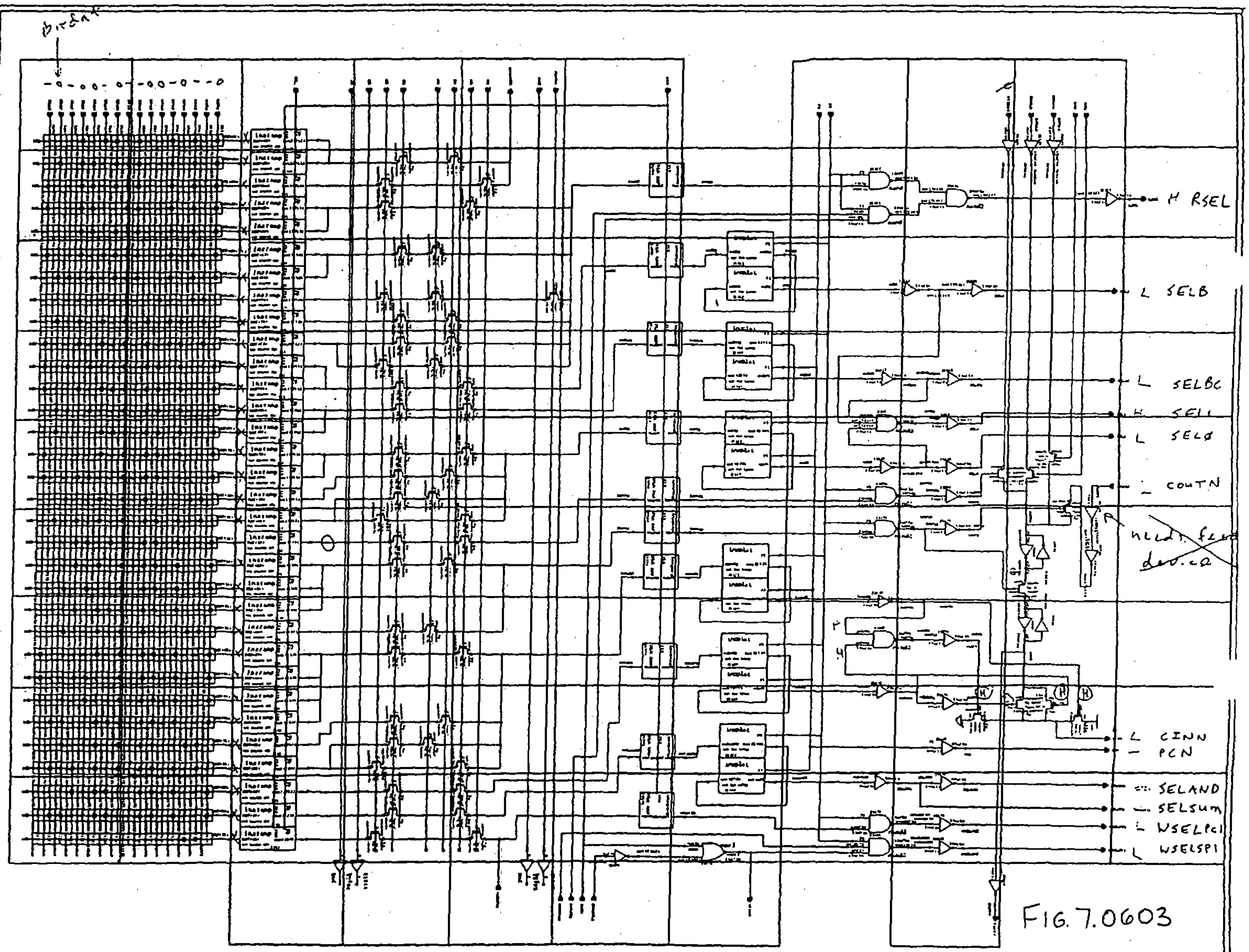


FIG. 7.0603

7.0604AA	7.0604AB	7.0604AC	7.0604AD	7.0604AE	7.0604AF	7.0604AG	7.0604AH	7.0604AI
7.0604BA	7.0604BB	7.0604BC	7.0604BD	7.0604BE	7.0604BF	7.0604BG	7.0604BH	7.0604BI
7.0604CA	7.0604CB	7.0604CC	7.0604CD	7.0604CE	7.0604CF	7.0604CG	7.0604CH	7.0604CI
7.0604DA	7.0604DB	7.0604DC	7.0604DD	7.0604DE	7.0604DF	7.0604DG	7.0604DH	7.0604DI
7.0604EA	7.0604EB	7.0604EC	7.0604ED	7.0604EE	7.0604EF	7.0604EG	7.0604EH	7.0604EI
7.0604FA	7.0604FB	7.0604FC	7.0604FD	7.0604FE	7.0604FF	7.0604FG	7.0604FH	7.0604FI
7.0604GA	7.0604GB	7.0604GC	7.0604GD	7.0604GE	7.0604GF	7.0604GG	7.0604GH	7.0604GI
7.0604HA	7.0604HB	7.0604HC	7.0604HD	7.0604HE	7.0604HF	7.0604HG		
7.0604IA	7.0604IB	7.0604IC	7.0604ID	7.0604IE	7.0604IF	7.0604IG		
7.0604JA	7.0604JB	7.0604JC	7.0604JD	7.0604JE	7.0604JF	7.0604JG	7.0604JH	7.0604JI

Fig 7.0604

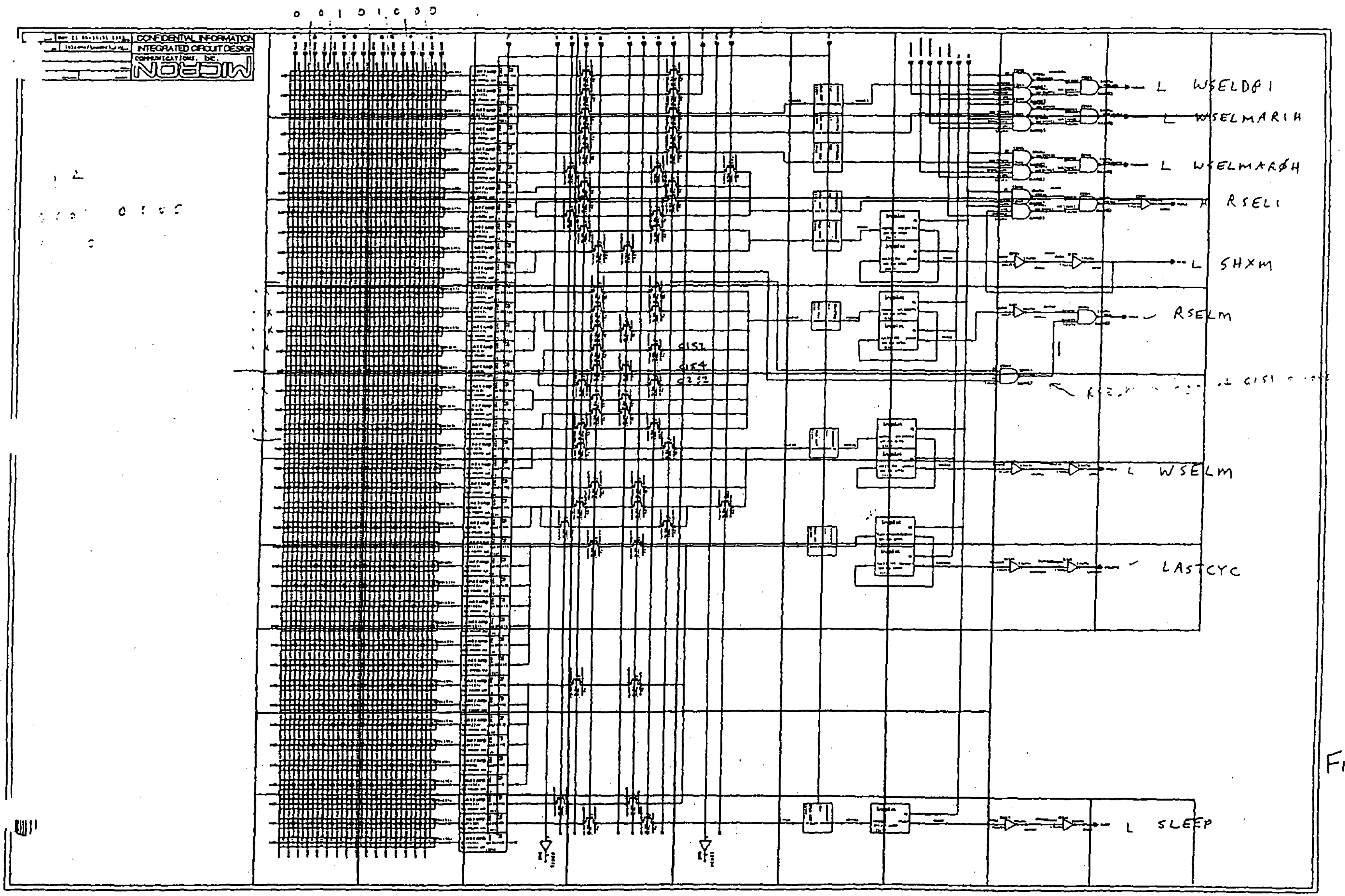
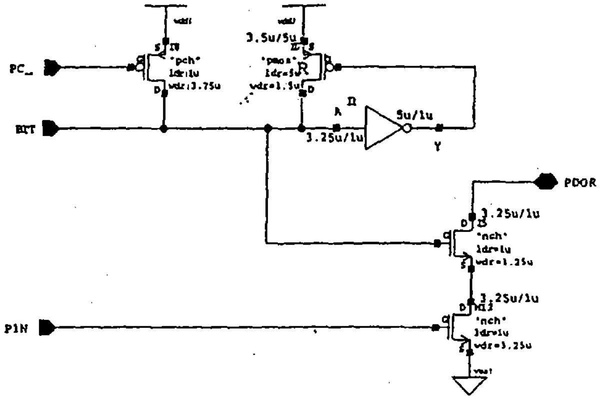

CONFIDENTIAL INFORMATION
INTEGRATED CIRCUIT DESIGN
COMMUNICATIONS, INC.
MICRON
L WSELD01
L WSELMAR1H
L WSELMAR0H
H RSEL1
L SHXM
RSELM
L WSELM
LASTCYC
L SLEEP
d1S2
d1S4
d2S2

FIG. 7.06

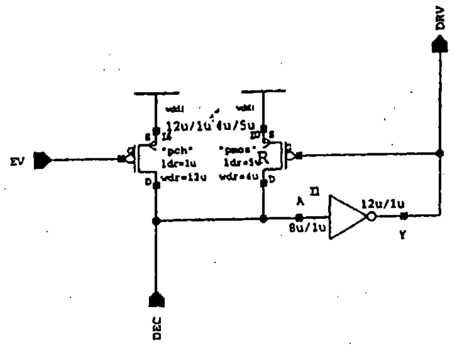


MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: Rotzoll
TITLE: Instruction Decoder ROM Amp	
NAME: 103reva/insramp	REV: - SIZE: A
DATE: Oct 6 12:20:55 1993	SHEET:

FIG. 7.060401

Fig. 7.060402



MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: Instruction Decoder PLA Amp
NAME: 103reva/inspamp
REV: -
SIZE: A
DATE: Oct 6 12:21:34 1993
SHEET:

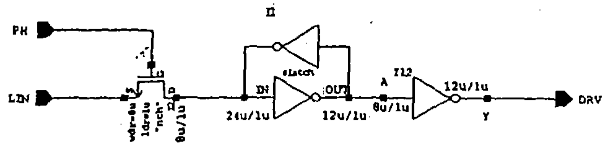


FIG. 7.060903

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: Instruction Decoder PLA Latch
NAME: 103reva/insplat
REV: -
SIZE: A
DATE: Sep 29 16:10:56 1993
SHEET:

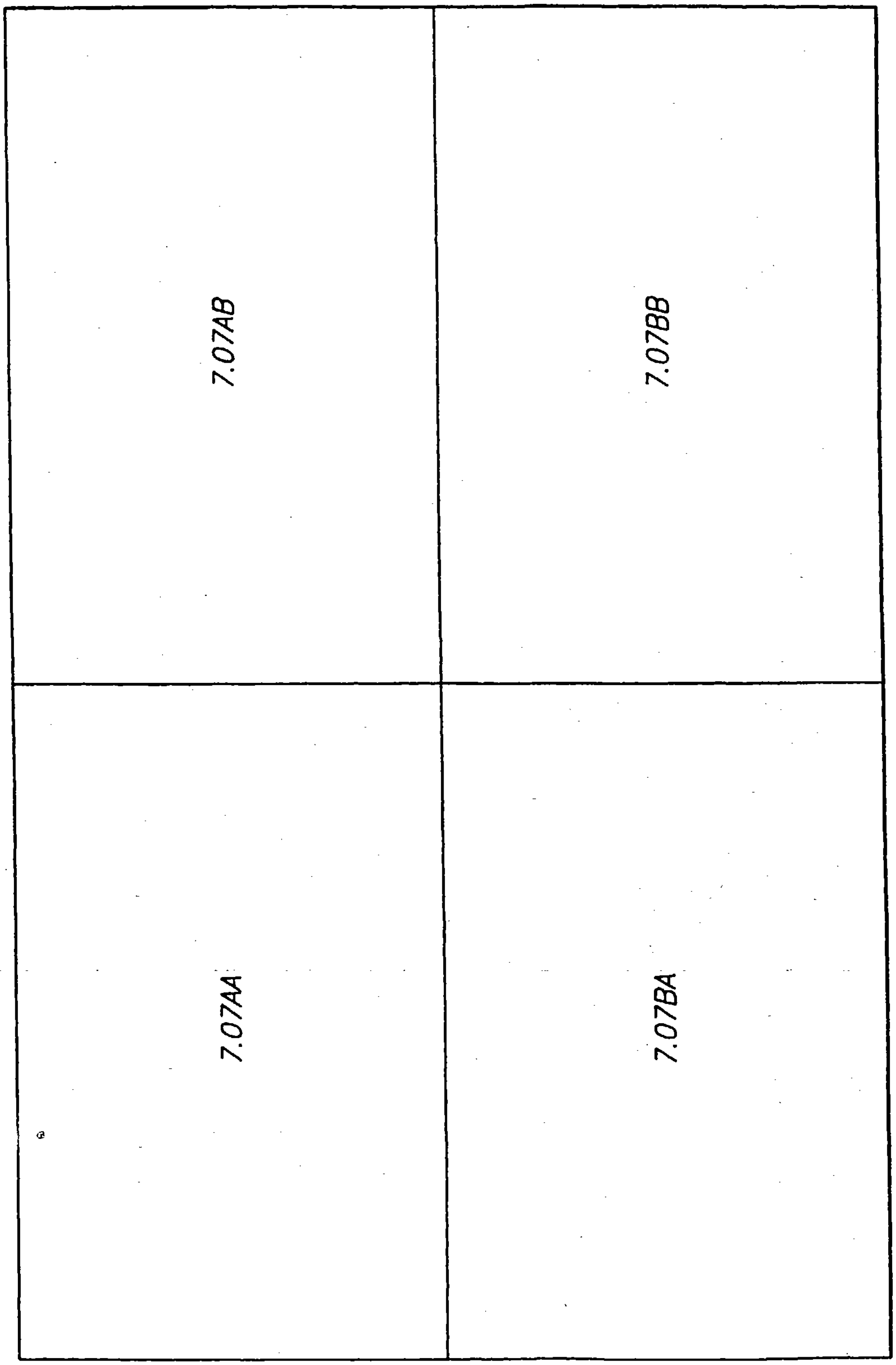


FIG. 7.07

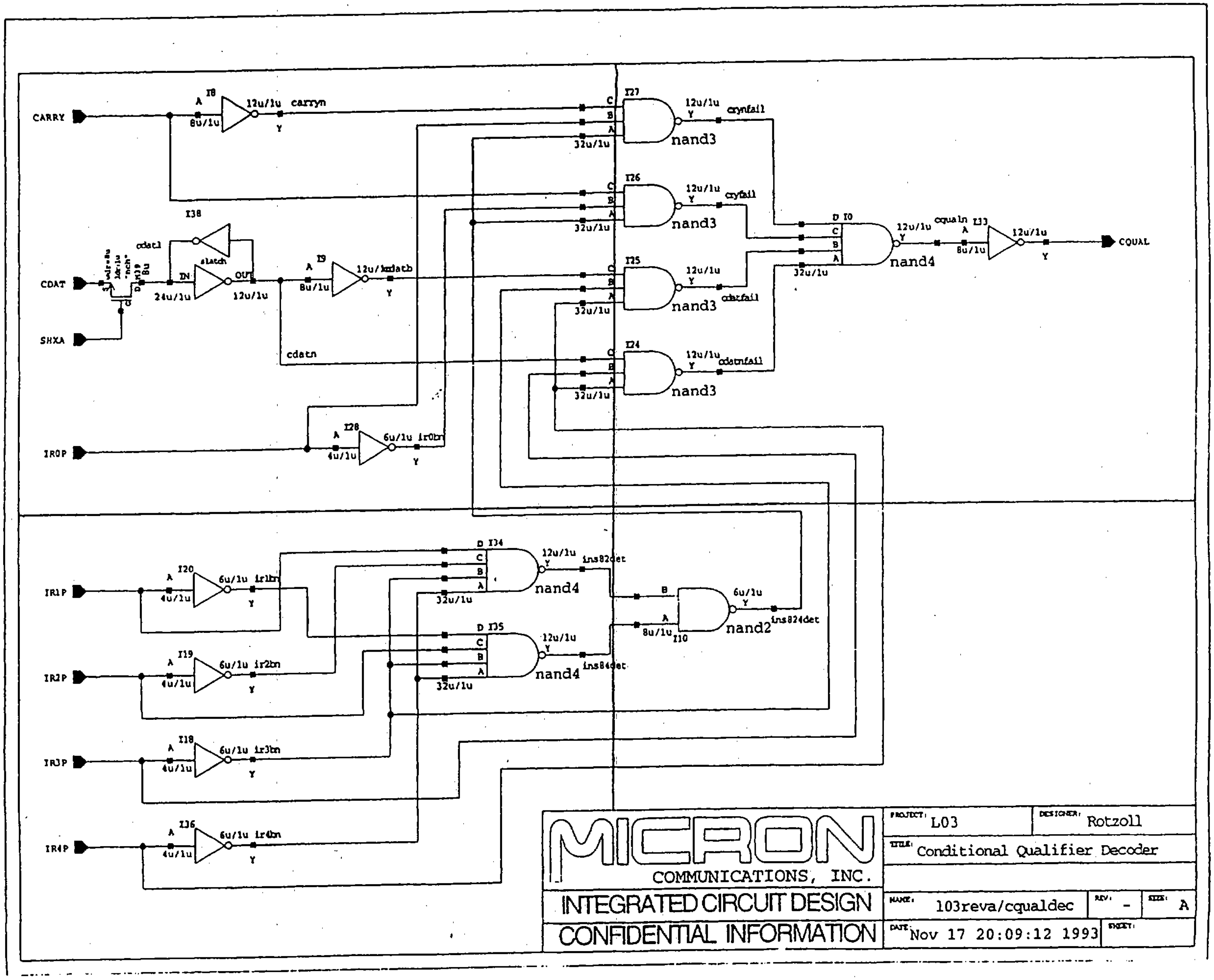

CARRY
CDAT
SHXA
IR0P
IR1P
IR2P
IR3P
IR4P
COQUAL
I8
I9
I10
I13
I18
I19
I20
I24
I25
I26
I27
I28
I34
I35
I36
I38
carryn
cdatl
slatch
IN
OUT
cdatn
ir0bn
ir1bn
ir2bn
ir3bn
ir4bn
crynfail
cryfail
cdatfail
cdatnfail
cqualn
ins82det
ins84det
ins824det
nand2
nand3
nand4
8u/1u
12u/1u
24u/1u
32u/1u
6u/1u
4u/1u
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
PROJECT: L03
DESIGNER: Rotzoll
TITLE: Conditional Qualifier Decoder
NAME: 103reva/cqualdec
REV: -
SIZE: A
DATE: Nov 17 20:09:12 1993
SHEET:

FIG. 7.07

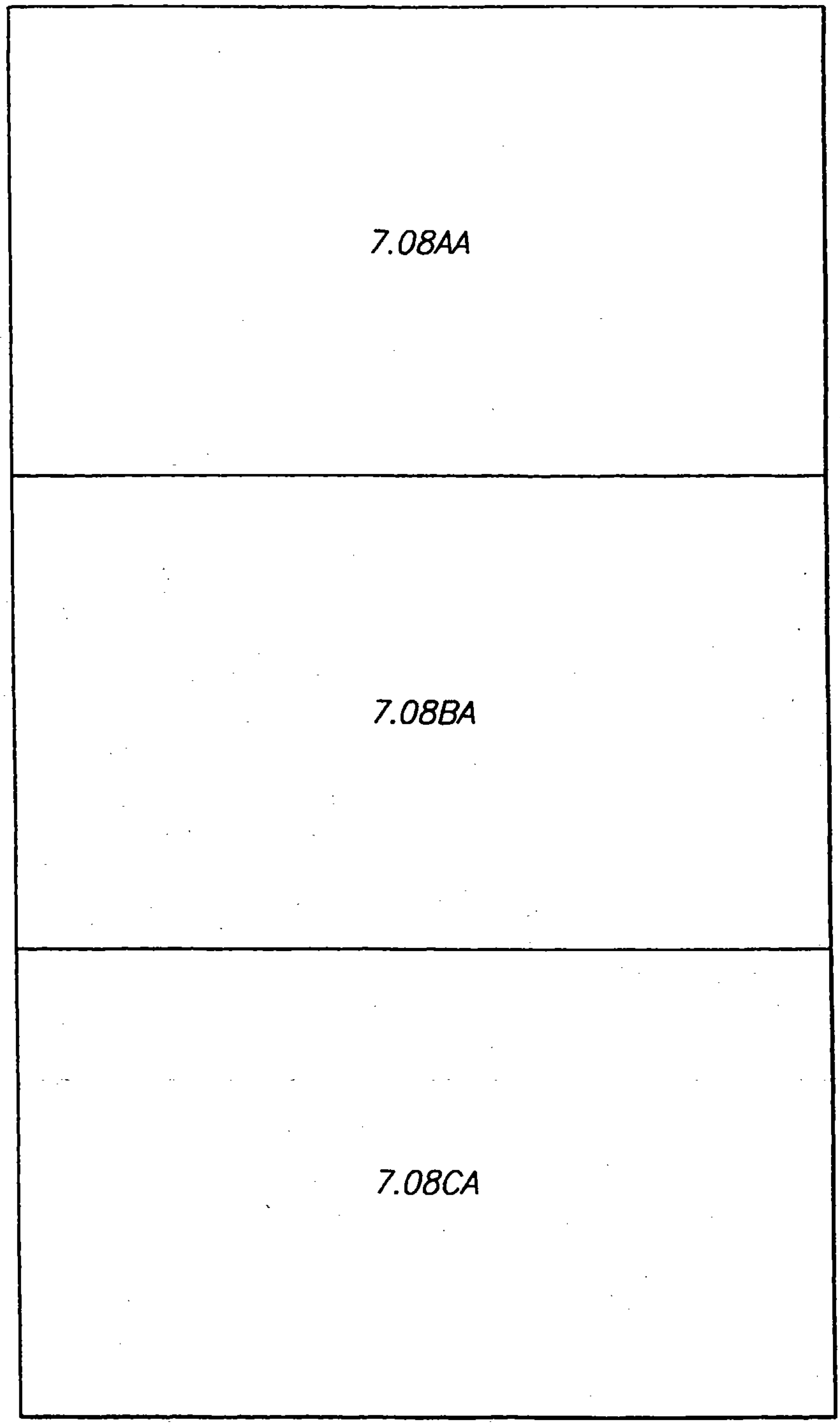


Fig 7.08

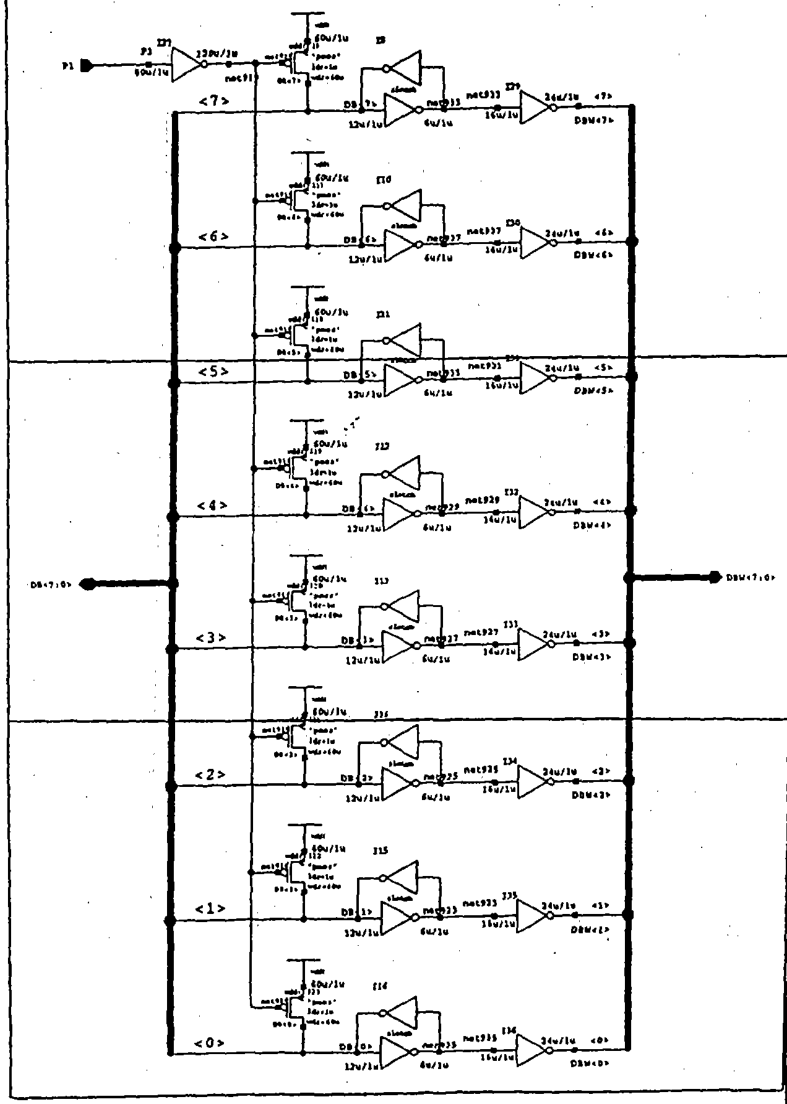


FIG. 7.08

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
Rotzoll
Databus Latch/Precharge
103reva/dblatch
-
nil
Oct 1 14:51:49 1993

7.09AA	7.09AB	7.09AC	7.09AD	7.09AE	7.09AF
7.09BA	7.09BB	7.09BC	7.09BD	7.09BE	7.09BF

FIG 7.09

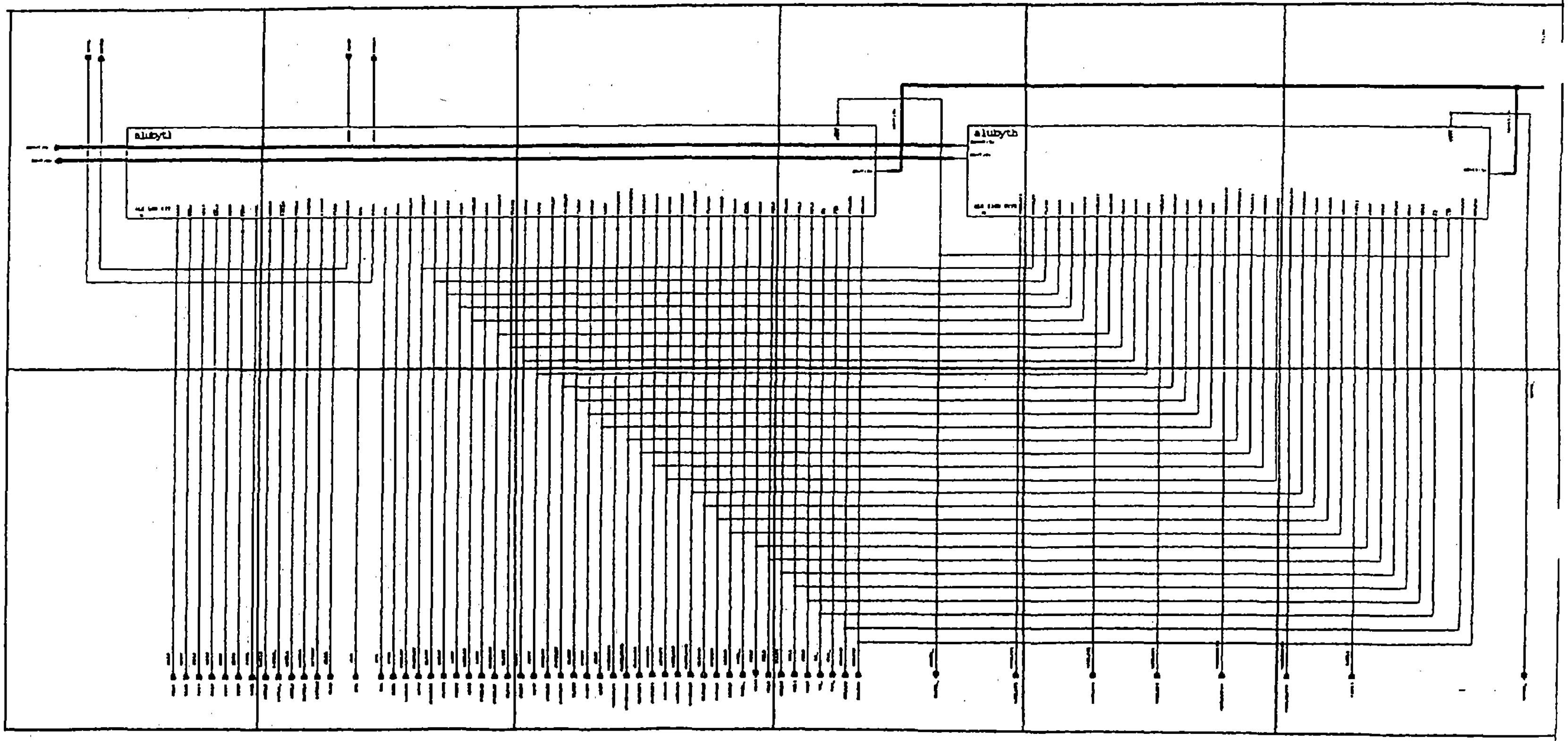


Fig. 7.09

MICRON
COMMUNICATIONS, INC
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

7.0901AA	7.0901AB	7.0901AC	7.0901AD	7.0901AE
7.0901BA	7.0901BB	7.0901BC	7.0901BD	7.0901BE
7.0901CA	7.0901CB	7.0901CC	7.0901CD	7.0901CE

Fig 7.0901

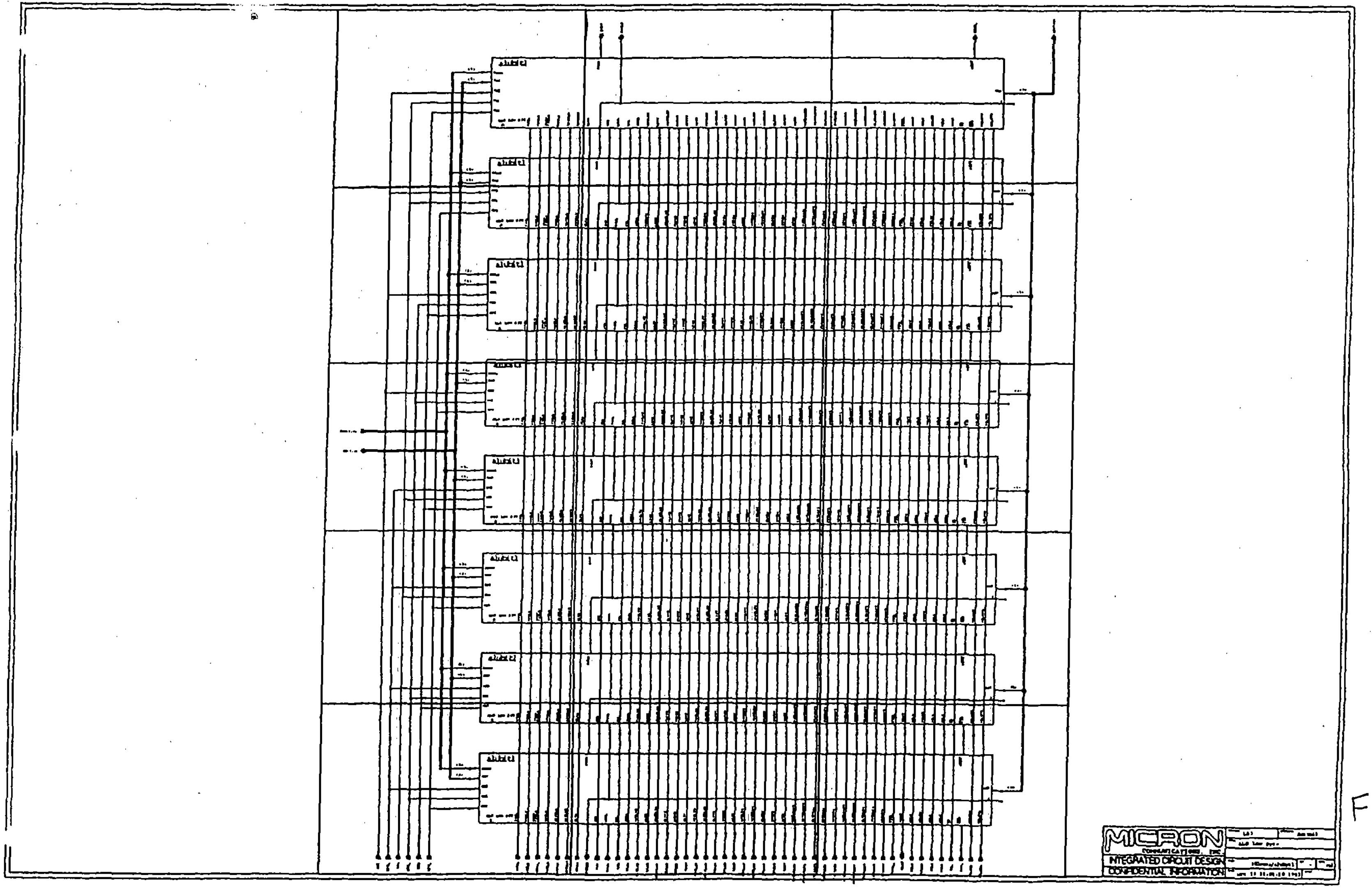
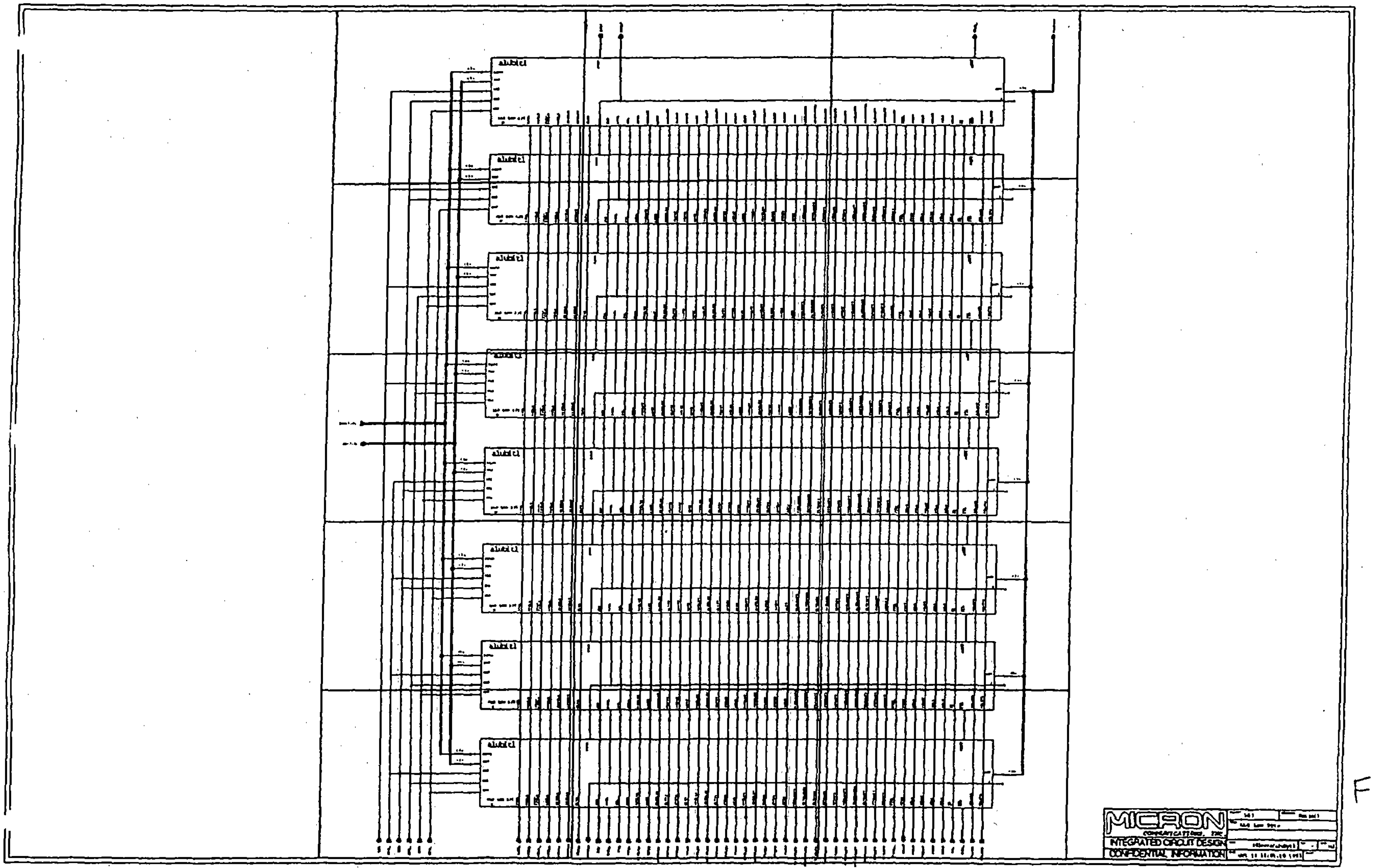

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

FIG. 7.0901


MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

F1G. 7.0901

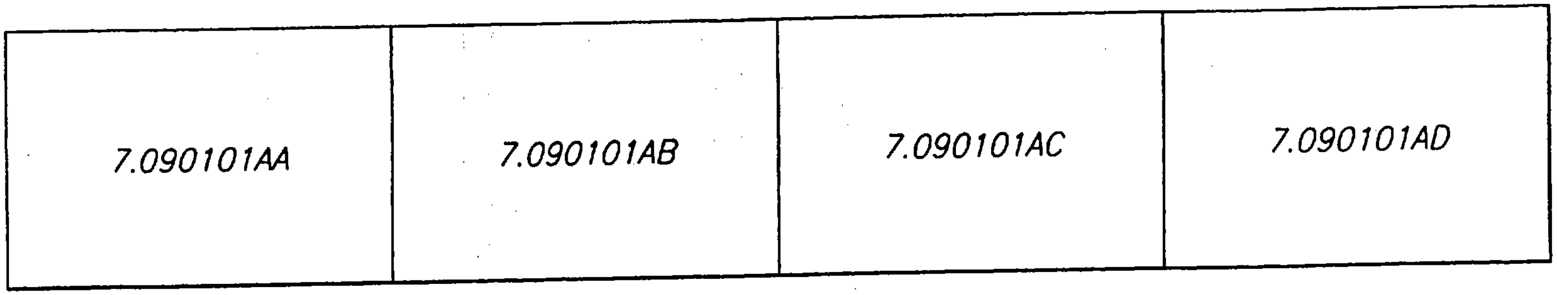


Fig 7.090101

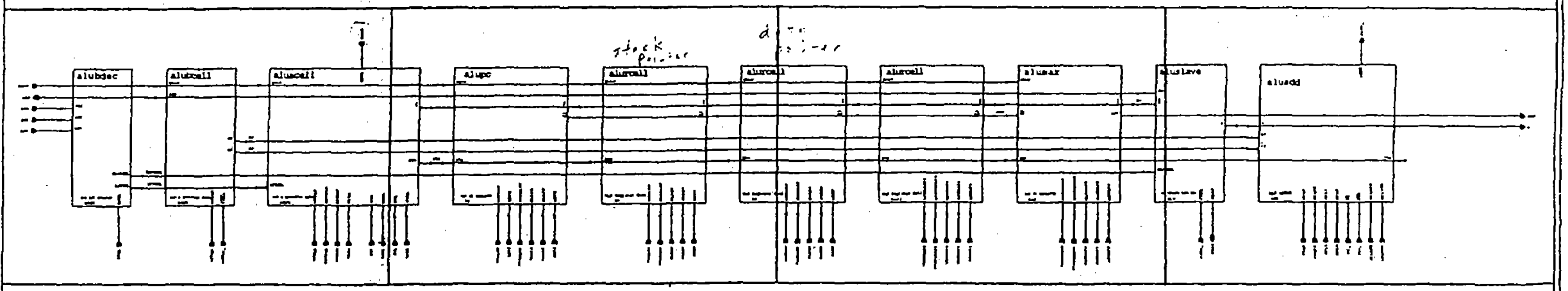


FIG. 7.090101

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

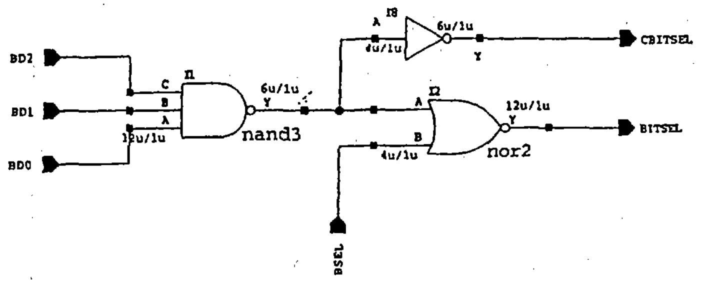


Fig. 7.09010101

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: ALU Bit Decoder Cell
NAME: 103reva/alubdec
REV: -
SIZE: A
DATE: Sep 29 16:07:43 1993
SHEET:

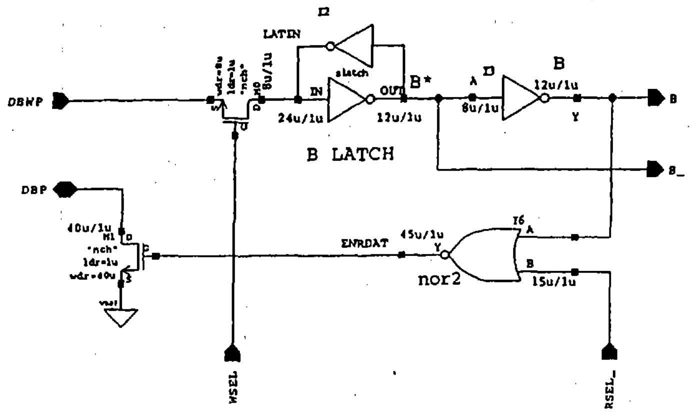


FIG. 7.09010102

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: Rotzoll
TITLE: ALU B Register Cell	
NAME: 103reva/alubcell	REV: - SIZE: A
DATE: Oct 1 15:32:35 1993	SHEET:

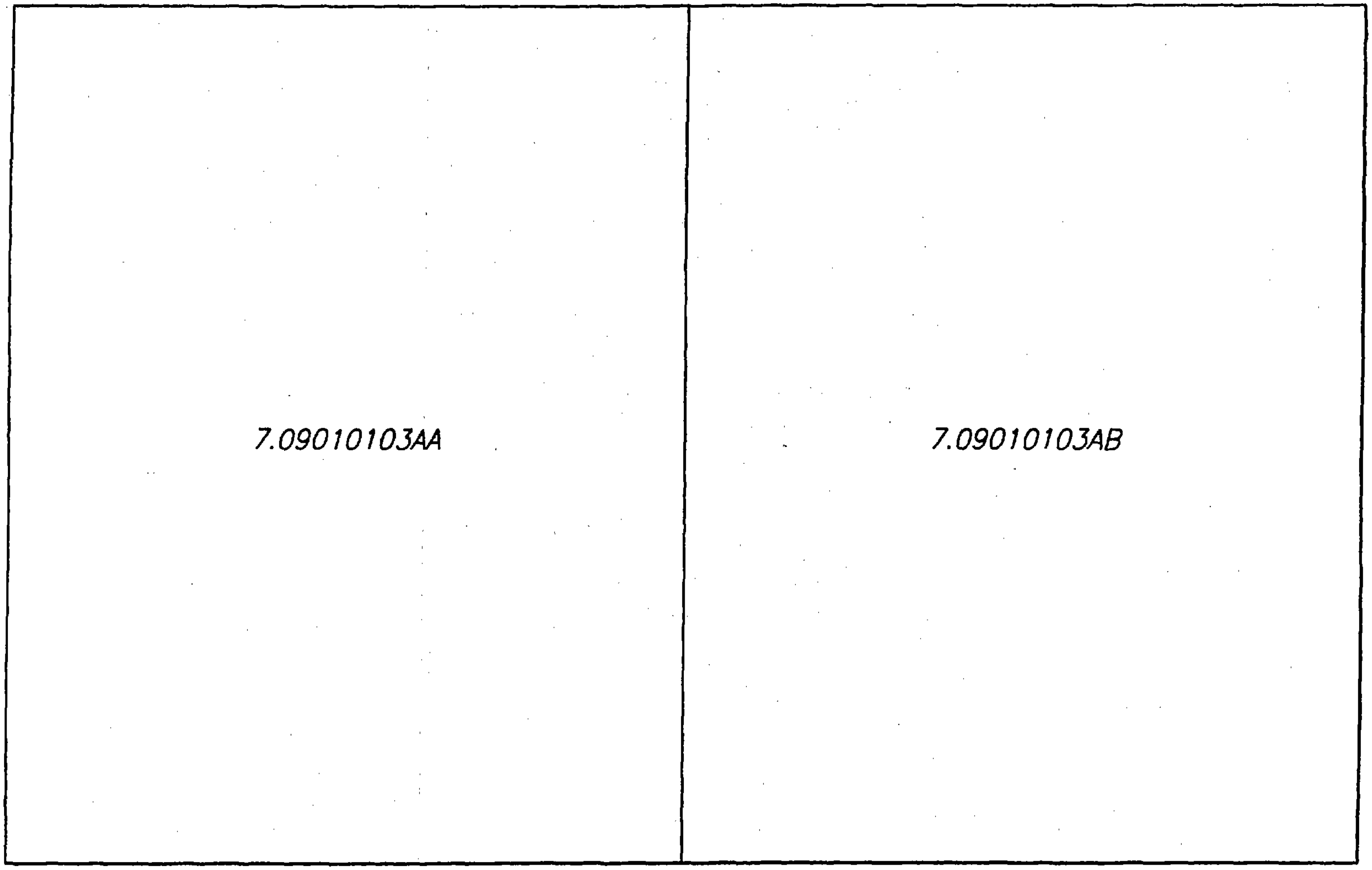
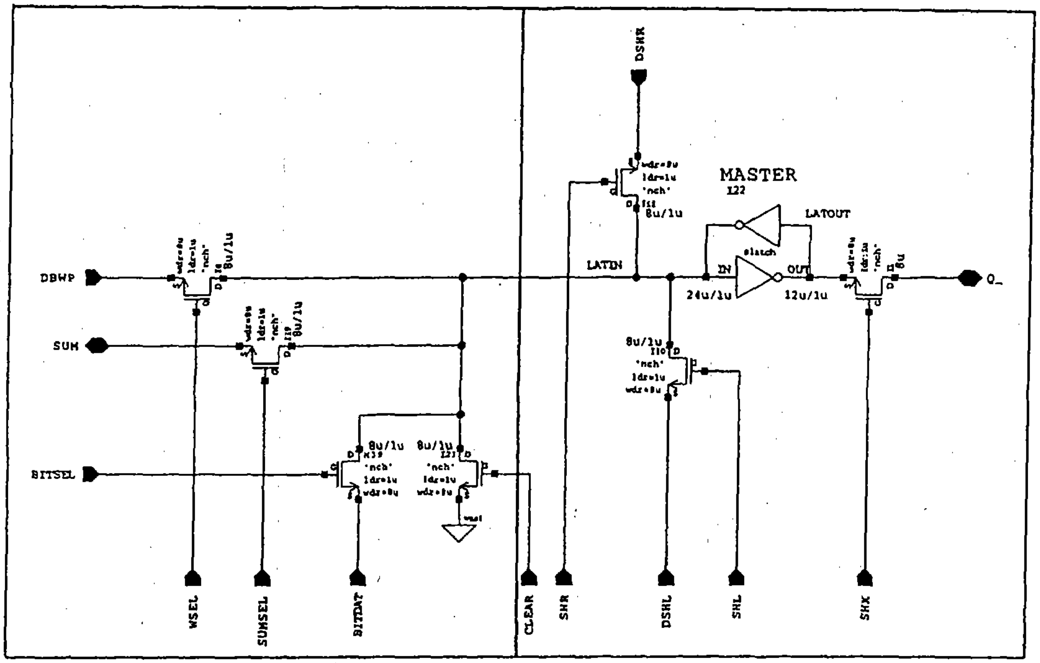


FIG 7.09010103



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: ALU A Register Cell
NAME: 103reva/aluacell
REV: -
STEP: A
DATE: Oct 1 15:41:37 1993
SHEET:

FIG. 7.09010103

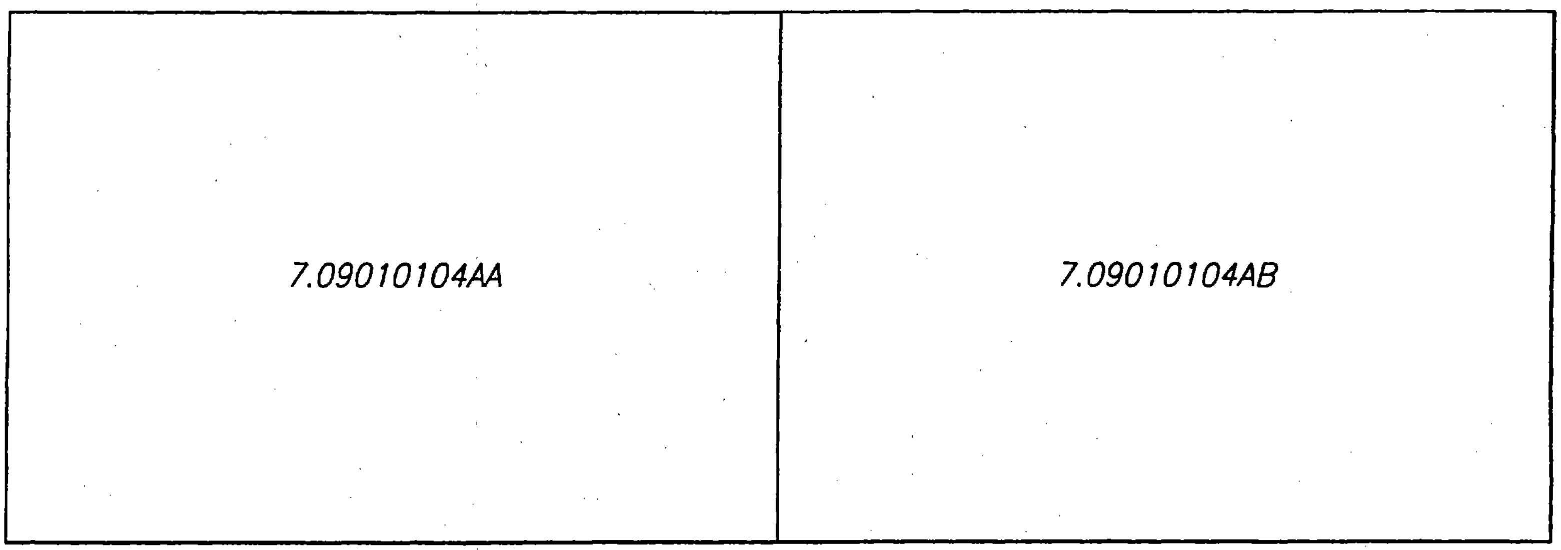
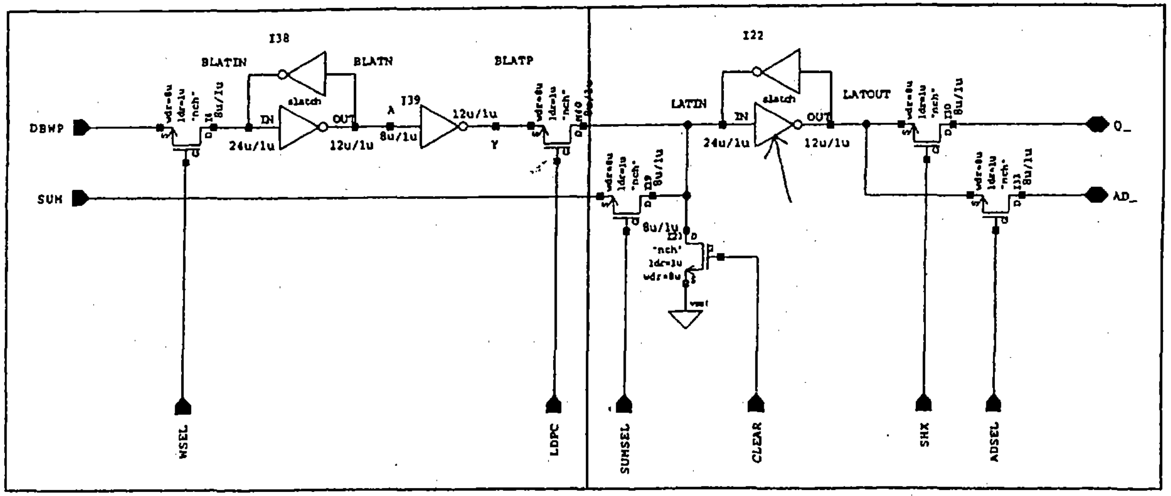


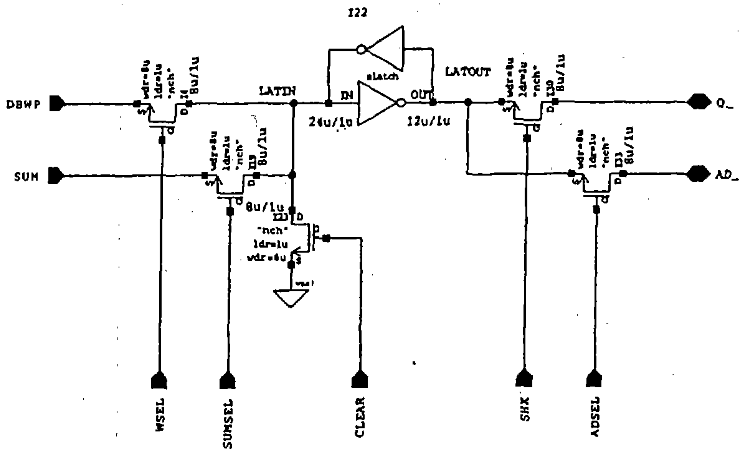
FIG 7.09010104

Fig. 7.09010104



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03			DESIGNER: Rotzoll		
TITLE: ALU Register Cell					
NAME: 103reva/alupc		REV: -		SIZE: A	
DATE: Oct 1 15:45:48 1993		SHEET:			



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: ALU Register Cell
NAME: 103reva/alurcell
REV: -
SIZE: A
DATE: Oct 1 15:51:03 1993
SHEET:

FIG. 7.09010105

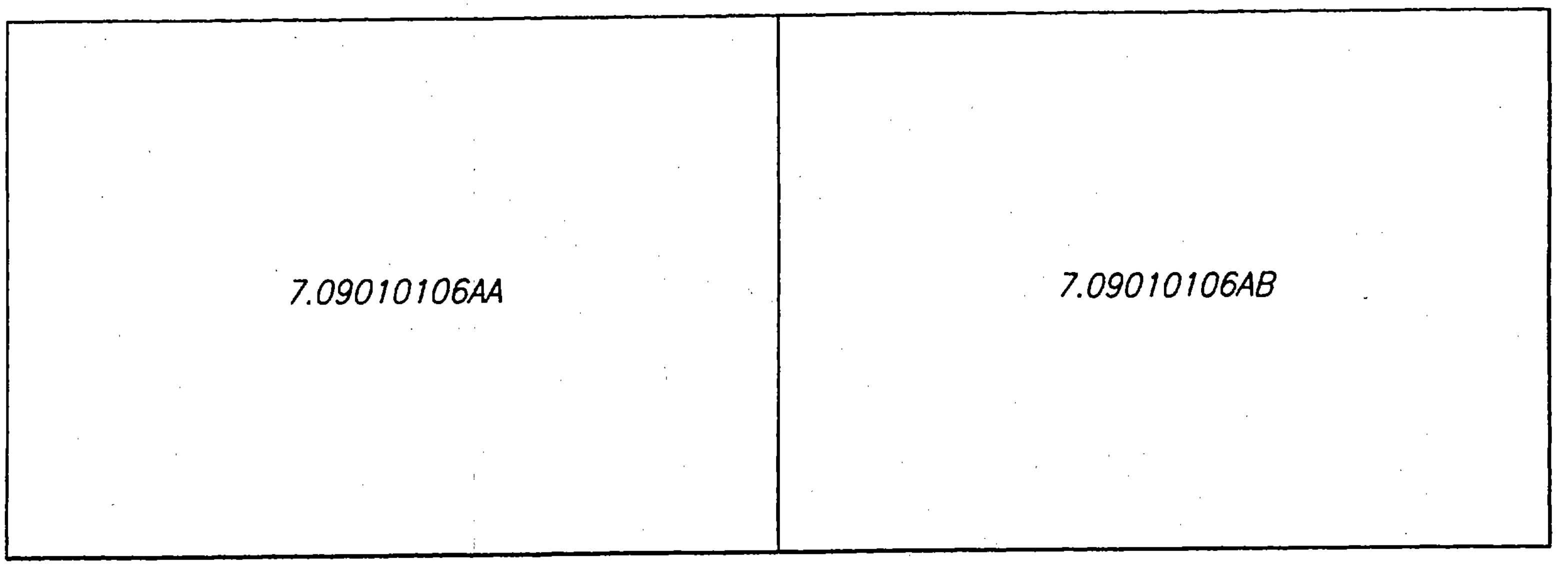
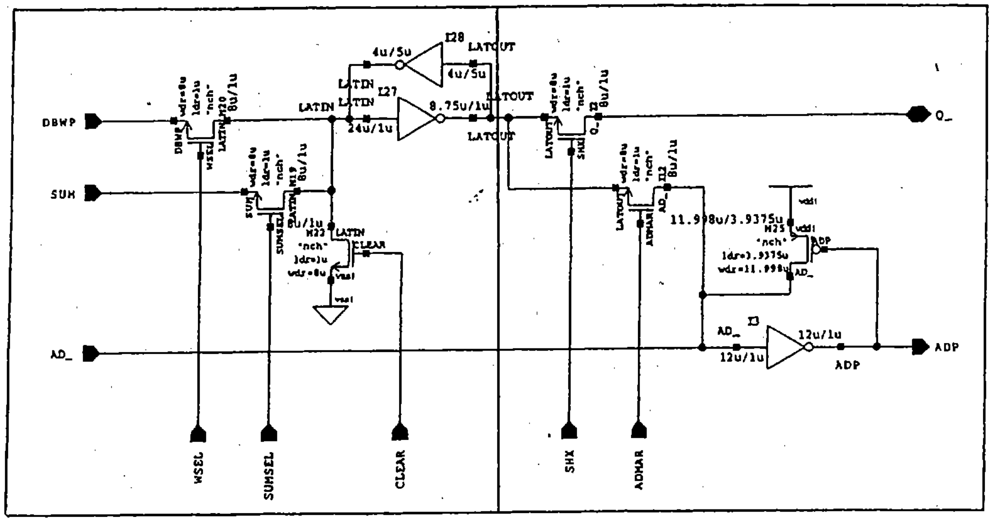


Fig 7.09010106

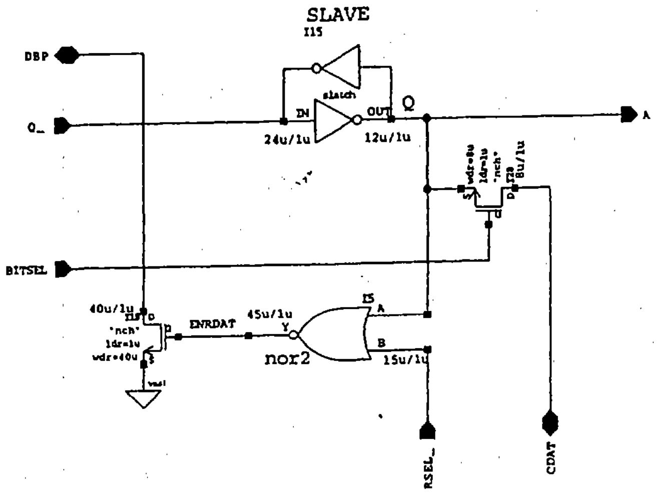


B8: added pch feedback device

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: ALU Memory Address Register
NAME: 103reva/alumar
REV: B8
SIZE: A
DATE: Jan 4 10:27:28 1996
SHEET:

FIG. 7.09010106



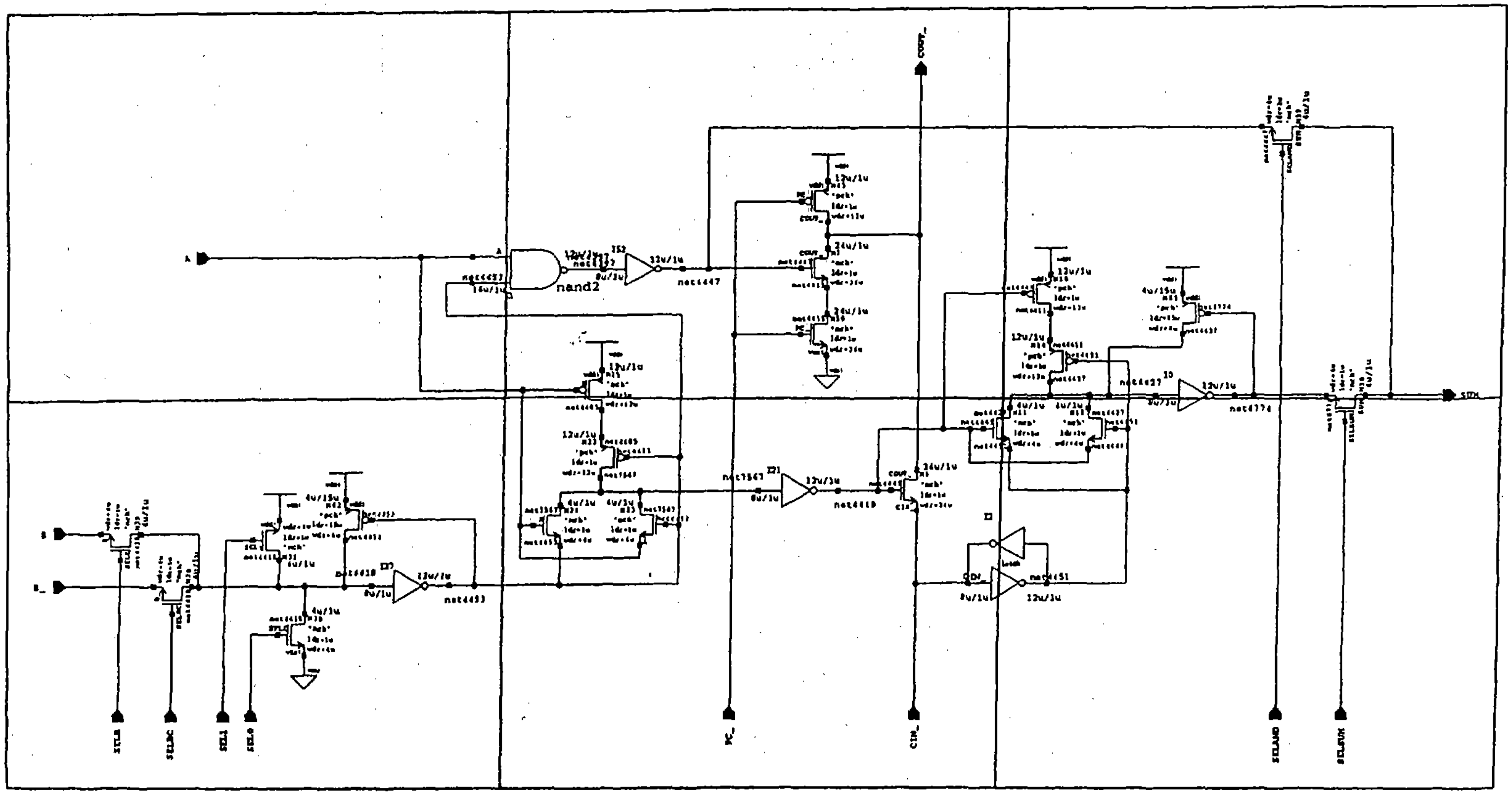
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: ALU Slave Cell
NAME: 103reva/aluslave
REV: -
SIZE: A
DATE: Sep 29 16:09:53 1993
SHEET:

FIG. 7.09010107

7.09010108AA	7.09010108AB	7.09010108AC
7.09010108BA	7.09010108BB	7.09010108BC

Fig 7.09010108



B5: move feedback device from I21 to I27

FIG. 7.09010108

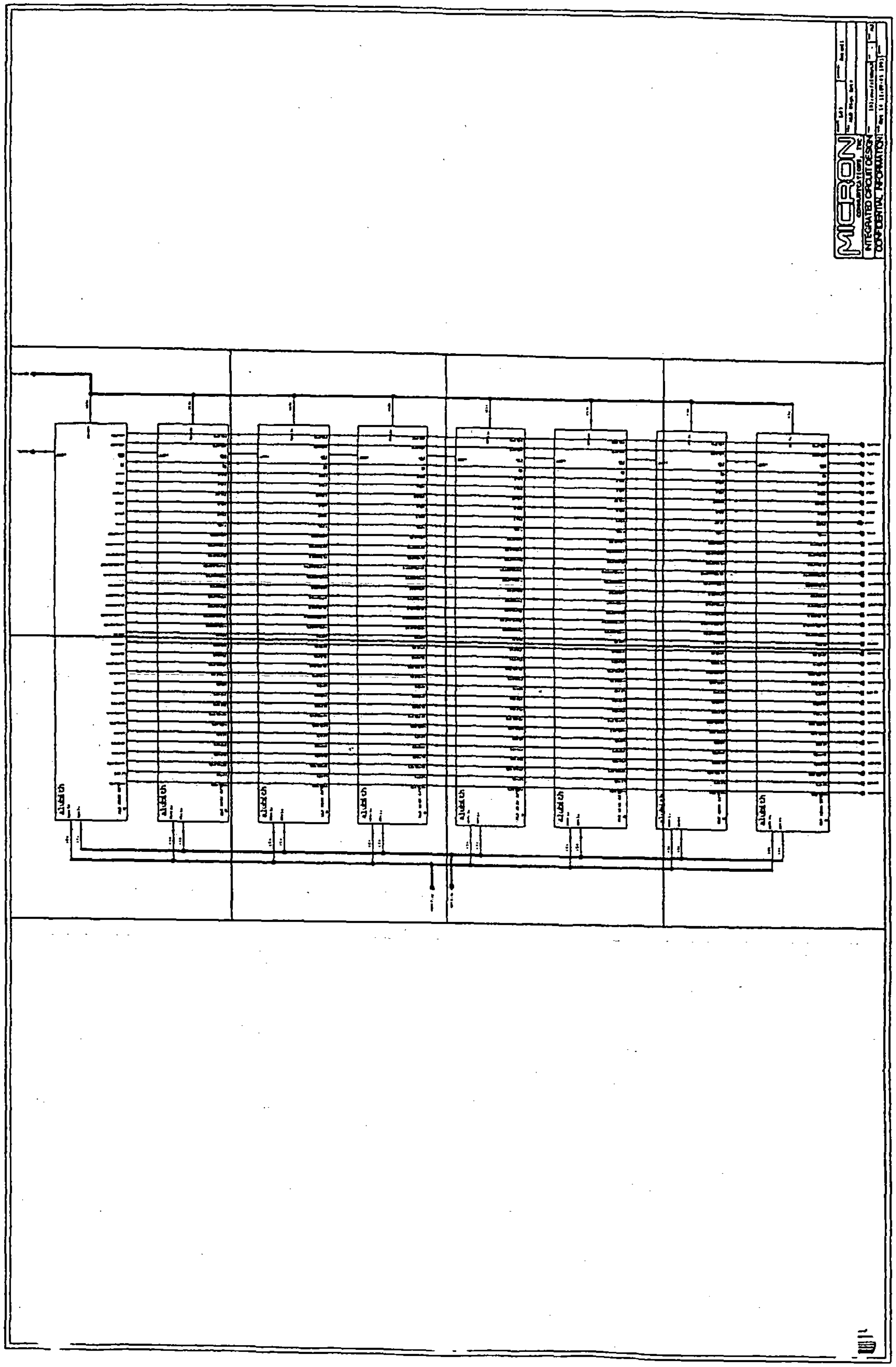
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: ALU Adder	
NAME: 103reva/aluadd	REV: B5
DATE: Sep 16 15:48:21 1995	SHEET:

7.0902AA	7.0902AB	7.0902AC	7.0902AD
7.0902BA	7.0902BB	7.0902BC	7.0902BD

Fig 7.0902

FIG. 7.0902


MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

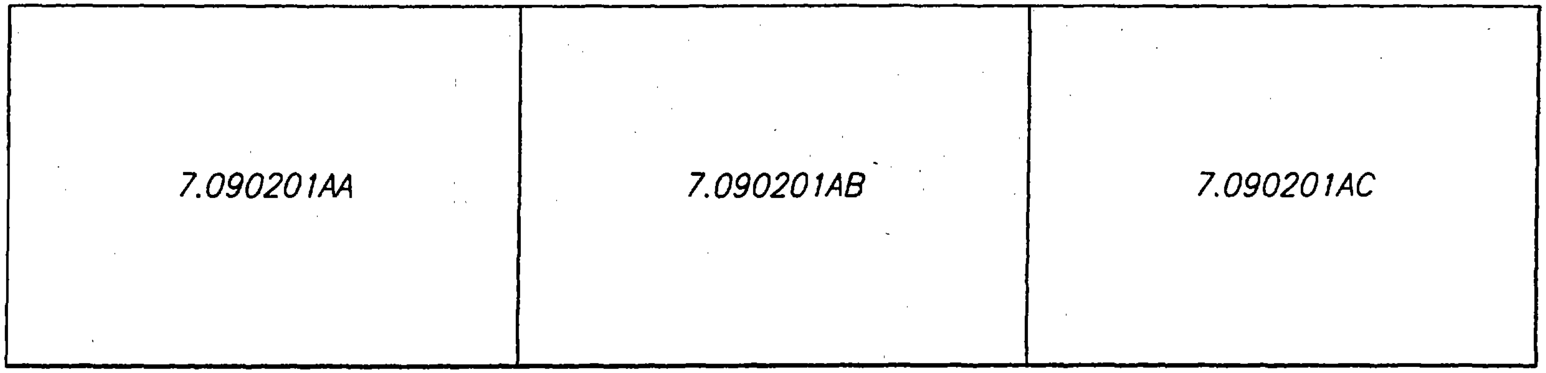


Fig 7.090201

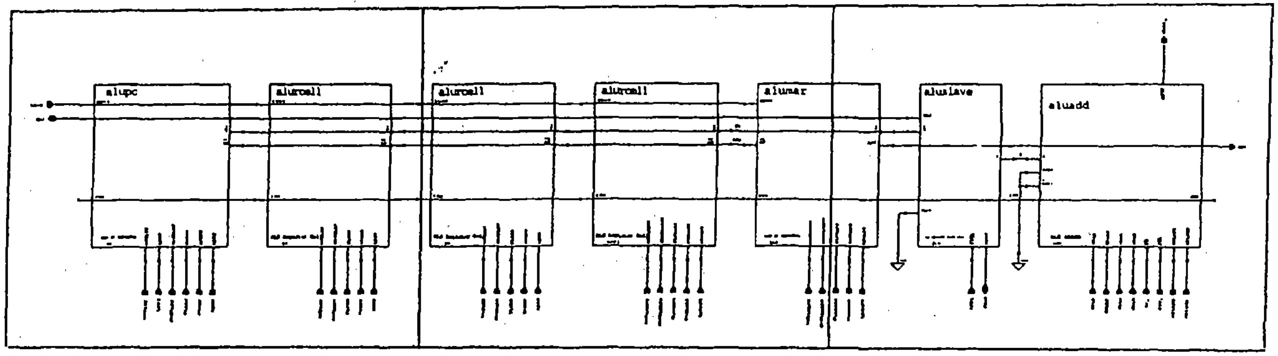


FIG. 7.090201

MICRON COMMUNICATIONS, INC
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

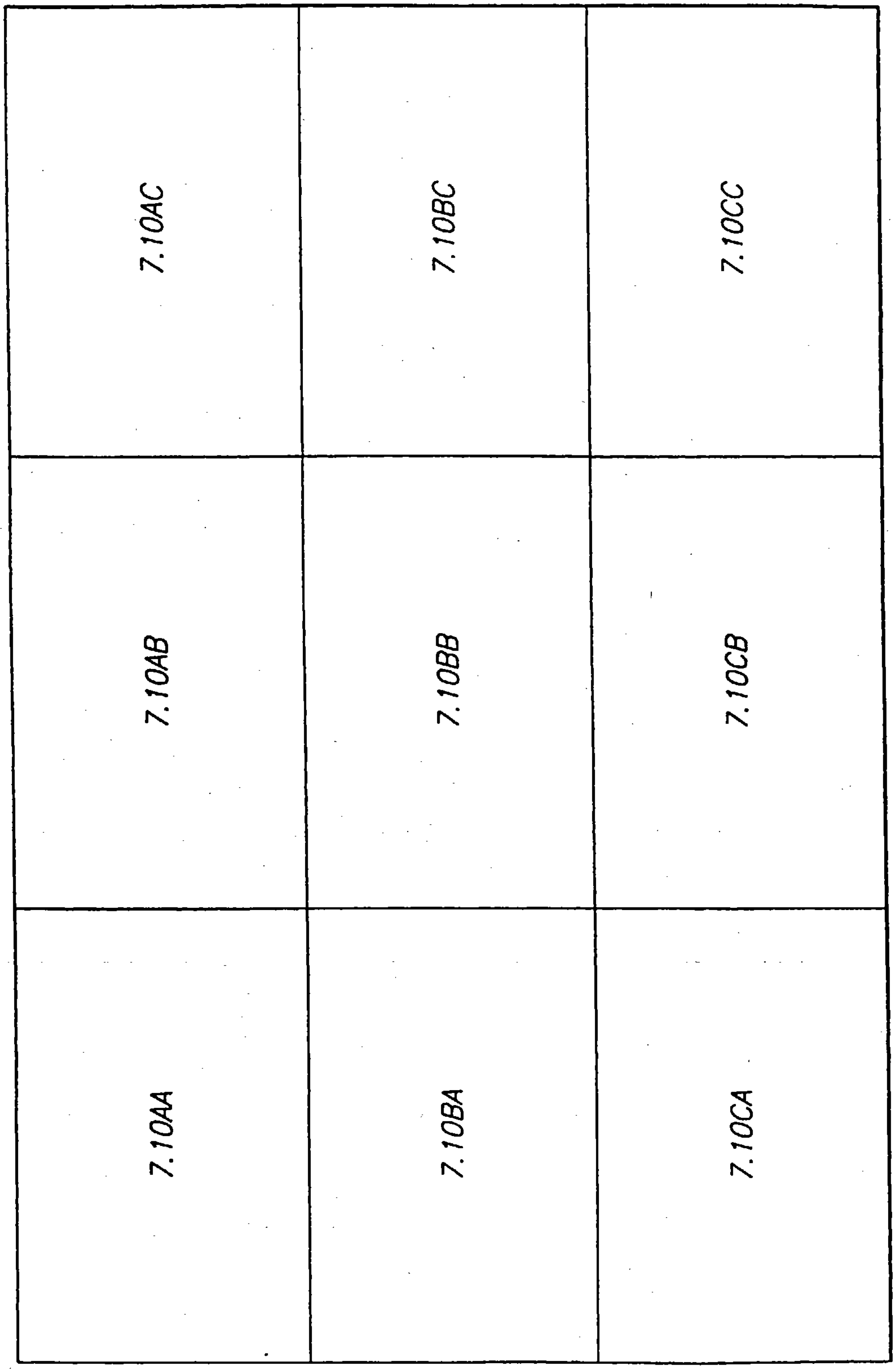


FIG. 7.10

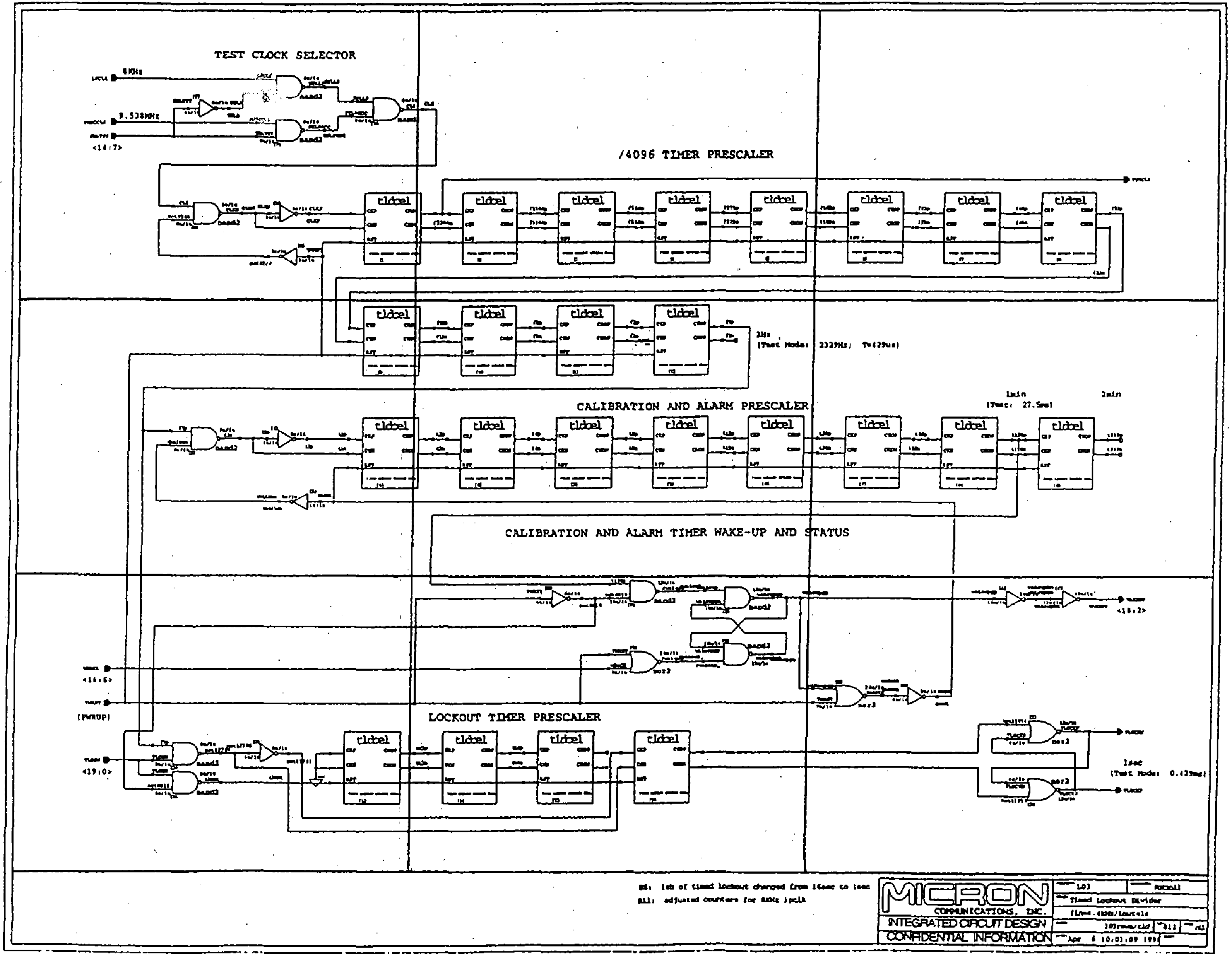
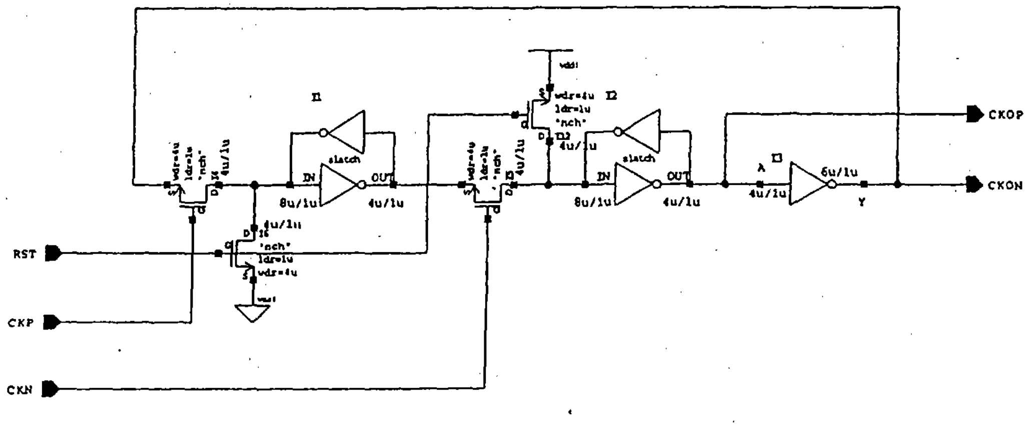

TEST CLOCK SELECTOR
8KHz
9.538MHz
<14:7>
nand2
/4096 TIMER PRESCALER
tldcel
1Hz
(Test Mode: 2329Hz; T=429us)
CALIBRATION AND ALARM PRESCALER
1min
(Test: 27.5ms)
2min
CALIBRATION AND ALARM TIMER WAKE-UP AND STATUS
<18:2>
<16:6>
(PWRUP)
nor2
LOCKOUT TIMER PRESCALER
<19:0>
1sec
(Test Mode: 0.429ms)
B8: lsb of timed lockout changed from 16sec to 1sec
B11: adjusted counters for 8KHz ipclk
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
Timed Lockout Divider
B11
Apr 6 10:01:09 199

FIG. 7.10



12/29/92

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: Rotzoll
TITLE: Timed Lockout Divider Cell	
NAME: 103reva/tldcel	REV: SIZE: A
DATE: Sep 22 15:26:56 1994	SHEET:

FIG. 7.1001

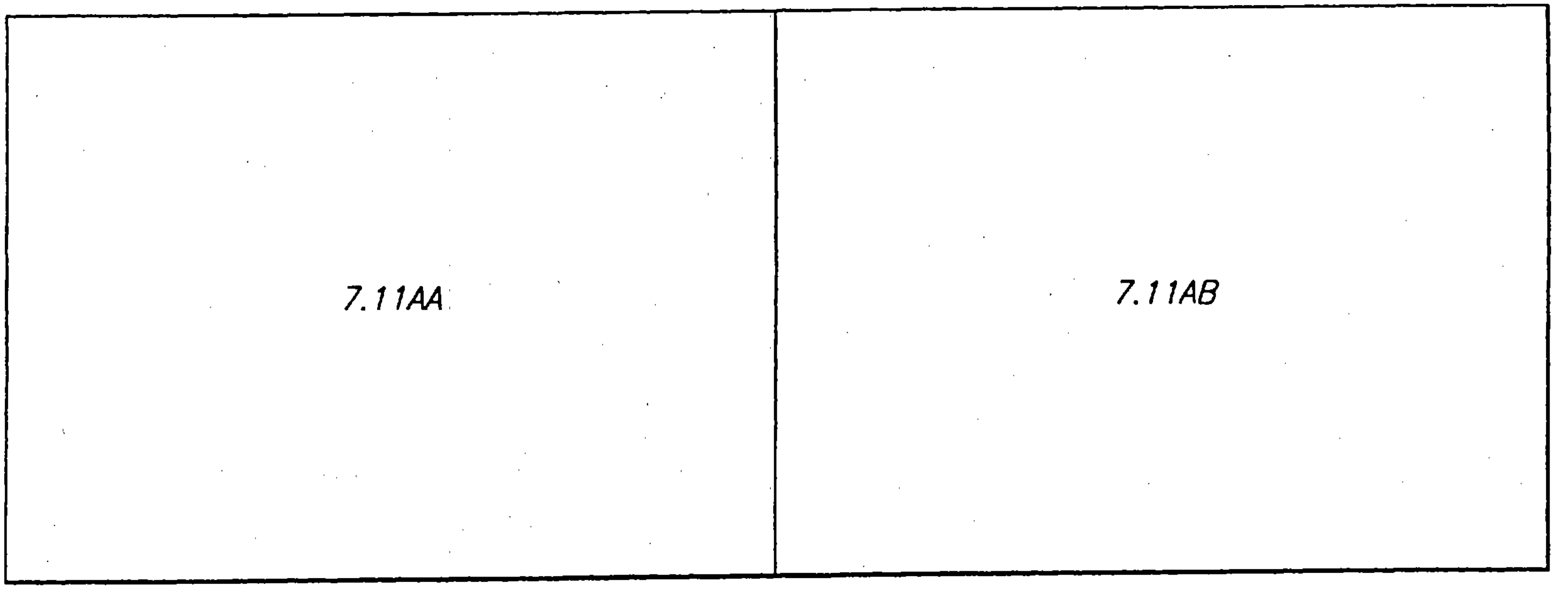


Fig 7.11

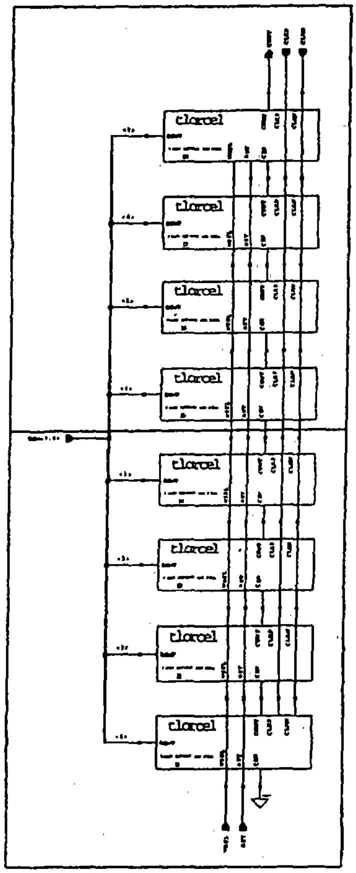


FIG. 7.11

MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
Rocall
Timed Lockout Register
10)teva/tloreg
Oct 1 13:05:37 199

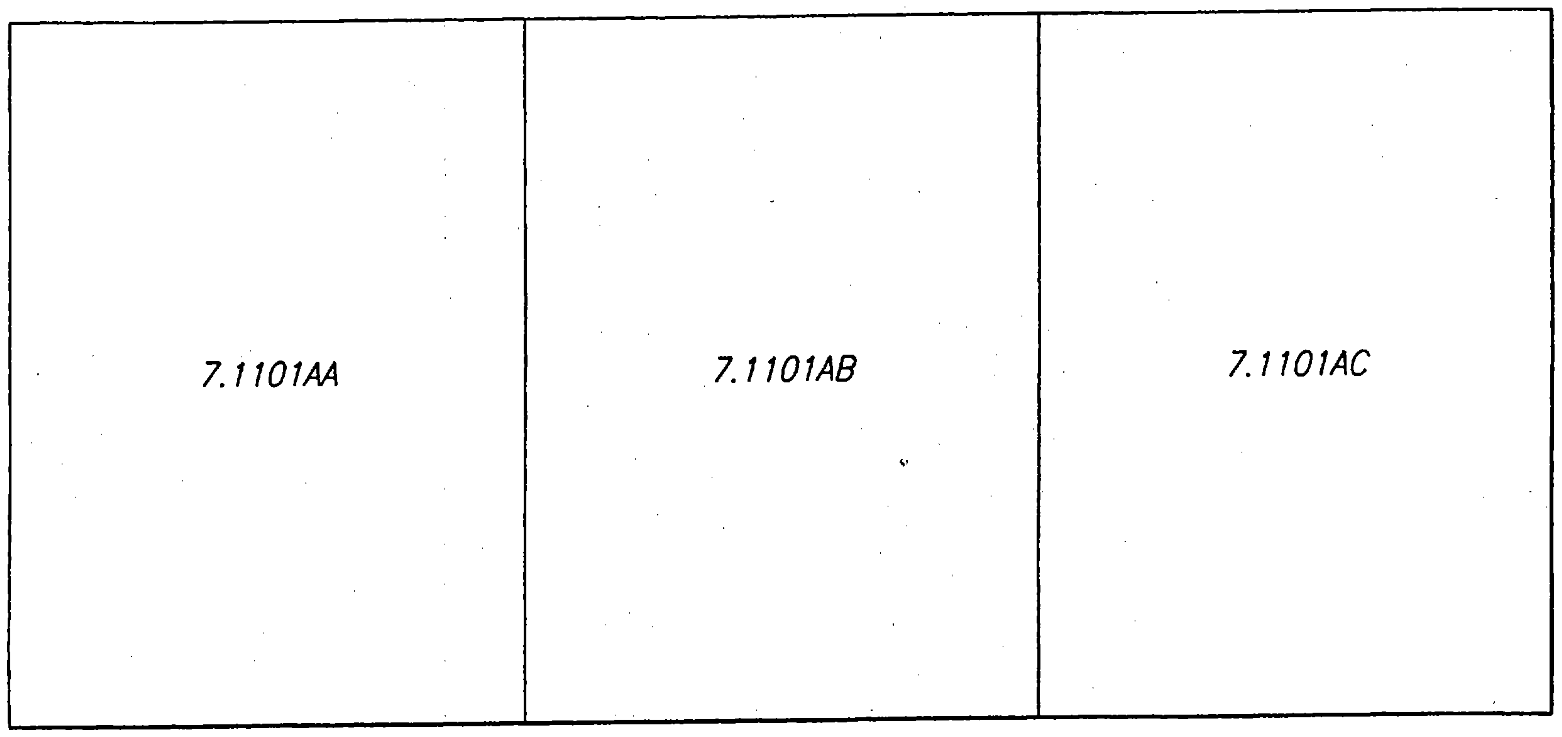
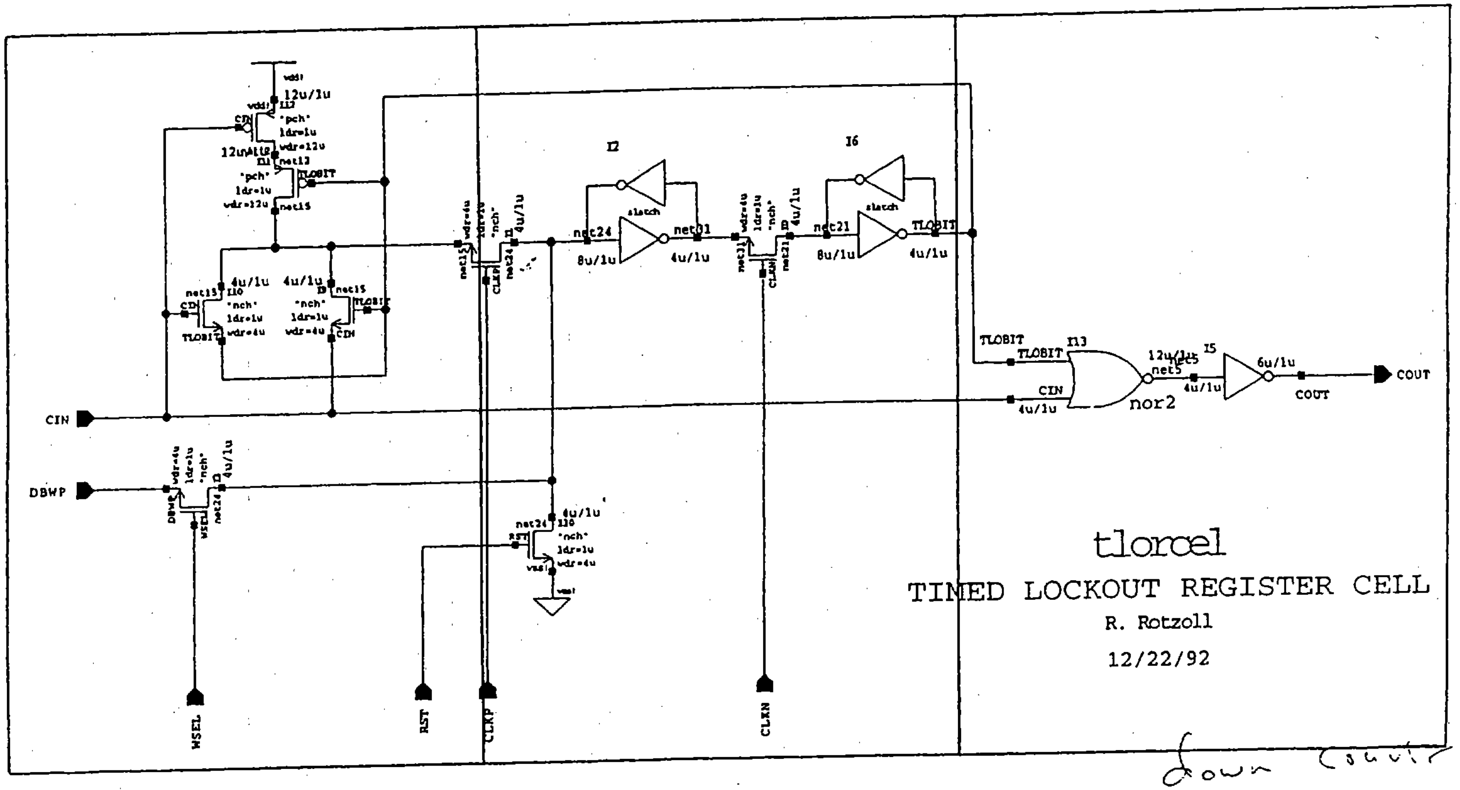


Fig 7.1101



tlorcel

TIMED LOCKOUT REGISTER CELL

R. Rotzoll

12/22/92

down counter

FIG. 7.1101

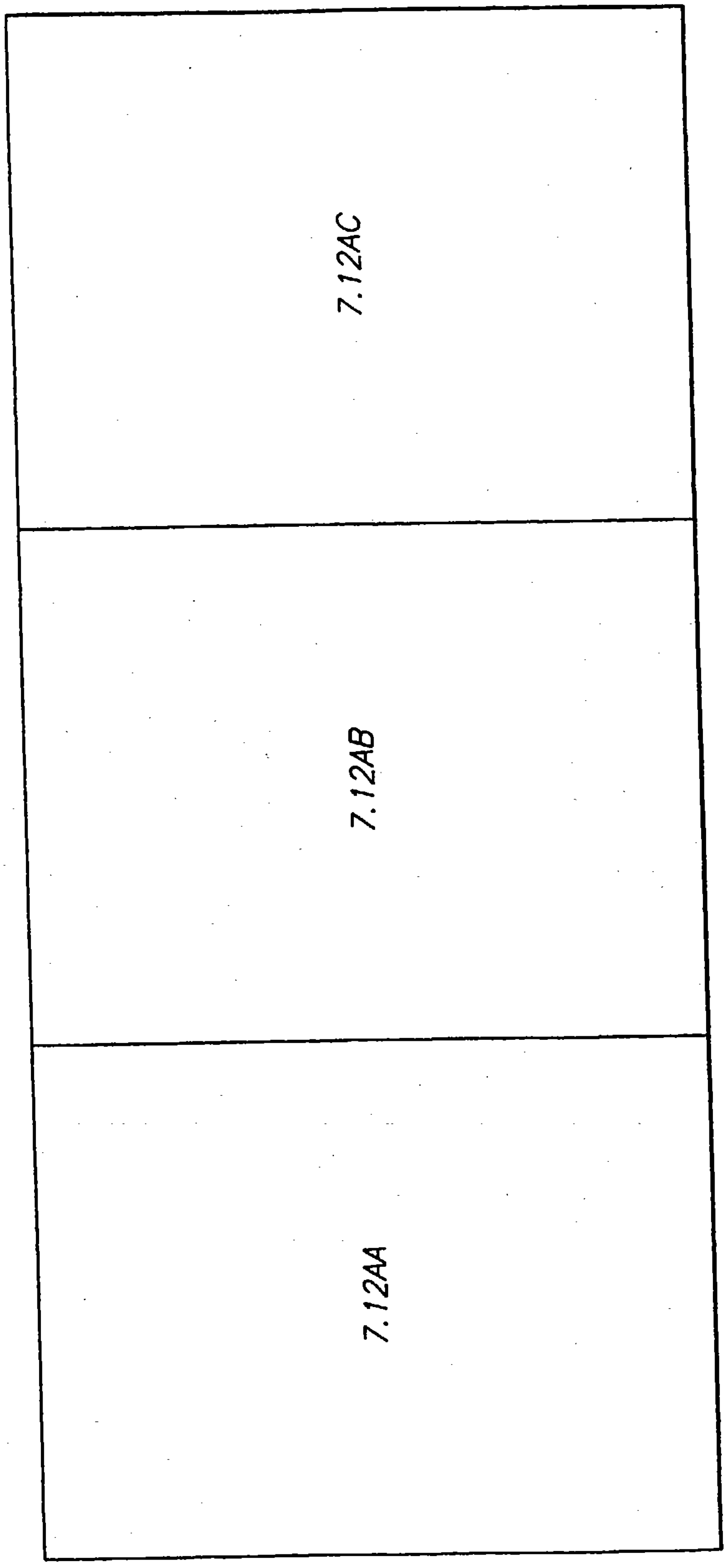


Fig. 7.12

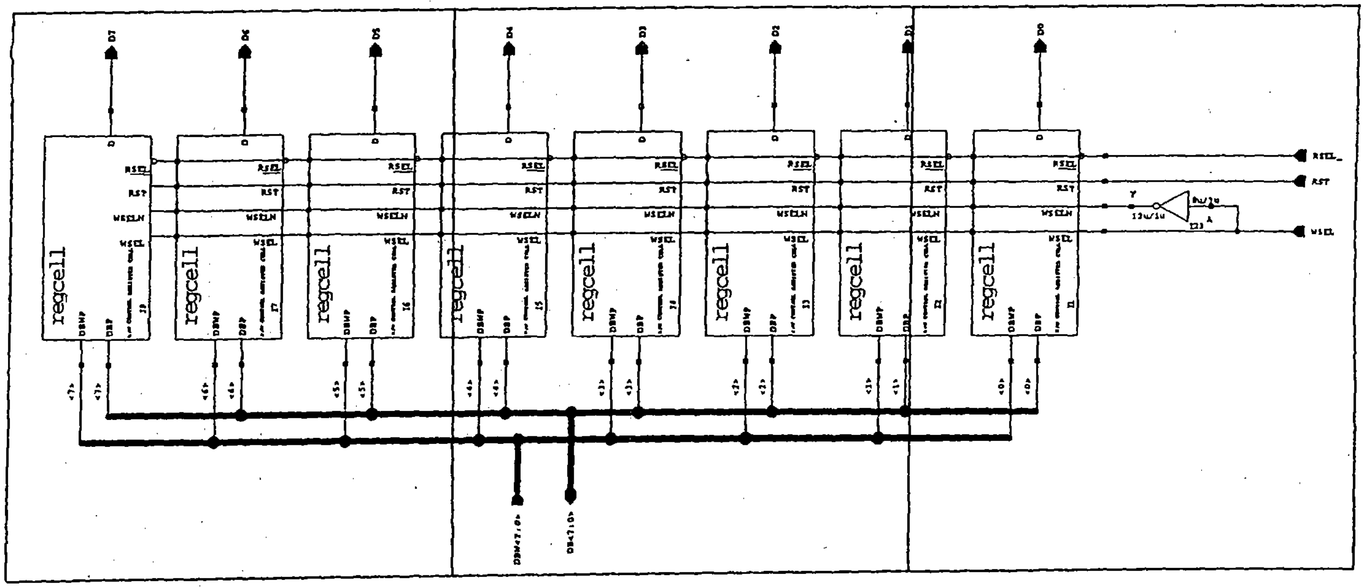
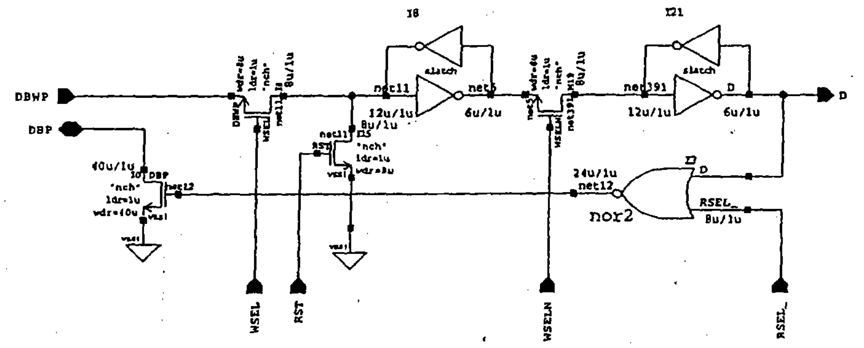


Fig. 7.12

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
Rotzoll
R/W Control Register
103reva/oreg
-
nil
Nov 12 09:44:40 1993



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03		DESIGNER: Rotzoll	
TITLE: R/W Control Register Cell			
NAME: 103reva/regcell		REV: -	SIZE: A
DATE: Nov 12 09:41:36 1993		SHEET:	

FIG. 7.1201

MI40-030

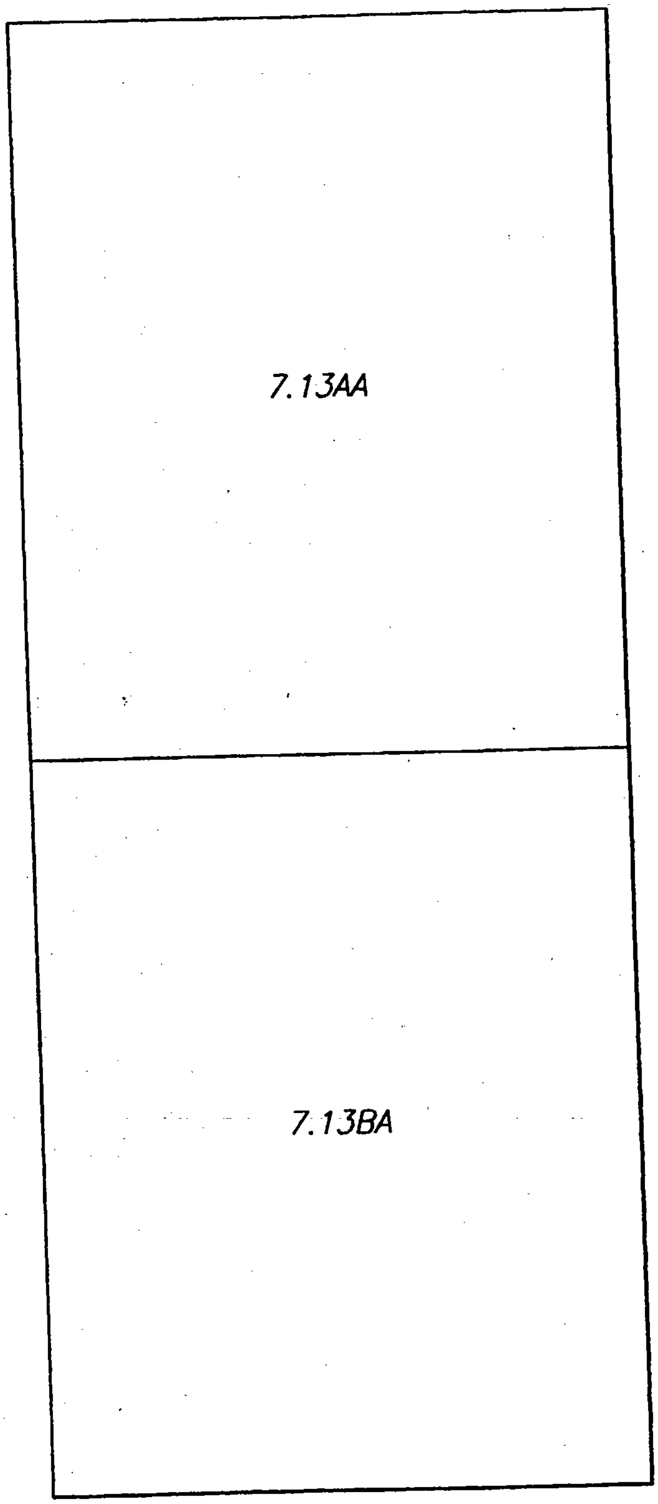
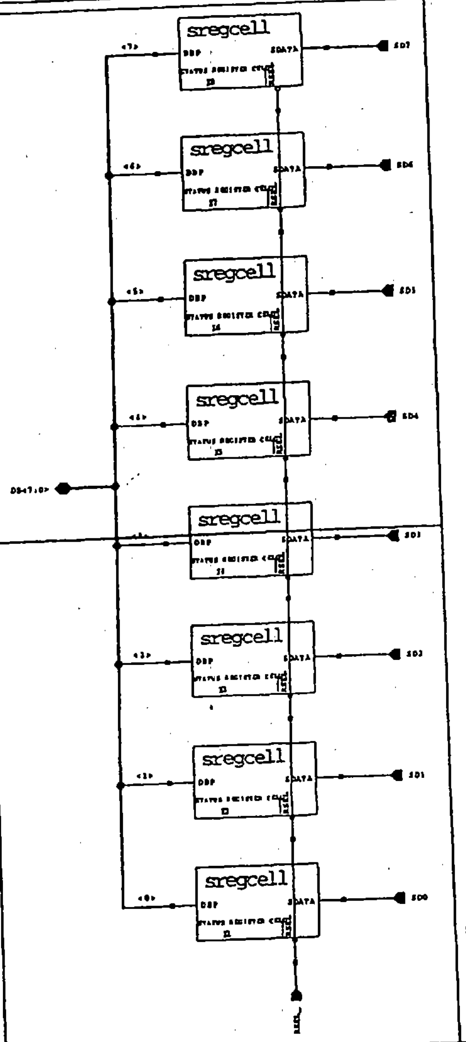


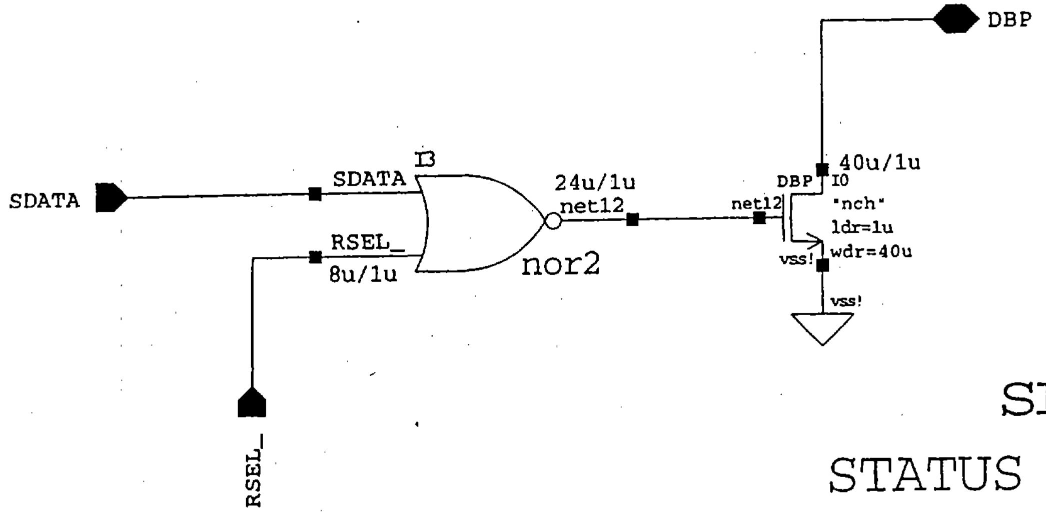
FIG 7.13



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotroll
TITLE: Status Register
NAME: 103reva/sreg
REV: -
DATE: Oct 1 14:49:00 1993

FIG. 7.13



sregcell

STATUS REGISTER CELL

R. Rotzoll

12/8/92

FIG. 7.1301

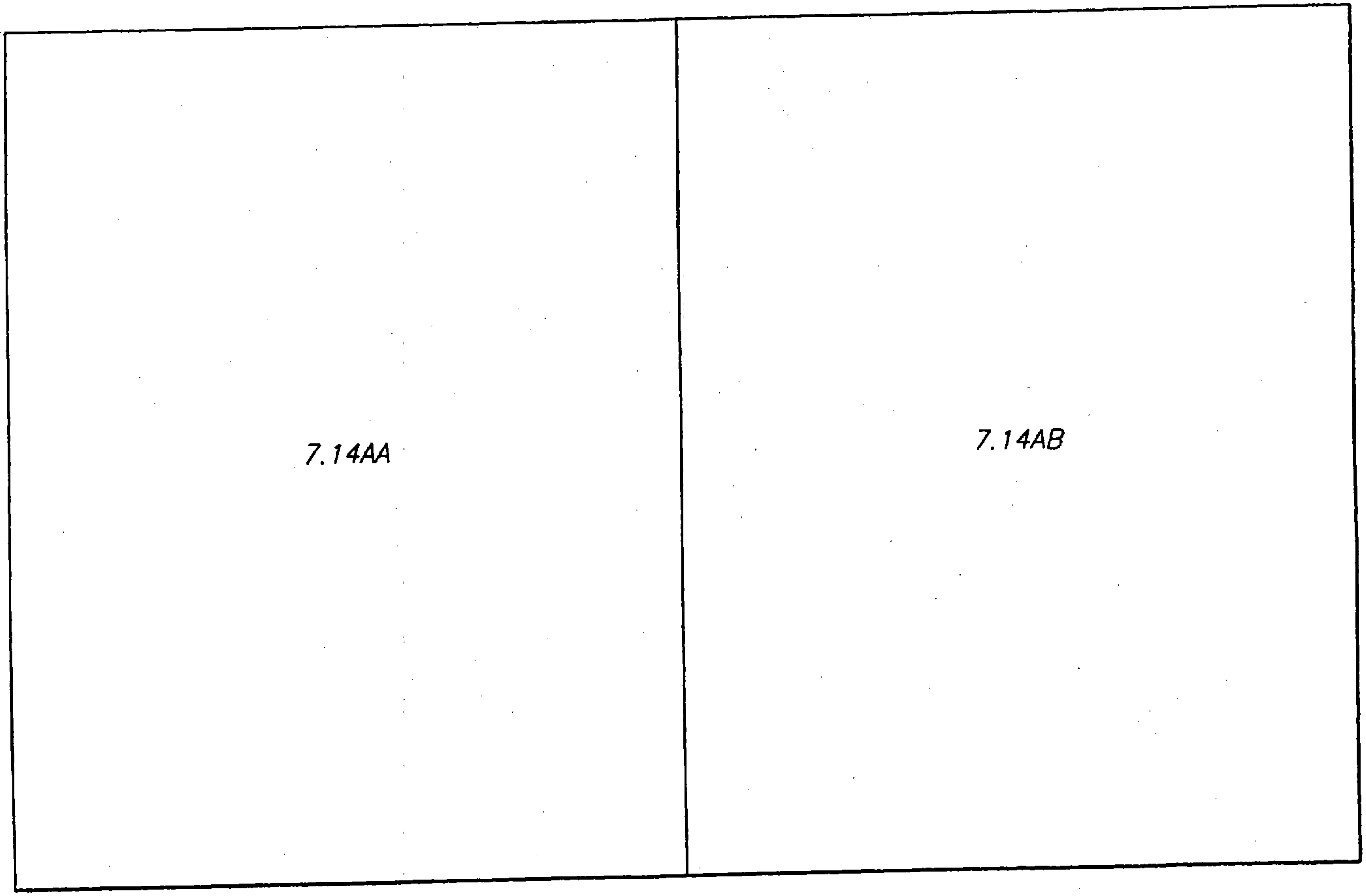
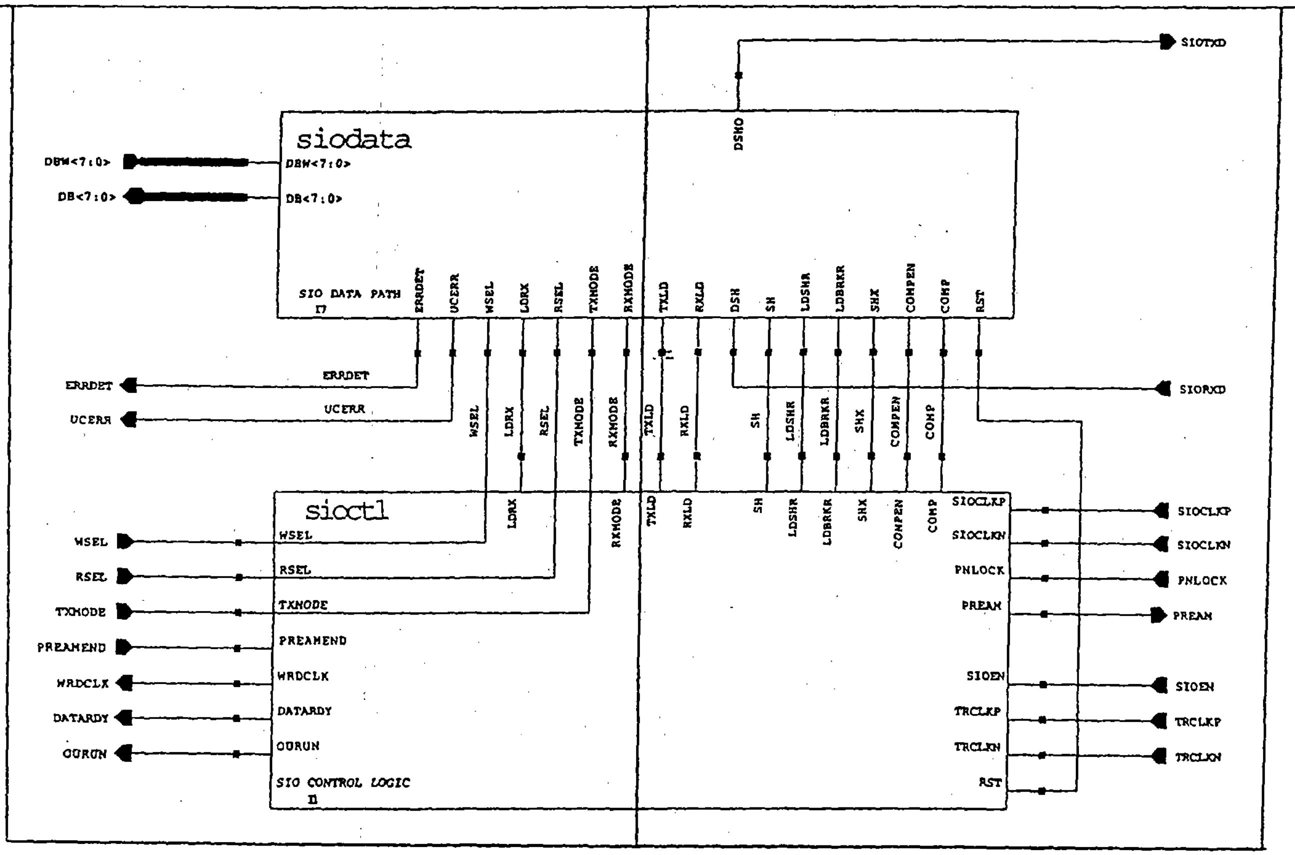


FIG. 7.14



B8: deleted BRKREN
B11: added non-overlapping clocks

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

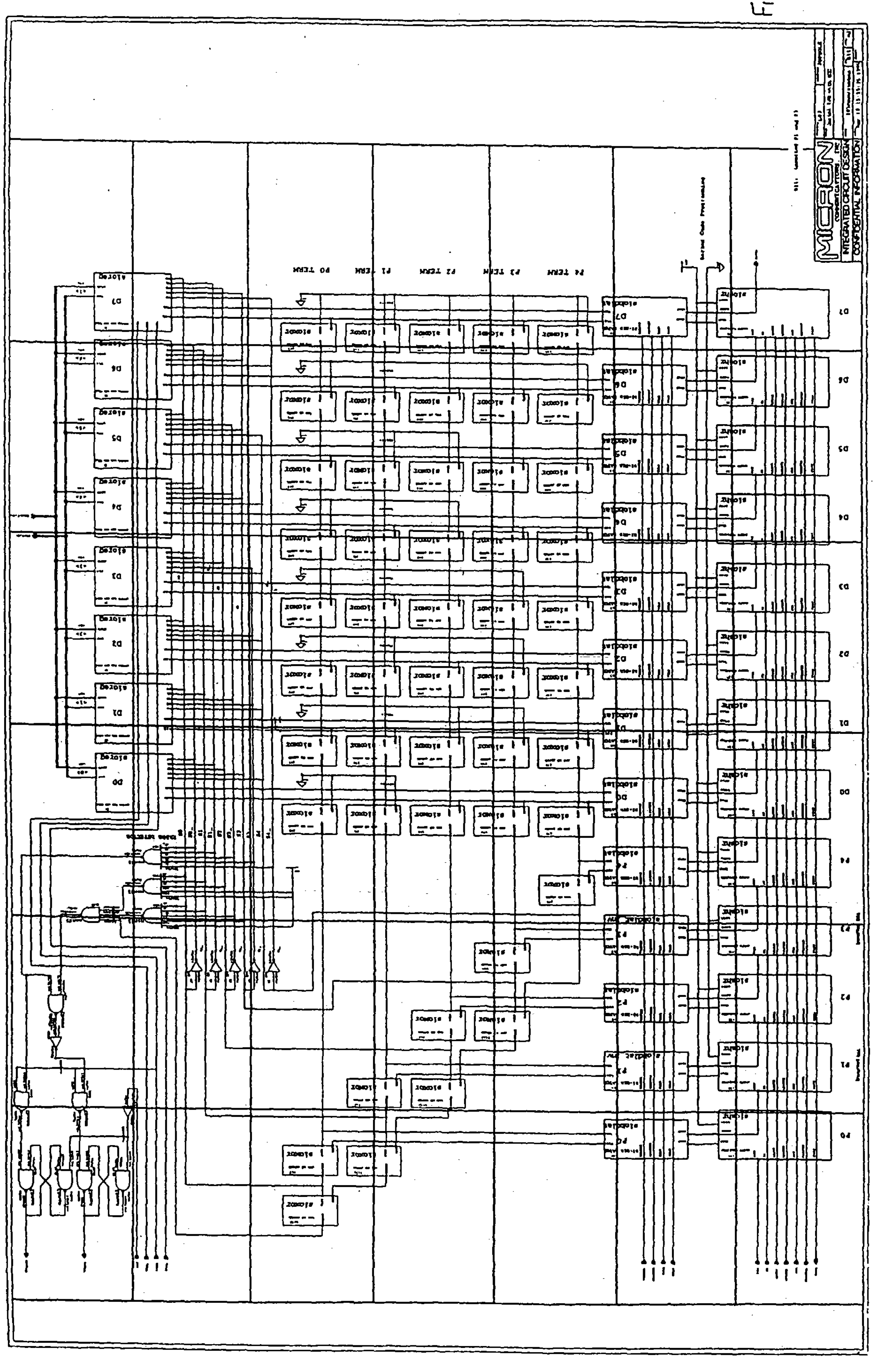
PROJECT: L03
DESIGNER: Rotzoll
TITLE: Serial I/O
Serial/Block Enc/Dec
NAME: 103reva/sio
REV: B11
SIZE: A
DATE: Apr 4 10:16:14 1996
SHEET:

FIG. 7.14

7.1401AA	7.1401AB	7.1401AC	7.1401AD	7.1401AE	7.1401AF
7.1401BA	7.1401BB	7.1401BC	7.1401BD	7.1401BE	7.1401BF
7.1401CA	7.1401CB	7.1401CC	7.1401CD	7.1401CE	7.1401CF
7.1401DA	7.1401DB	7.1401DC	7.1401DD	7.1401DE	7.1401DF
7.1401EA	7.1401EB	7.1401EC	7.1401ED	7.1401EE	7.1401EF
7.1401FA	7.1401FB	7.1401FC	7.1401FD	7.1401FE	7.1401FF
7.1401GA	7.1401GB	7.1401GC	7.1401GD	7.1401GE	7.1401GF

Fig. 7.1401

Fig. 7.1401


P0 TERM
P1 TERM
P2 TERM
P3 TERM
P4 TERM
D0
D1
D2
D3
D4
D5
D6
D7
P0
P1
P2
P3
P4
MICRON
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

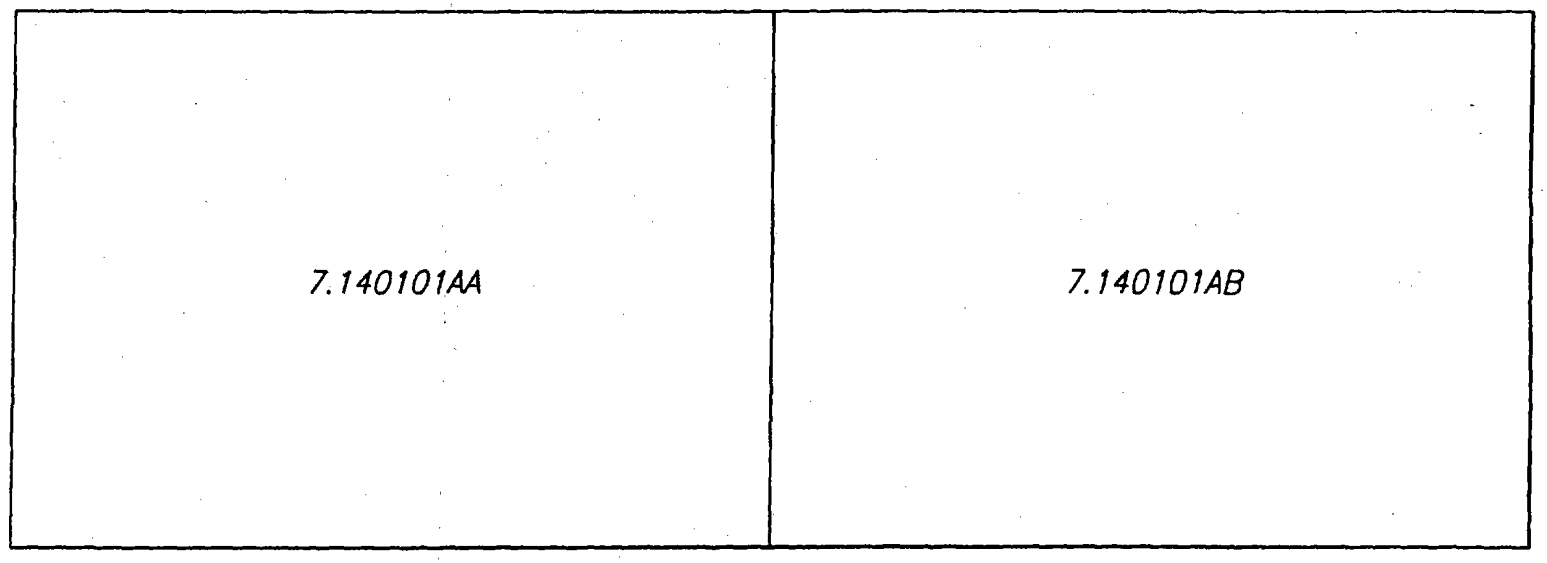
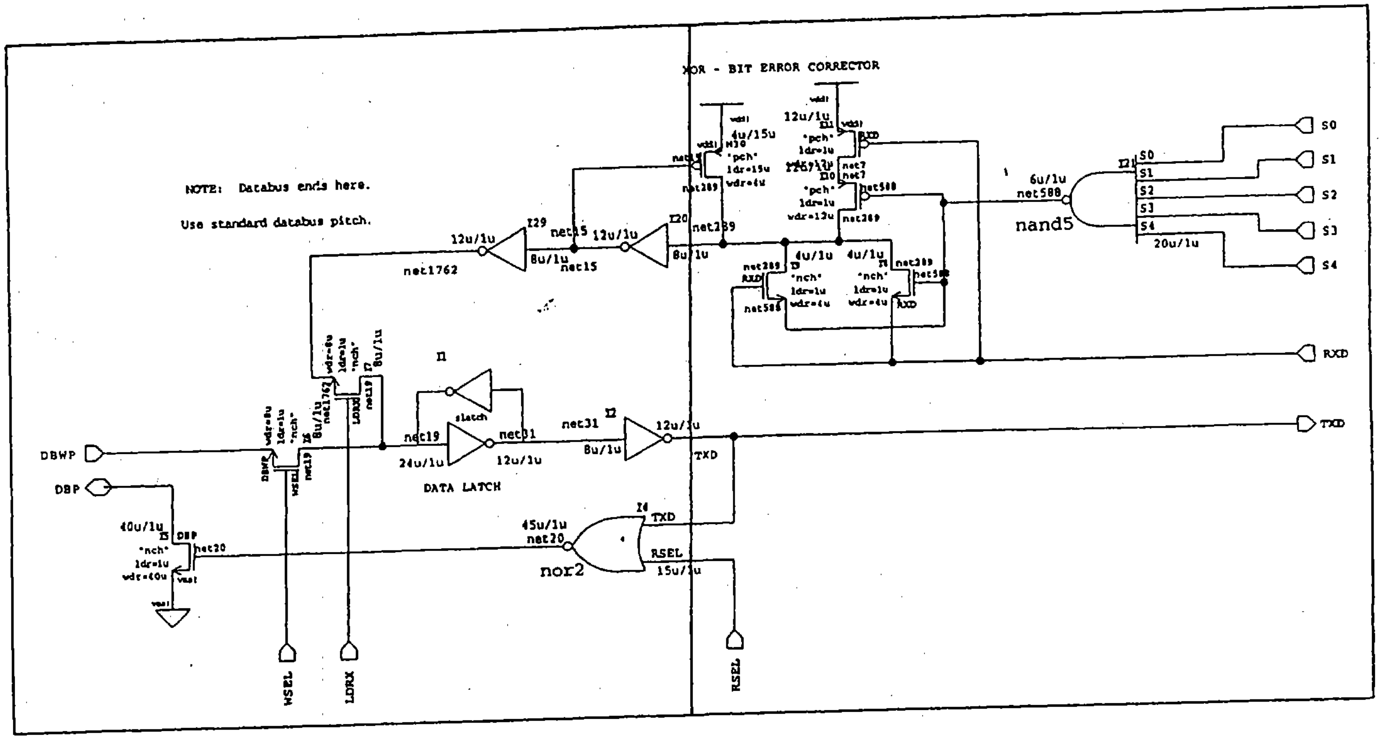


FIG 7.140101



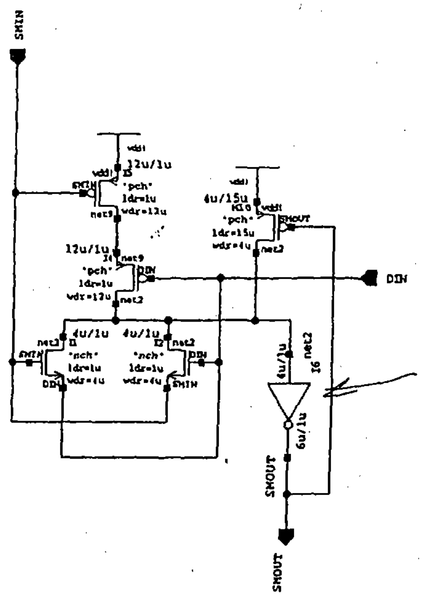
NOTE: Databus ends here.

Use standard databus pitch.

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: Serial I/O Register Cell
NAME: 103reva/sioreg
REV: B1
SIZE: A
DATE: Sep 1 18:03:52 1994
SHEET:

FIG. 7.140101



too small!
to drive b&lot

FIG. 7.140102

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: SIO XOR
NAME: 103reva/sioxor
REV: B1
SIZE: A
DATE: Sep 1 18:07:22 1994
SHEET:

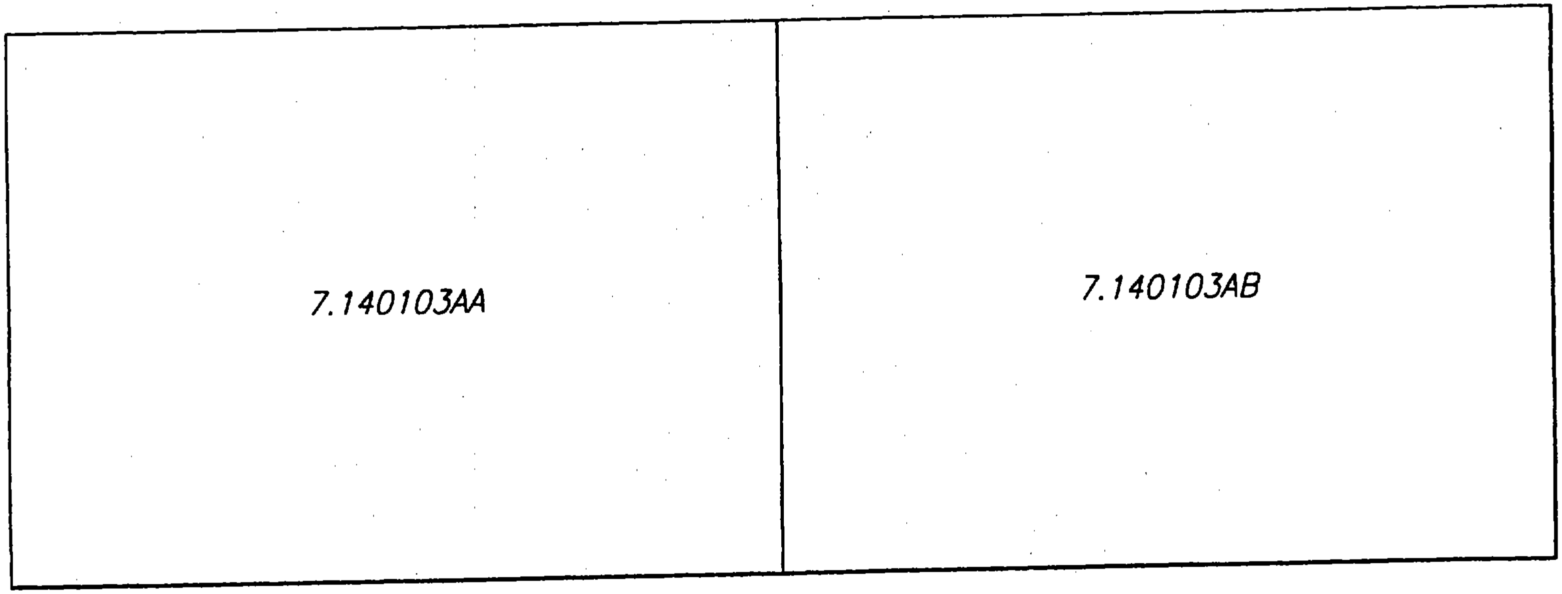
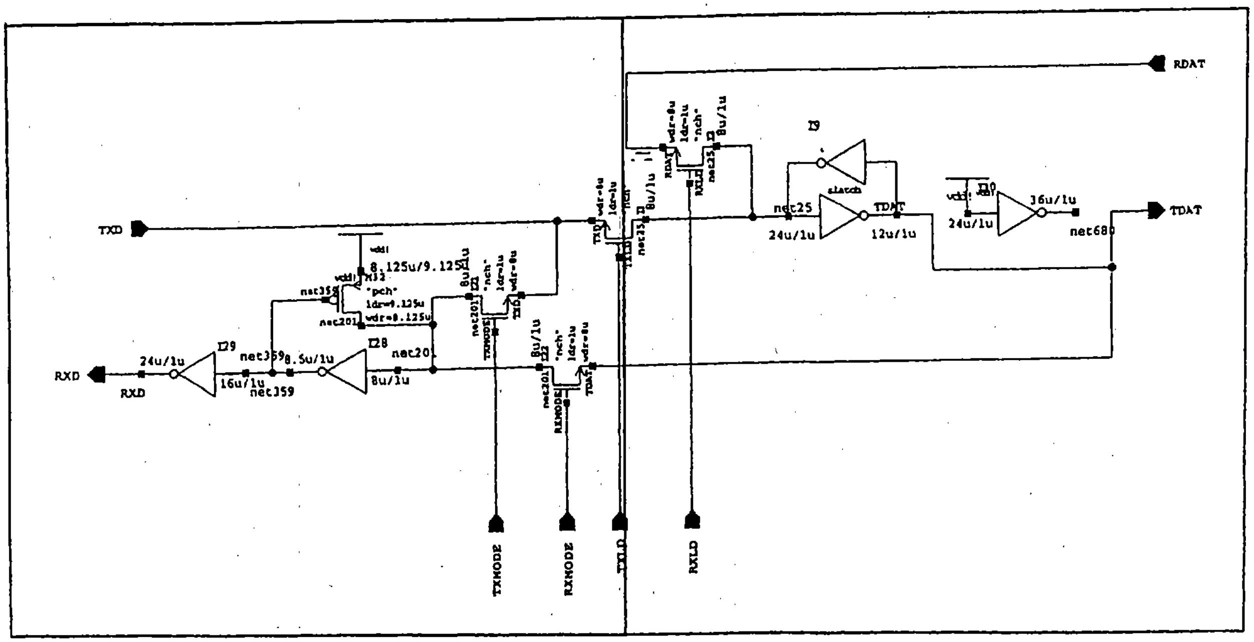


FIG 7.140103



B11: inverted bit

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: SIO Bidirectional Latch
NAME: 103reva/siobdlat_inv
REV: B11
SIZE: A
DATE: Apr 10 15:13:59 1996
SHEET:

FIG. 7.140103

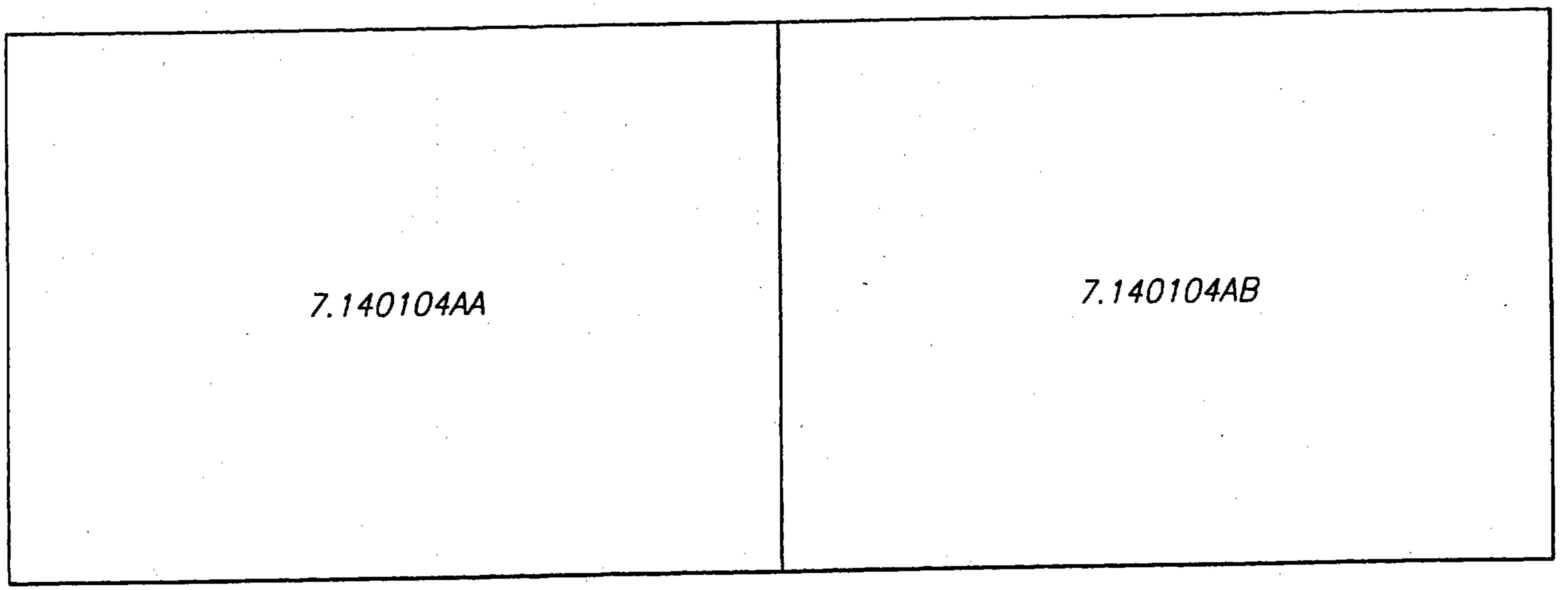
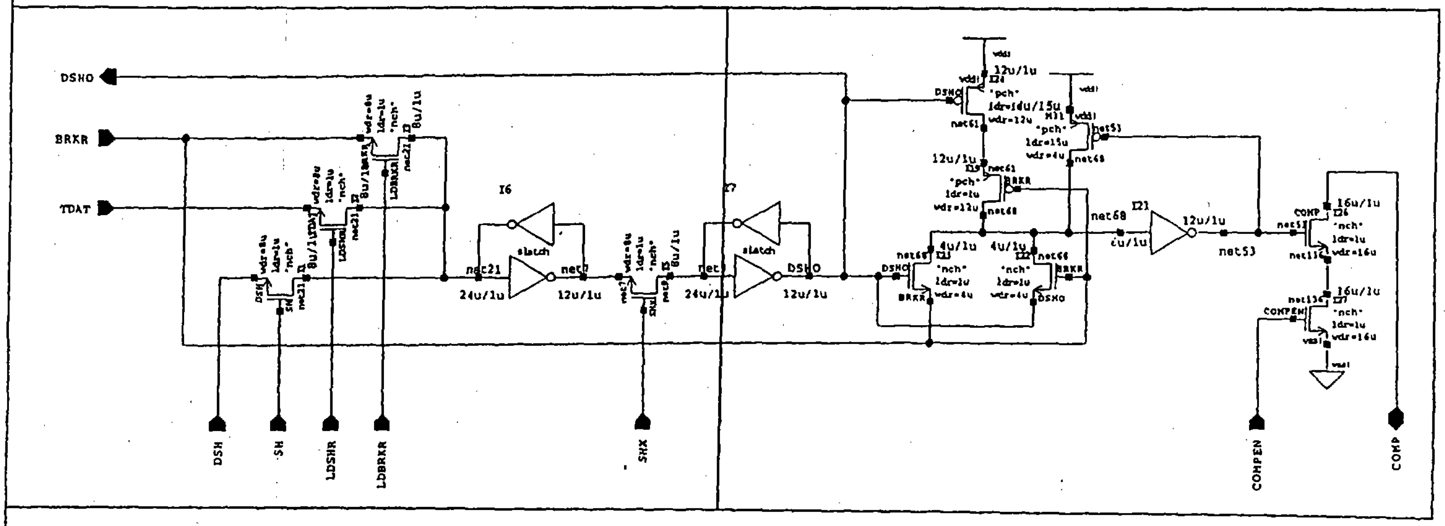


FIG. 7.140104



7.140104

FIG. 7.140[illegible]of

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: SIO Shift Register
NAME: 103reva/sioshr
REV: B1
SIZE: A
DATE: Sep 2 08:06:26 1994
SHEET:

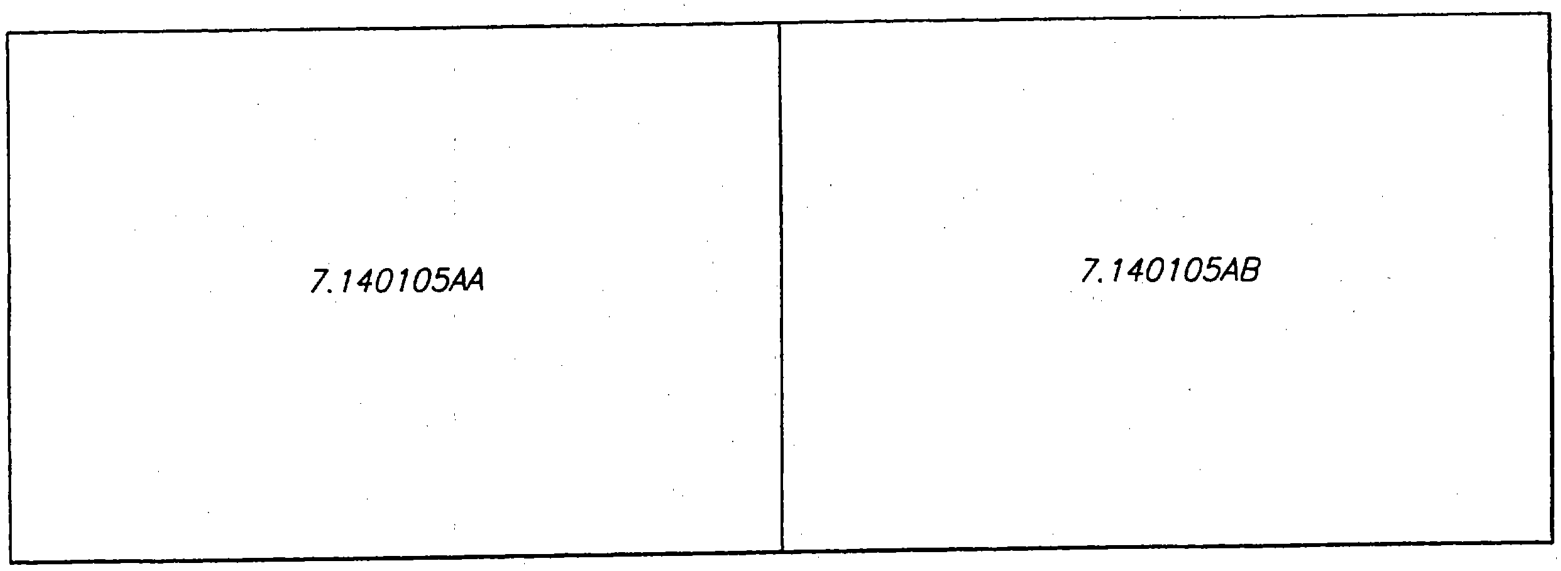
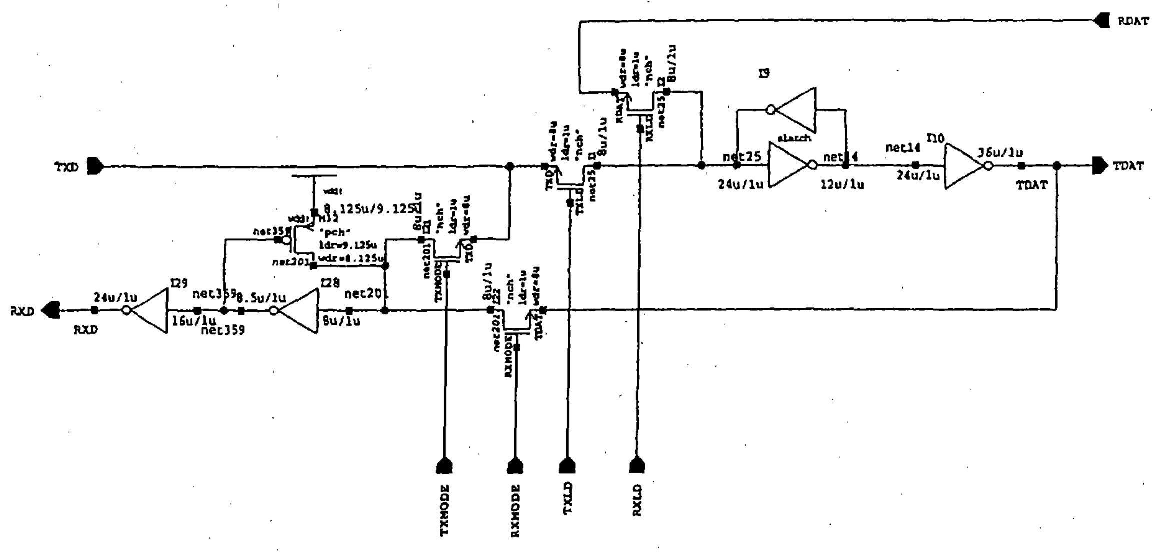


FIG 7.140105



B8: added feedback device

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: SIO Bidirectional Latch	
NAME: 103reva/siobdlat	REV: B8 SIZE: A
DATE: Jan 8 11:04:57 1996	SHEET:

FIG. 7.140105

		7.1402AC	7.1402AD	7.1402AE	7.1402AF	7.1402AG	7.1402AH	7.1402AI
7.1402BA	7.1402BB	7.1402BC	7.1402BD	7.1402BE	7.1402BF	7.1402BG	7.1402BH	7.1402BI
7.1402CA	7.1402CB	7.1402CC	7.1402CD	7.1402CE	7.1402CF	7.1402CG	7.1402CH	7.1402CI
7.1402DA	7.1402DB	7.1402DC	7.1402DD	7.1402DE	7.1402DF	7.1402DG	7.1402DH	7.1402DI
7.1402EA	7.1402EB	7.1402EC	7.1402ED	7.1402EE	7.1402EF	7.1402EG	7.1402EH	7.1402EI

Fig. 7.1402

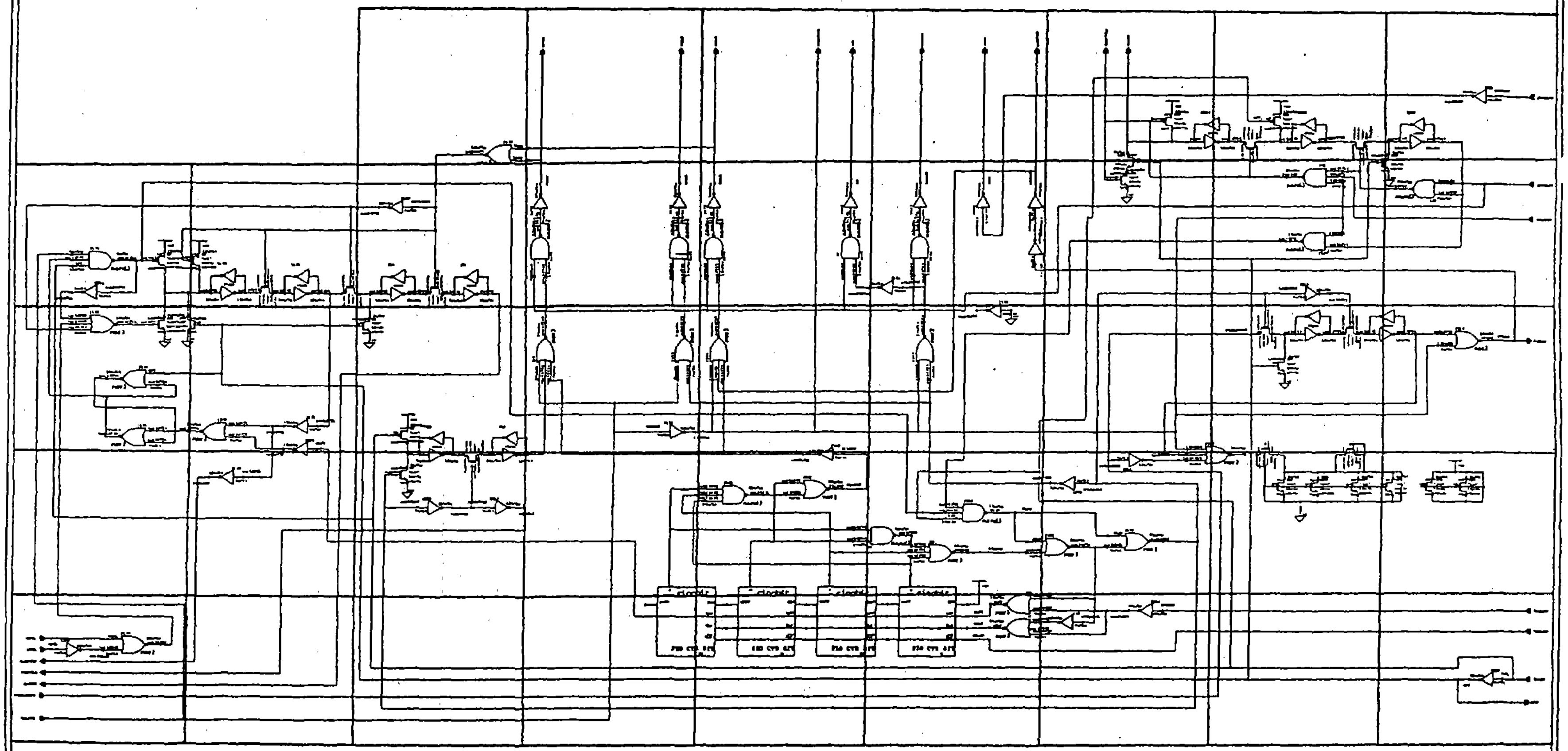


FIG. 7.1902

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

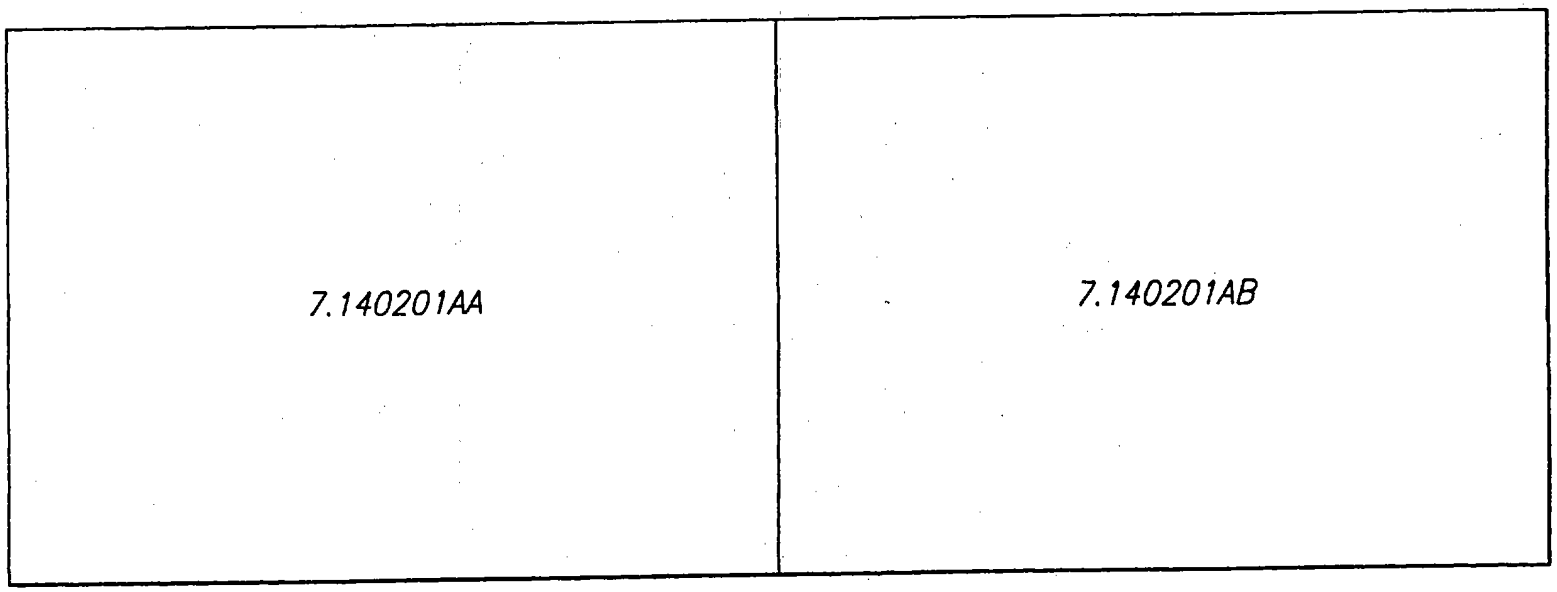
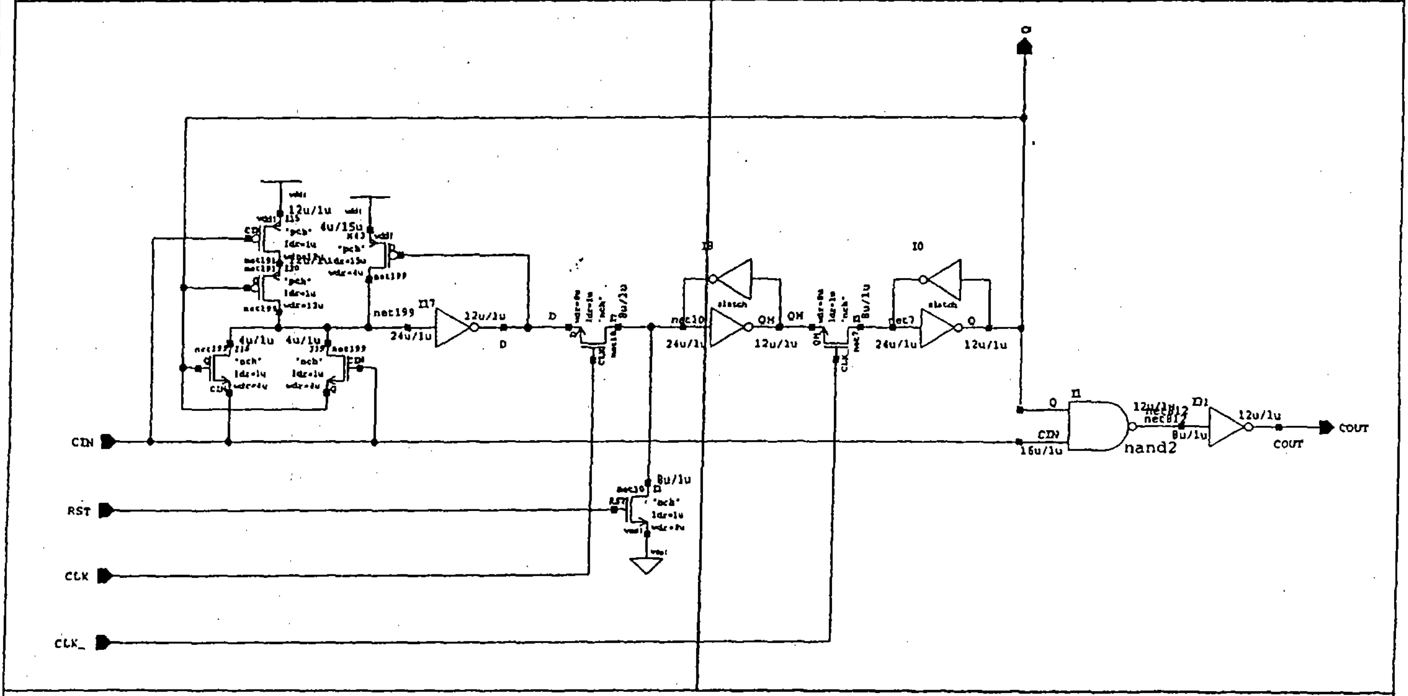


Fig 7.140201



MICRON COMMUNICATIONS, INC.	PROJECT: L03	DESIGNER: JOTOOLE	
INTEGRATED CIRCUIT DESIGN	TITLE: SIO Counter Bit		
CONFIDENTIAL INFORMATION	NAME: 103reva/siocbit	REV: B1	SIZE: A
	DATE: Sep 2 08:11:19 1994	SHEET:	

FIG. 7.190~~104~~201

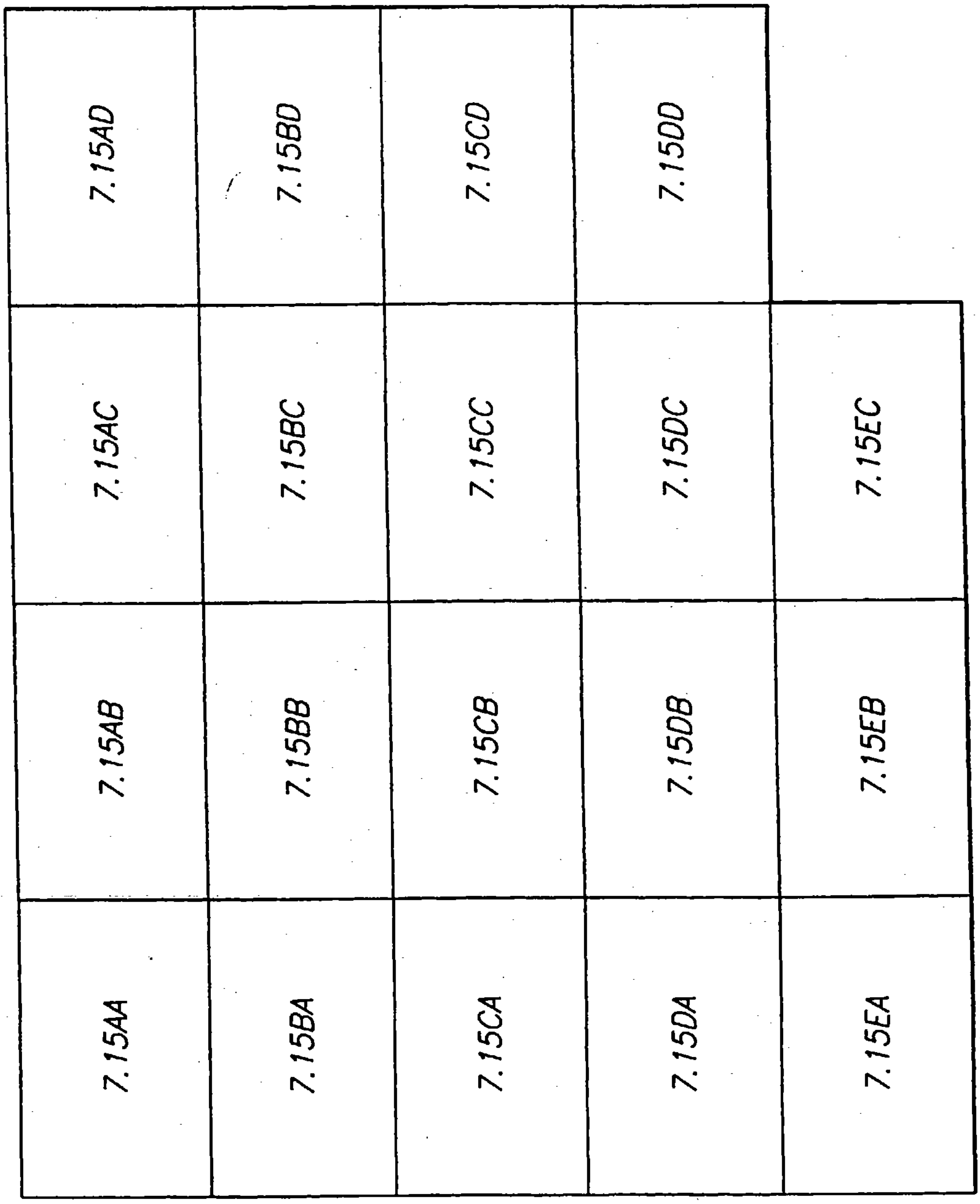

7.15AD
7.15AC
7.15AB
7.15AA
7.15BD
7.15BC
7.15BB
7.15BA
7.15CD
7.15CC
7.15CB
7.15CA
7.15DD
7.15DC
7.15DB
7.15DA
7.15EC
7.15EB
7.15EA

FIG. 7.15

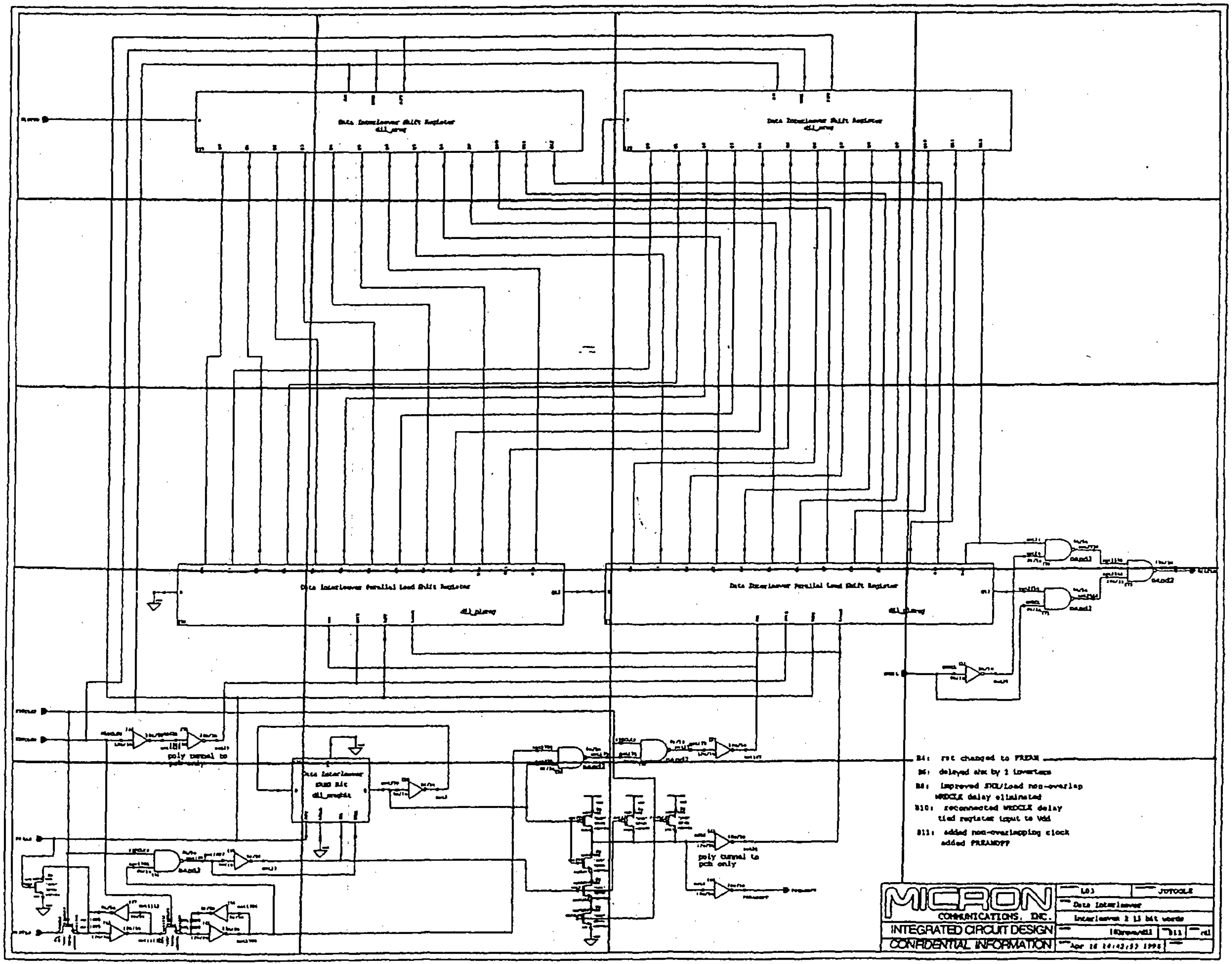

Data Interleaver Shift Register
dil_sreg
Data Interleaver Shift Register
dil_sreg
Data Interleaver Parallel Load Shift Register
dil_plsreg
Data Interleaver Parallel Load Shift Register
dil_plsreg
Data Interleaver
SUBB Bit
dil_msgbit
poly tunnel to
pch only
poly tunnel to
pch only
nand1
nand2
nand3
B4: rst changed to PREAM
B6: delayed shx by 2 inverters
B8: improved SHX/Load non-overlap
WRDCLK delay eliminated
B10: reconnected WRDCLK delay
tied register input to Vdd
B11: added non-overlapping clock
added PREAMOFF
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
JOTOOLE
Data Interleaver
Interleaver 2 13 bit words
B11
Apr 16 14:42:53 1996

FIG. 7.15

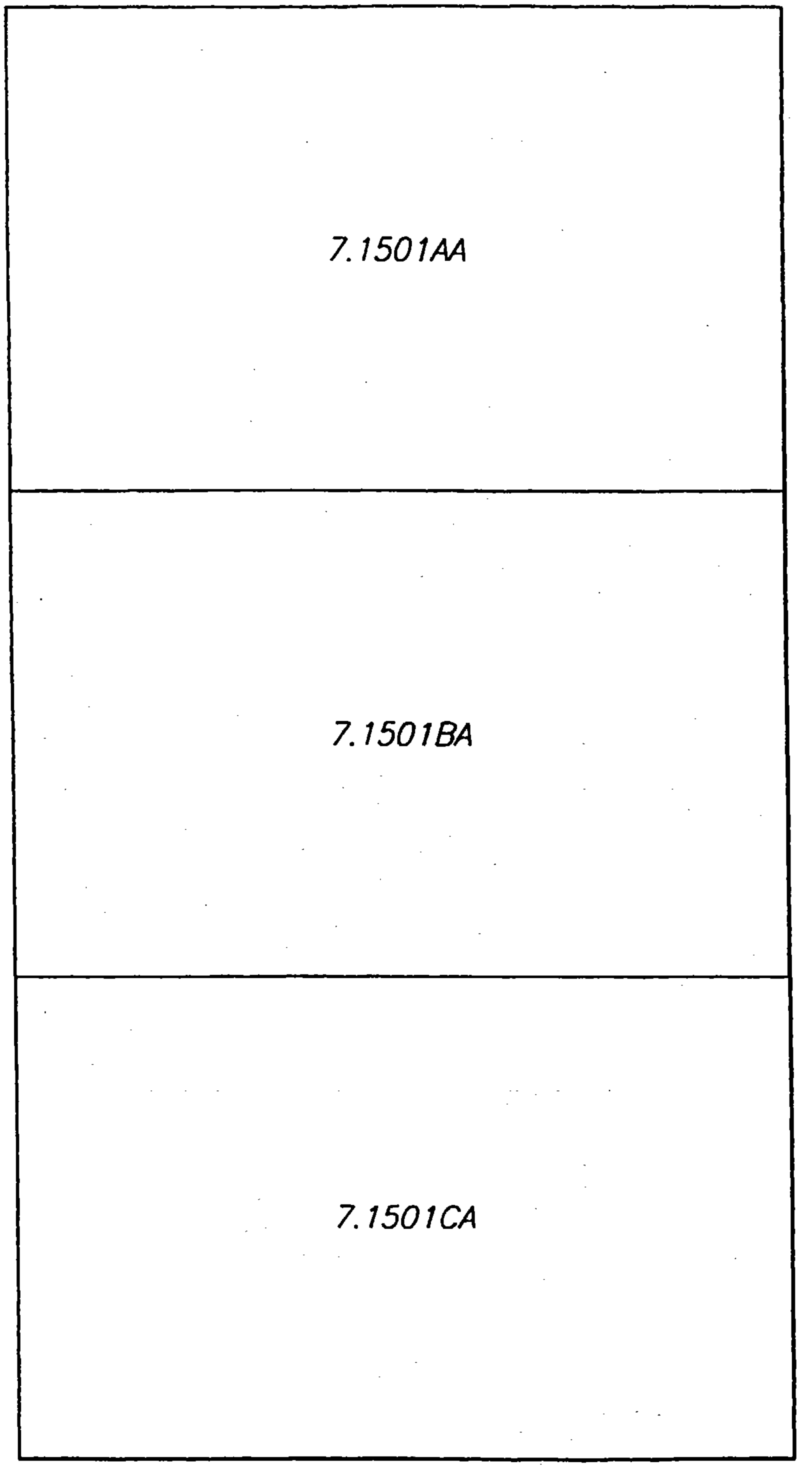


Fig 7.1501

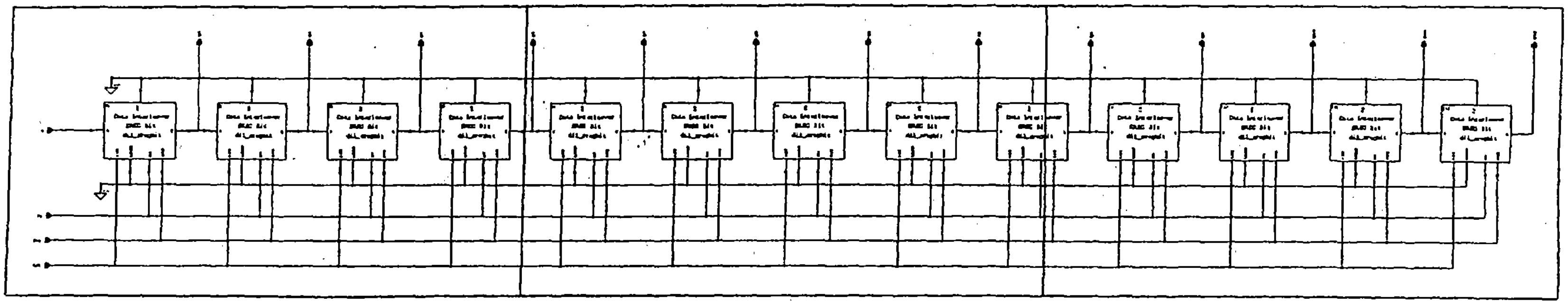


Fig. 7.1501

MICRON
COMMUNICATIONS, INC
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

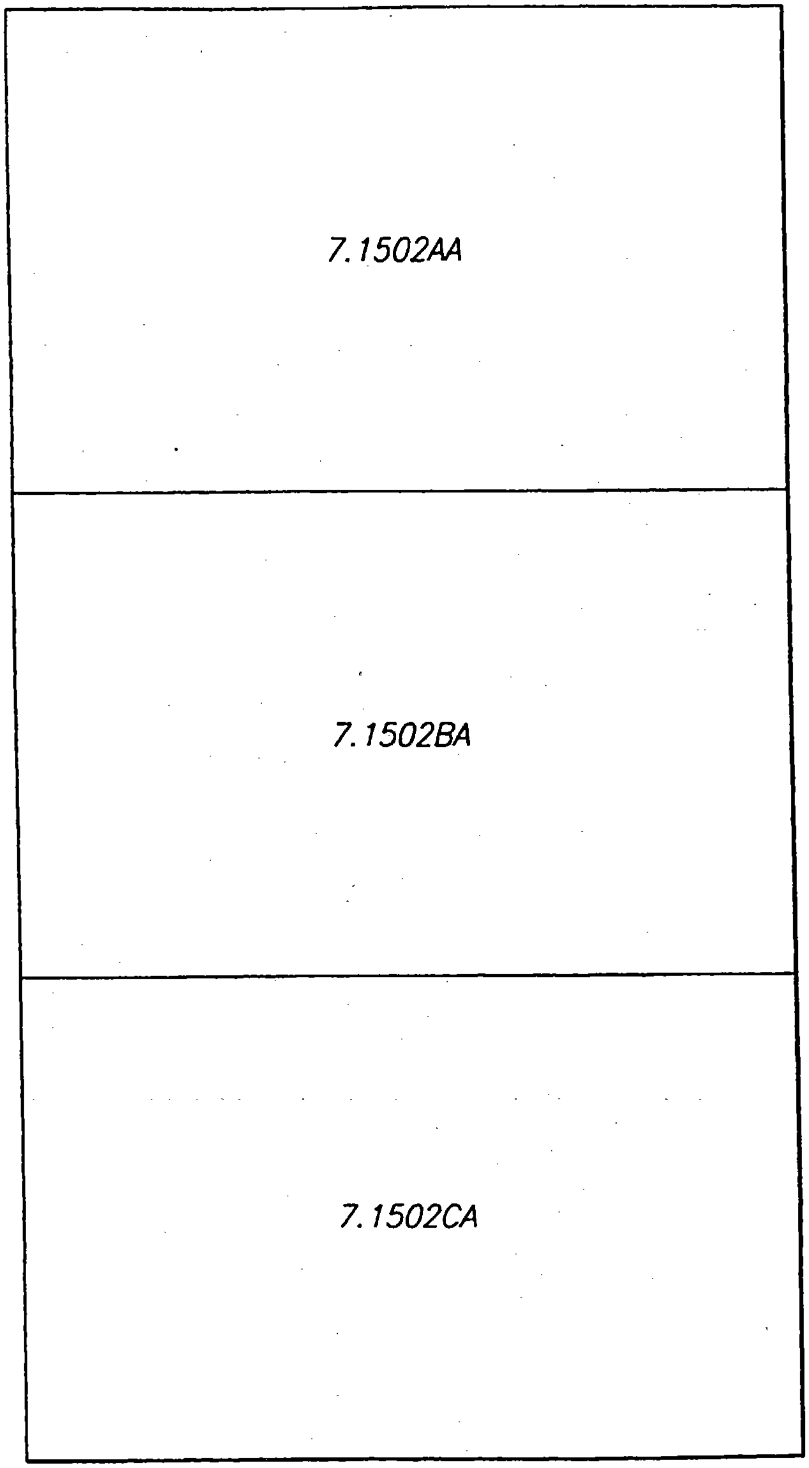


Fig 7.1502

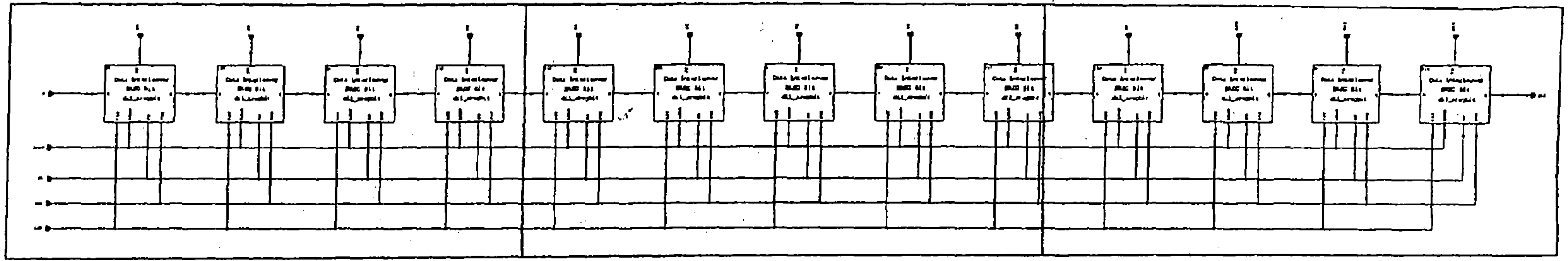
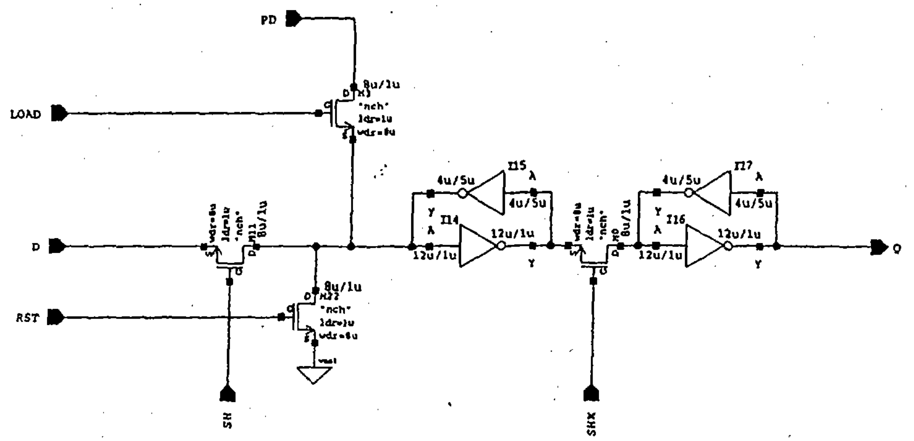


Fig. 7.1502

MICRON
COMMUNICATIONS, INC
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION



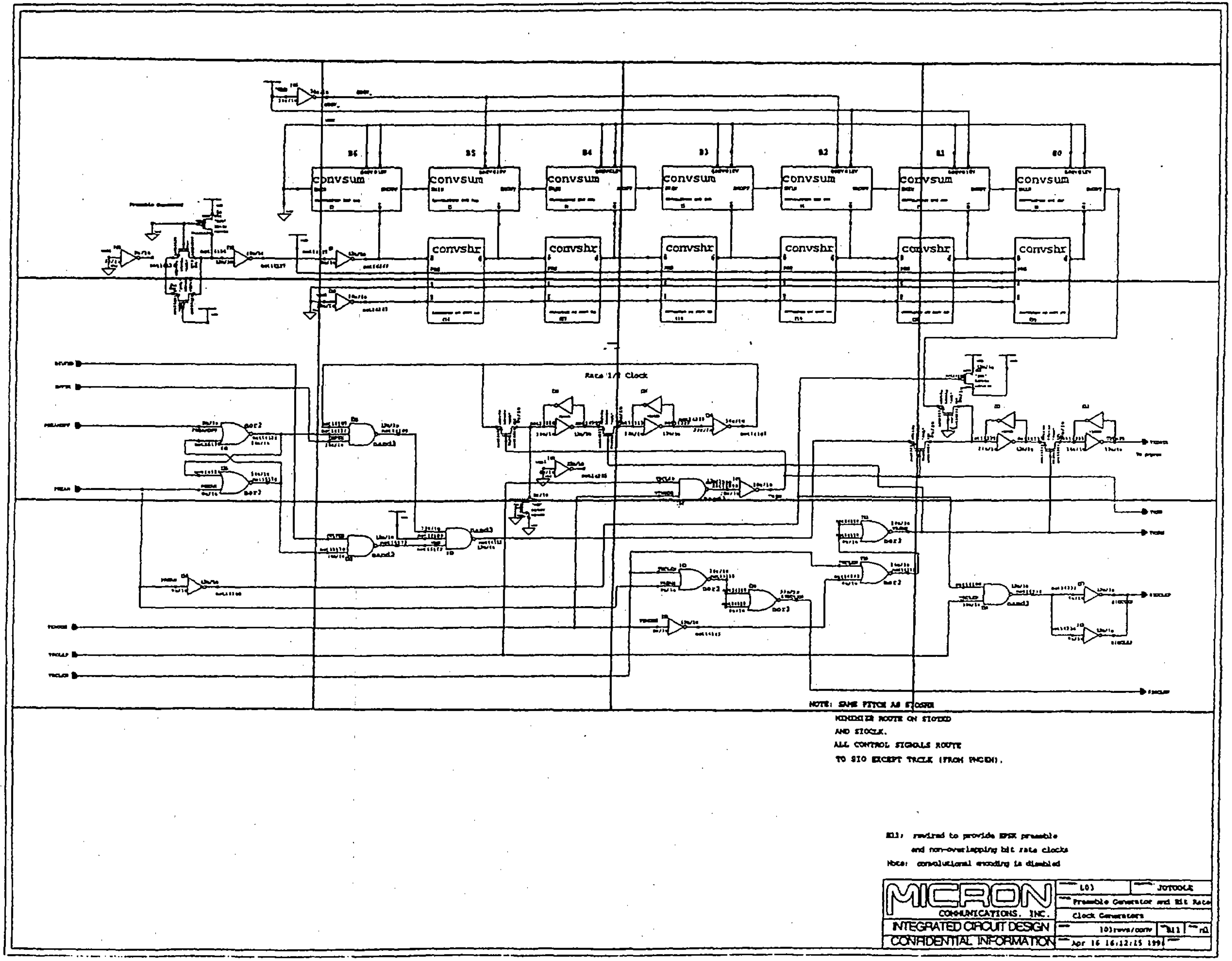
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: Data Interleaver Shift Register Bit			
NAME: 103reva/dil_sregbit	REV: B1	SIZE: A	
DATE: Sep 27 10:25:07 1994	SHEET:		

FIG. 7.150201

7.16AA	7.16AB	7.16AC	7.16AD
7.16BA	7.16BB	7.16BC	7.16BD
7.16CA	7.16CB	7.16CC	7.16CD

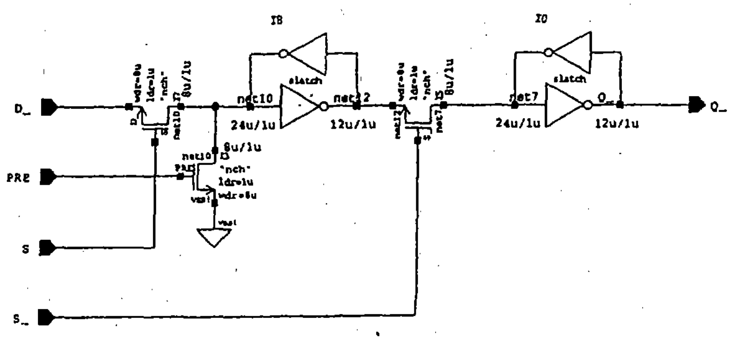
Fig 7.16



NOTE: SAME PITCH AS SIOSHR
MINIMIZE ROUTE ON SIOTXD
AND SIOCLK.
ALL CONTROL SIGNALS ROUTE
TO SIO EXCEPT TXCLK (FROM PNGEN).

B11: rewired to provide BPSK preamble
and non-overlapping bit rate clocks
Note: convolutional encoding is disabled

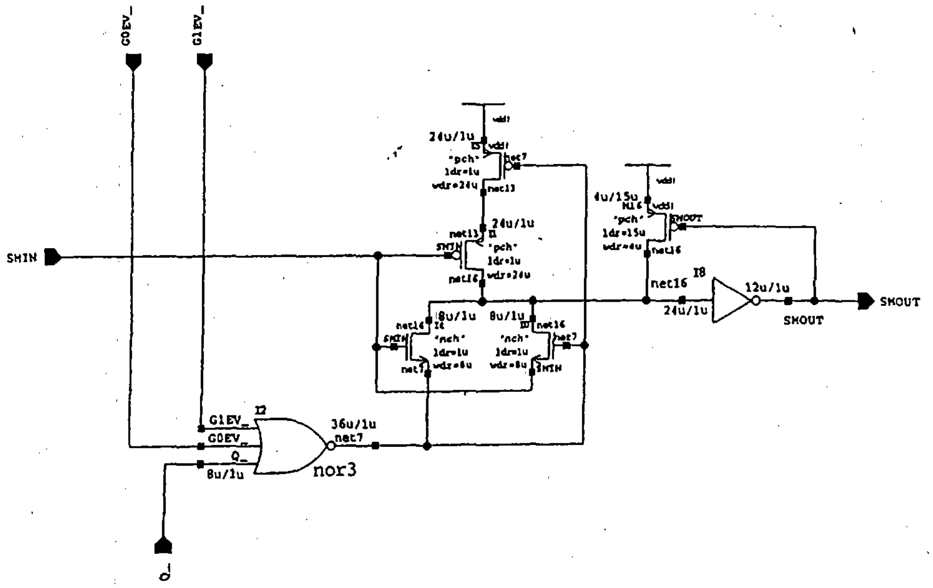
FIG. 7.16



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: Convolutional Encoder Shift
Register Cell
NAME: 103reva/convshr
REV:
SIZE: A
DATE: Sep 2 10:34:27 1994
SHEET:

Fig. 7.1601



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE		
TITLE: Convolutional Encoder Summer			
NAME: 103reva/convsum	REV: B1	SIZE: A	
DATE: Sep 2 10:32:17 1994	SHEET:		

FIG. 7.1602

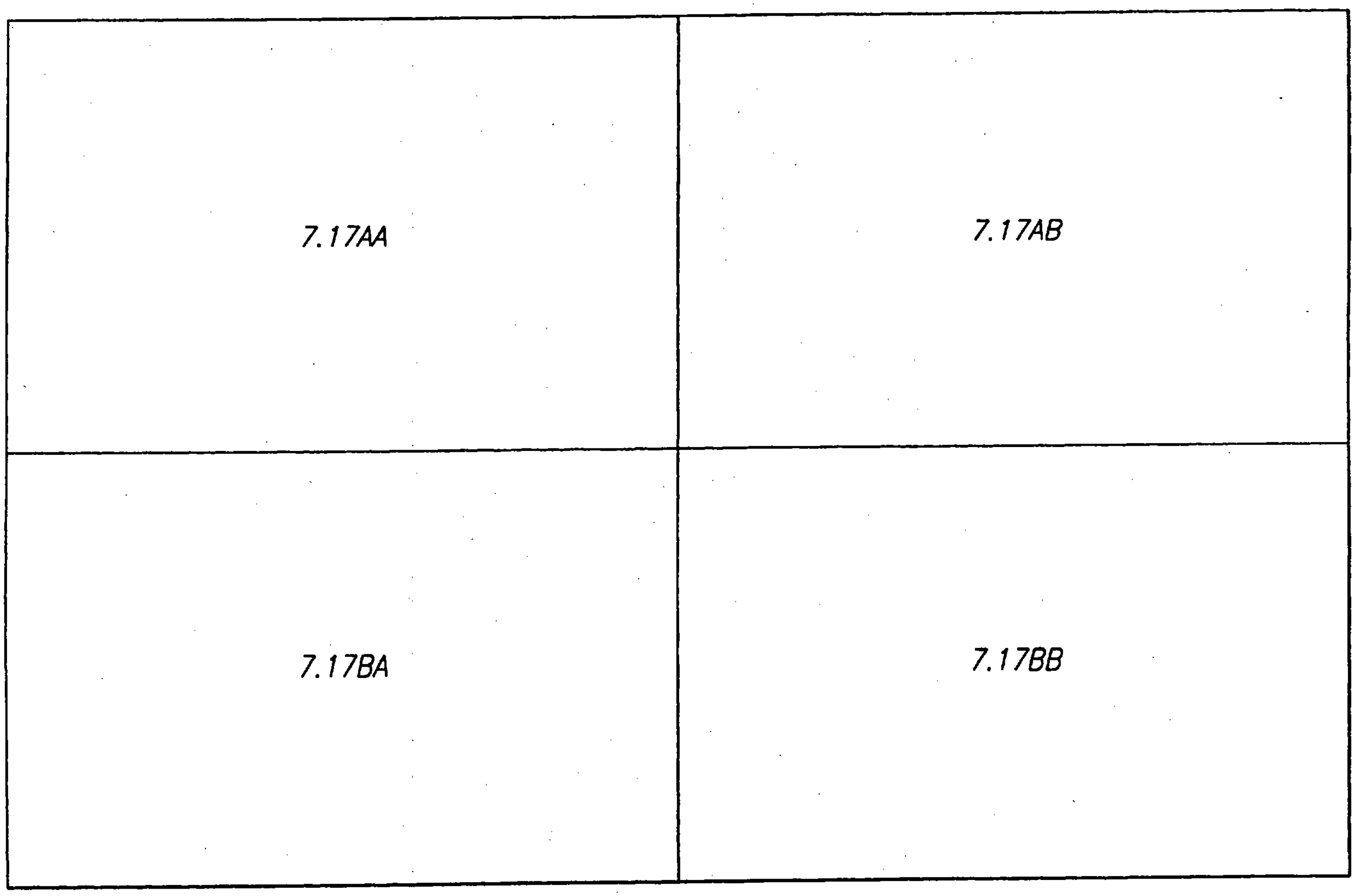
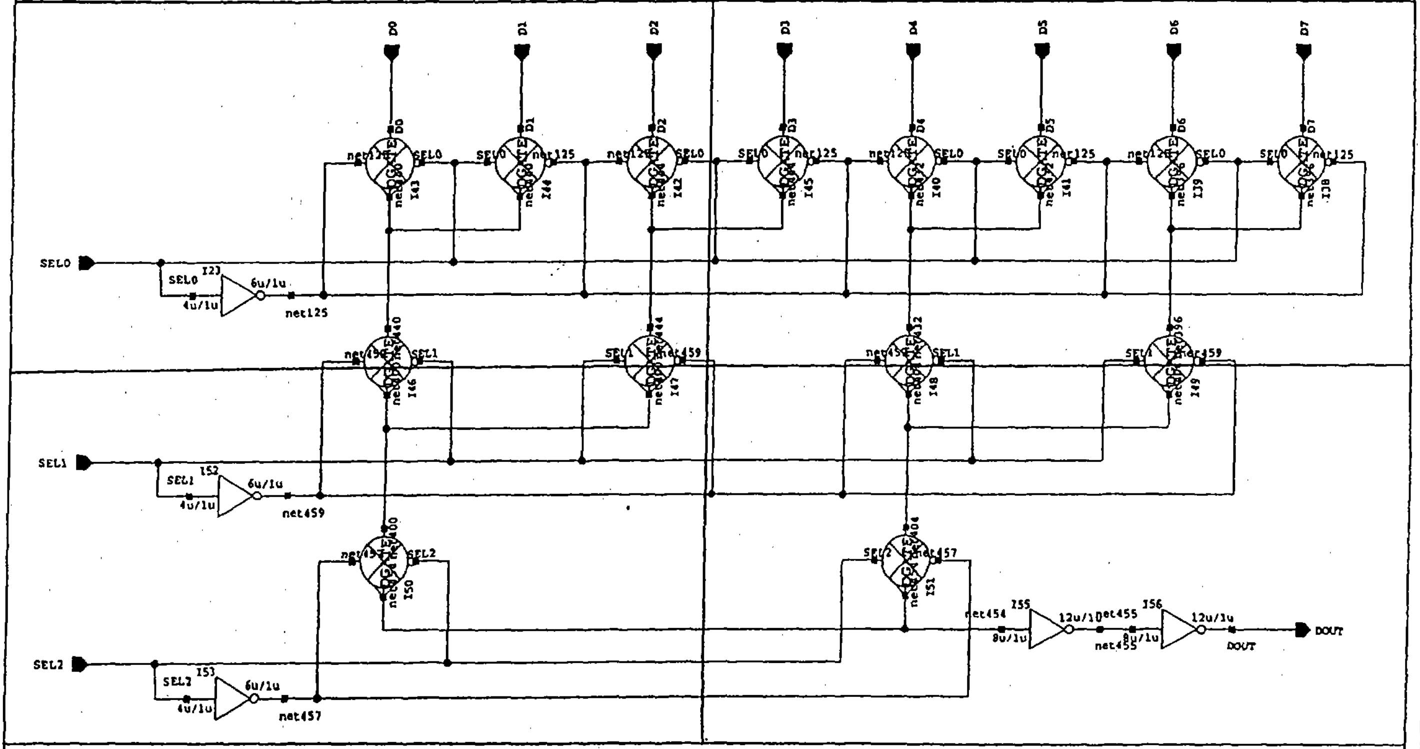


FIG. 7.17



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: Shift Register Input Data Mux
8 to 1 MUX
NAME: 103reva/shdsel
REV: -
SIZE: A
DATE: Nov 11 06:55:32 1993
SHEET:

FIG. 7.17

7.18AA	7.18AB	7.18AC
7.18BA	7.18BB	7.18BC
7.18CA	7.18CB	7.18CC

Fig. 7.18

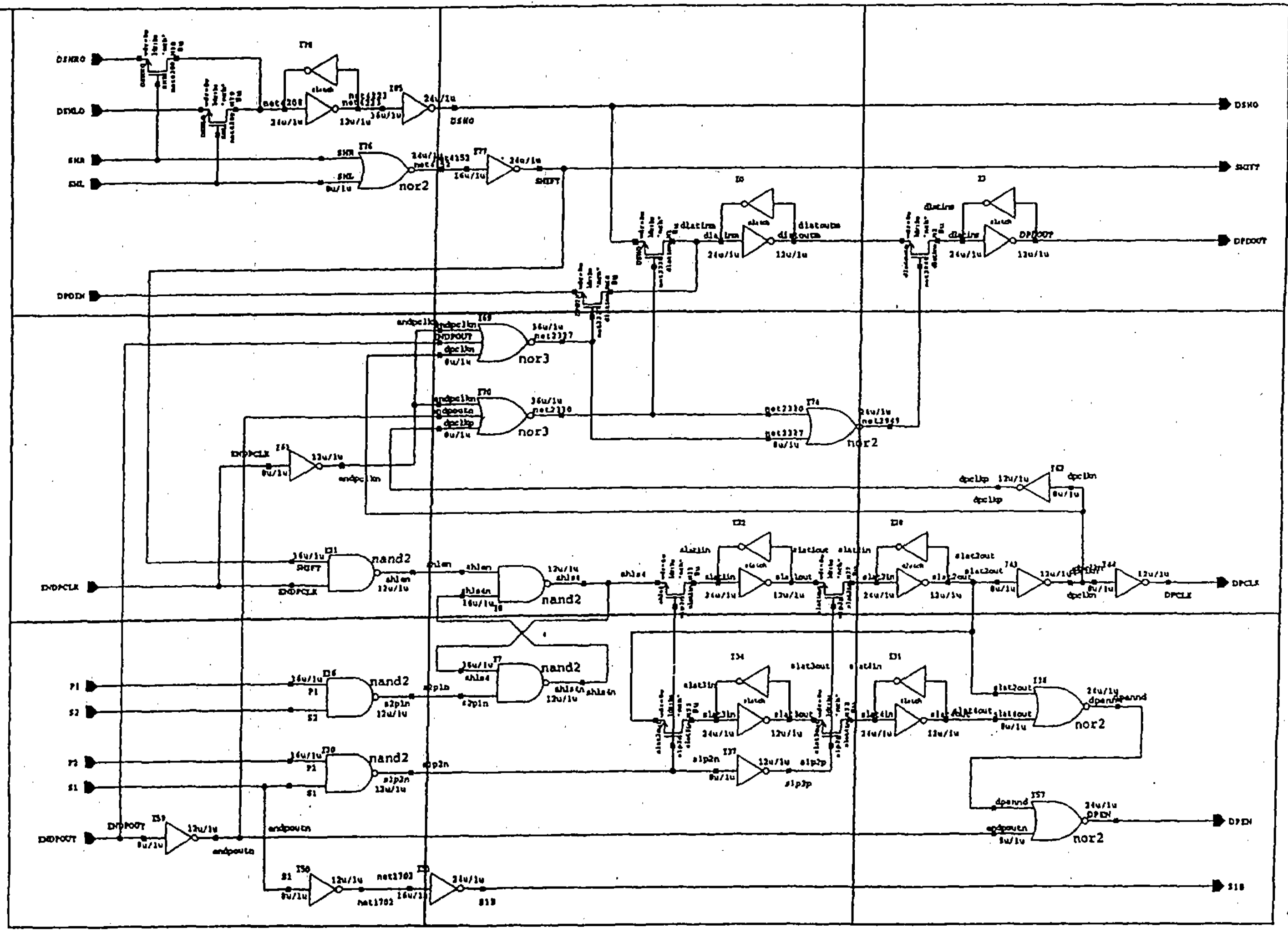


Fig. 7.18

MICRON COMMUNICATIONS, INC.	PROJECT: L03
	DESIGNER: Rotzoll
	TITLE: Digital Port Output Controller
INTEGRATED CIRCUIT DESIGN	NAME: 103reva/doutport
	REV: -
	SCALE: nil
CONFIDENTIAL INFORMATION	DATE: Nov 12 10:05:40 1993
	SHEET:

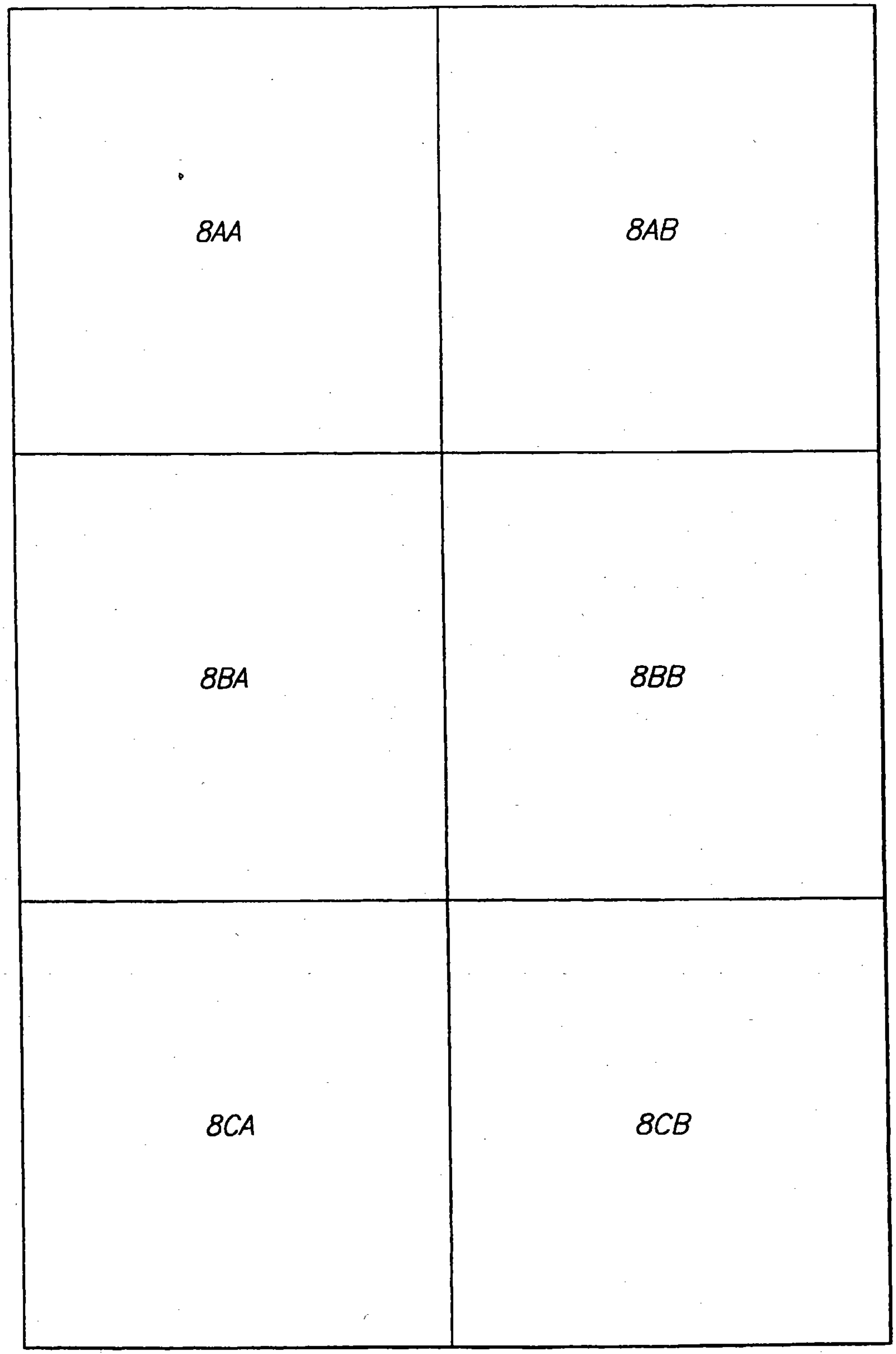
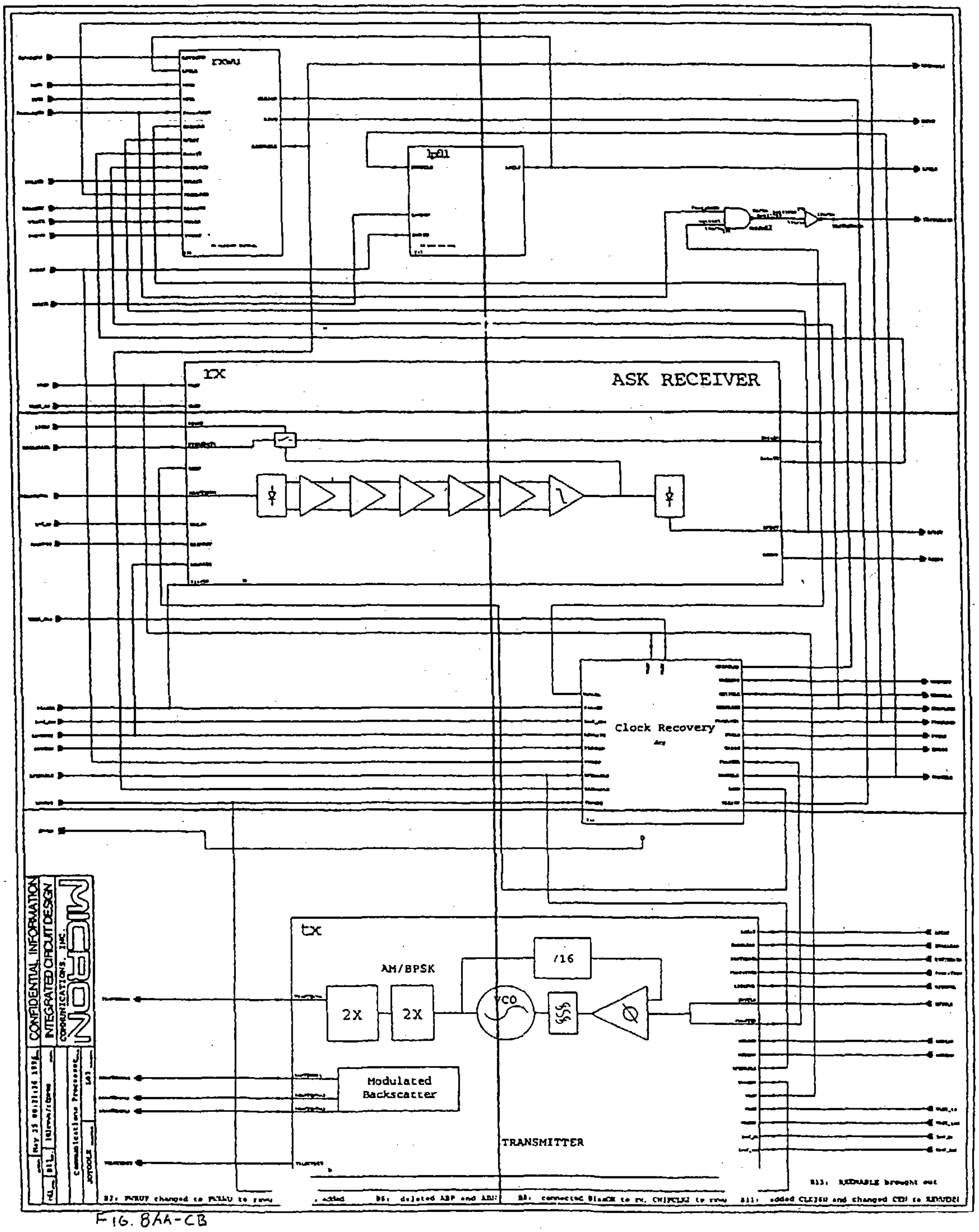


Fig 8



rxwu
lpf1
rx
ASK RECEIVER
Clock Recovery
tx
AM/BPSK
2X
2X
VCO
/16
Modulated Backscatter
TRANSMITTER
CONFIDENTIAL INFORMATION
INTEGRATED CIRCUIT DESIGN
MICRON
COMMUNICATIONS, INC.
Communications Processor

FIG. 8AA-CB

8.01AA	8.01AB	8.01AC	8.01AD	8.01AE
8.01BA	8.01BB	8.01BC	8.01BD	8.01BE
8.01CA	8.01CB	8.01CC	8.01CD	8.01CE
8.01DA	8.01DB	8.01DC	8.01DD	8.01DE

Fig 8.01

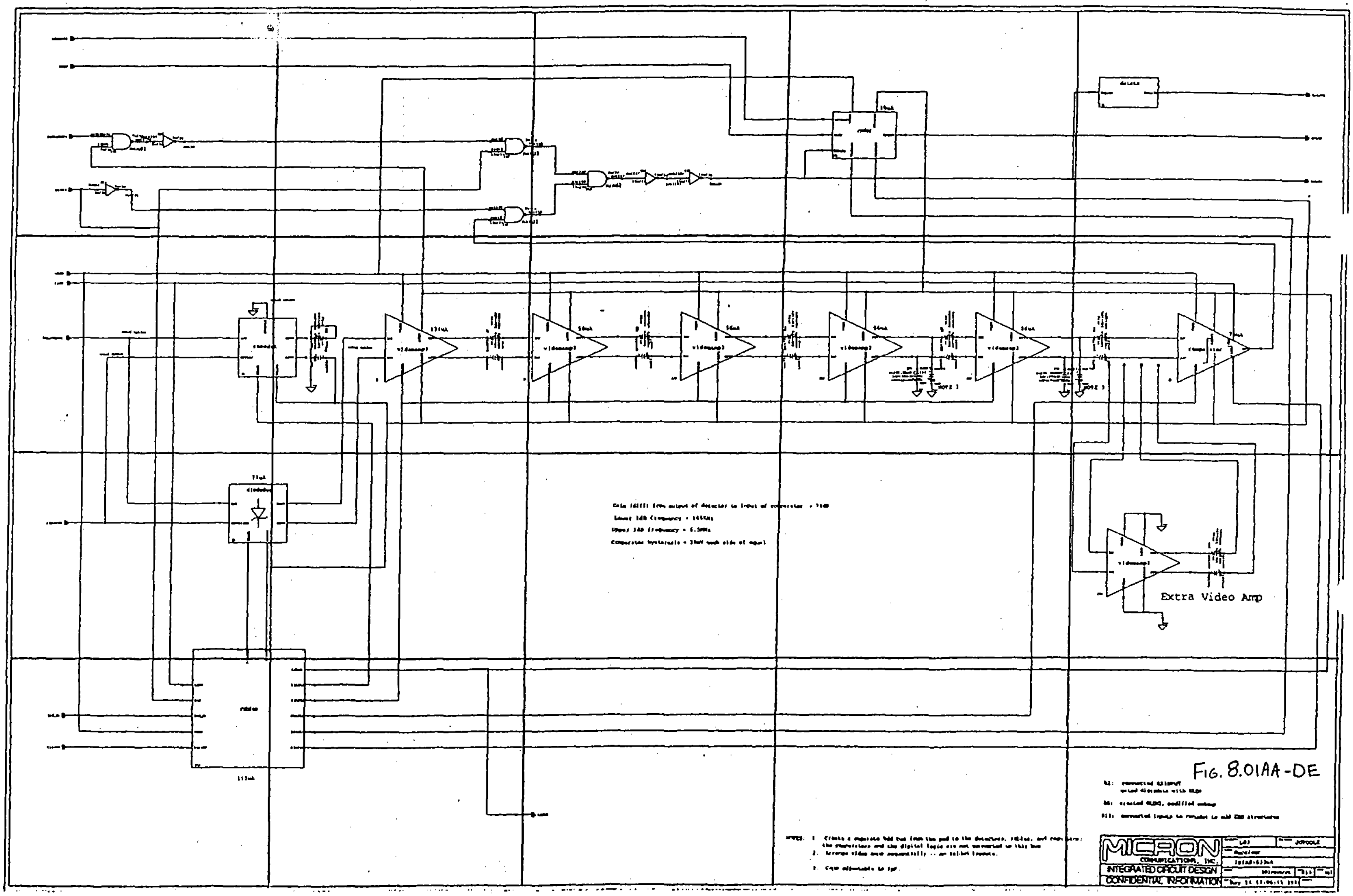
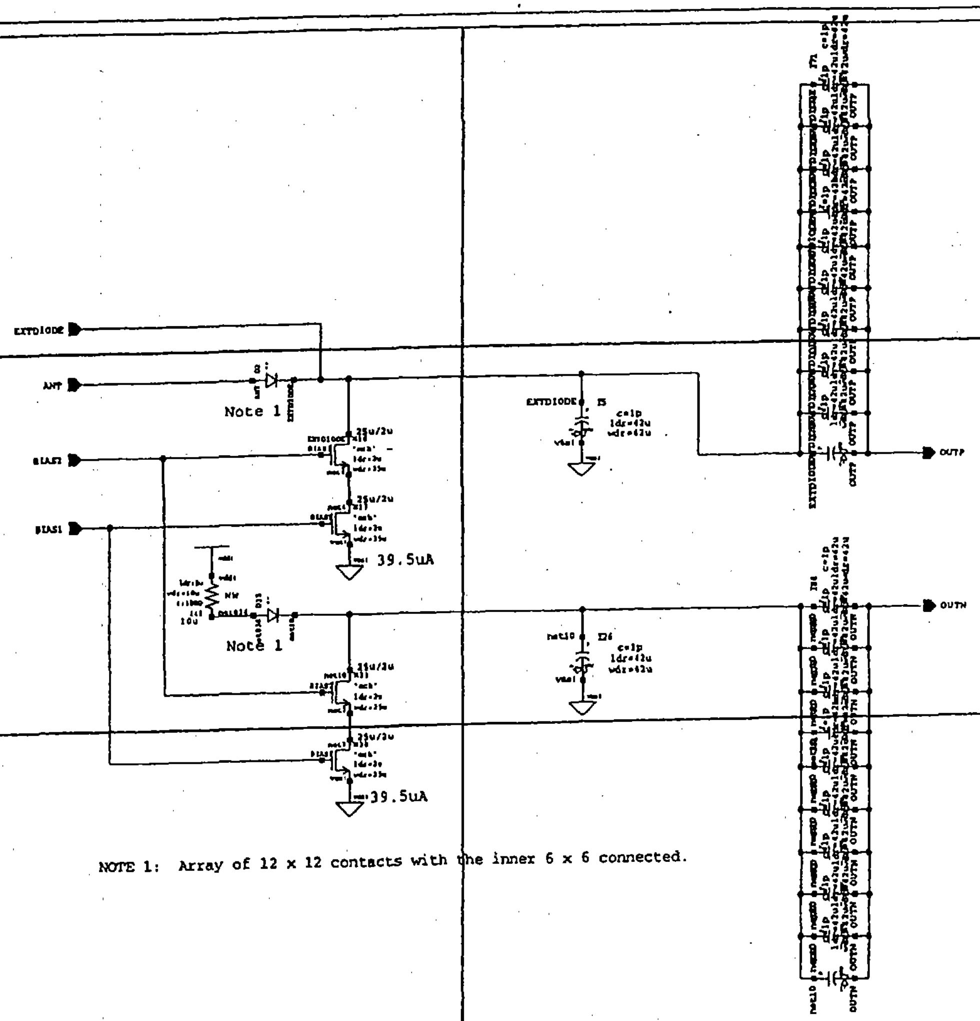

Extra Video Amp
videoamp2
Gain (diff) from output of detector to input of comparator = [illegible]
Lower 3dB frequency = [illegible]
Upper 3dB frequency = [illegible]
Comparator hysteresis = [illegible] each side of equal
NOTES: 1. Create a separate Vdd bus from the pad to the detectors, [illegible], and comparators; the comparators and the digital logic are not connected to this bus
2. Arrange video amps sequentially -- [illegible] layout.
3. Cap adjustable to [illegible].
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

Fig. 8.01AA-DE

8.0101AA	8.0101AB
8.0101BA	8.0101BB
8.0101CA	8.0101CB

Fig 8.0101



NOTE 1: Array of 12 x 12 contacts with the inner 6 x 6 connected.

F1G. 8. D101AA-CB

B2: connected EXTDIODE line
B6: schottky array changed to 6x6
rf cap reduced to 1pF
B8: increased Cc to 10pF; decreased Crf to 1pF
B13: added 1K resistor in series with dummy diode for ESD

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Schottky Diode Detector	
IBIAS=79uA	
NAME: 103reva/diodedet	REV: B13
DATE: May 24 13:54:28 1996	SHEET:

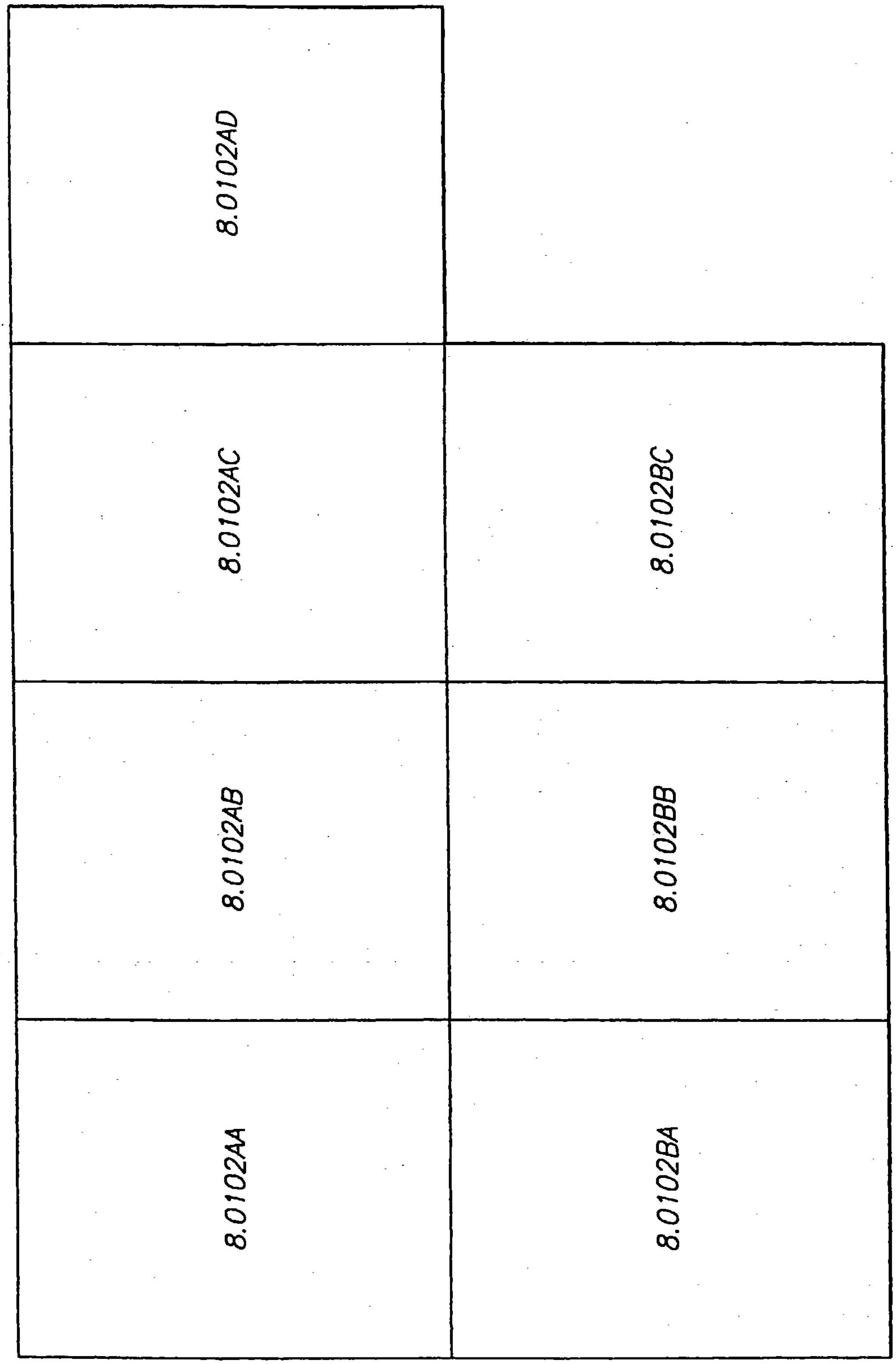
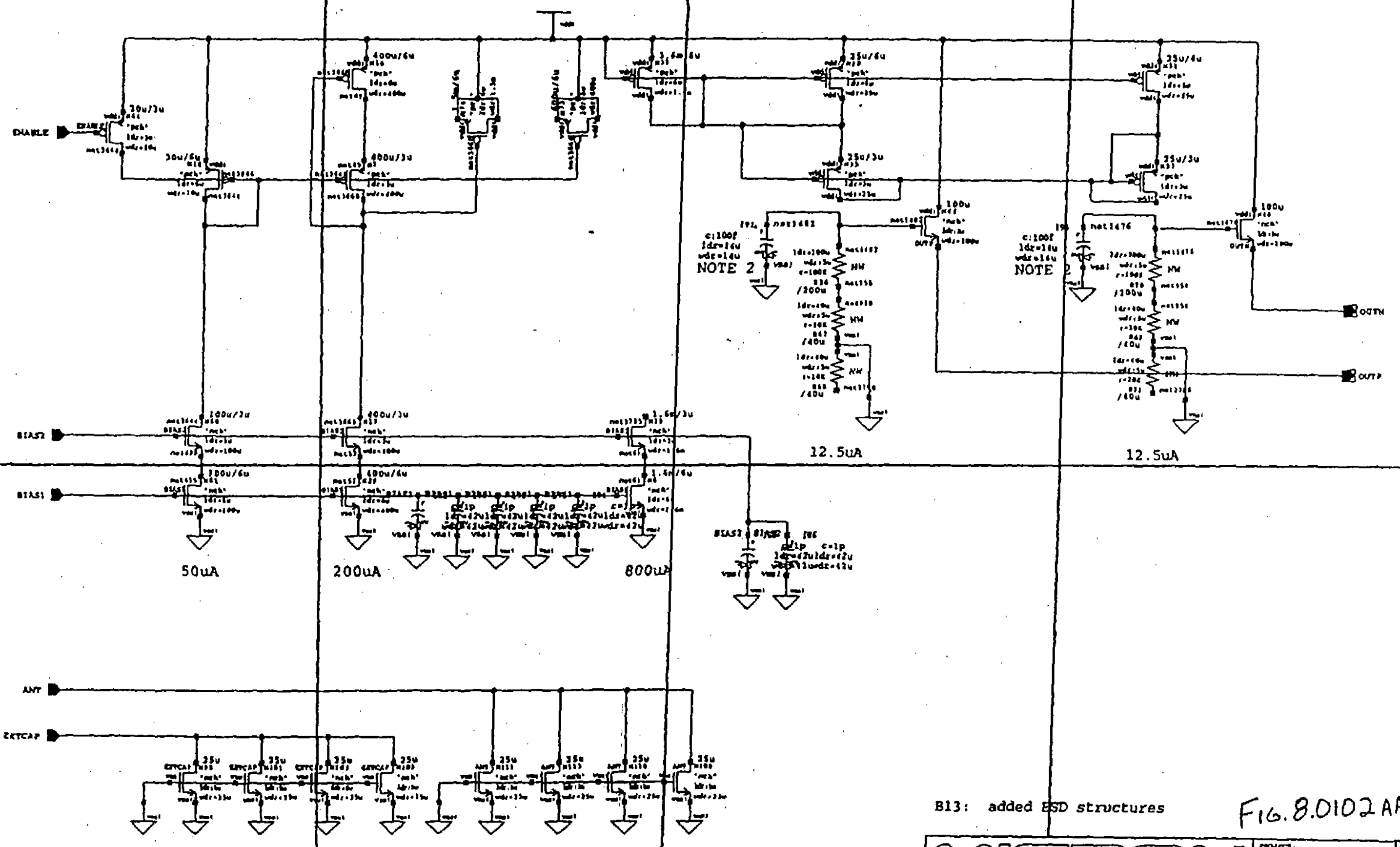


FIG. 8.0102



B13: added ESD structures

F16.8.0102AA-BC

NOTES:
1. All devices with W's > 100 are to be layed out with 100u segments.
2. Cap adjustable to 300fF (23/23)

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: CMOS Square Law Detector	
IBIAS=1.175mA	
NAME: 103reva/cmosdet	REV: B13 / SCALE: nil
DATE: May 25 14:10:58 1996	SHEET:

8.0103AA	8.0103AB	8.0103AC	8.0103AD	8.0103AE	8.0103AF
8.0103BA	8.0103BB	8.0103BC	8.0103BD	8.0103BE	8.0103BF
8.0103CA	8.0103CB	8.0103CC	8.0103CD	8.0103CE	8.0103CF

FIG. 8.0103

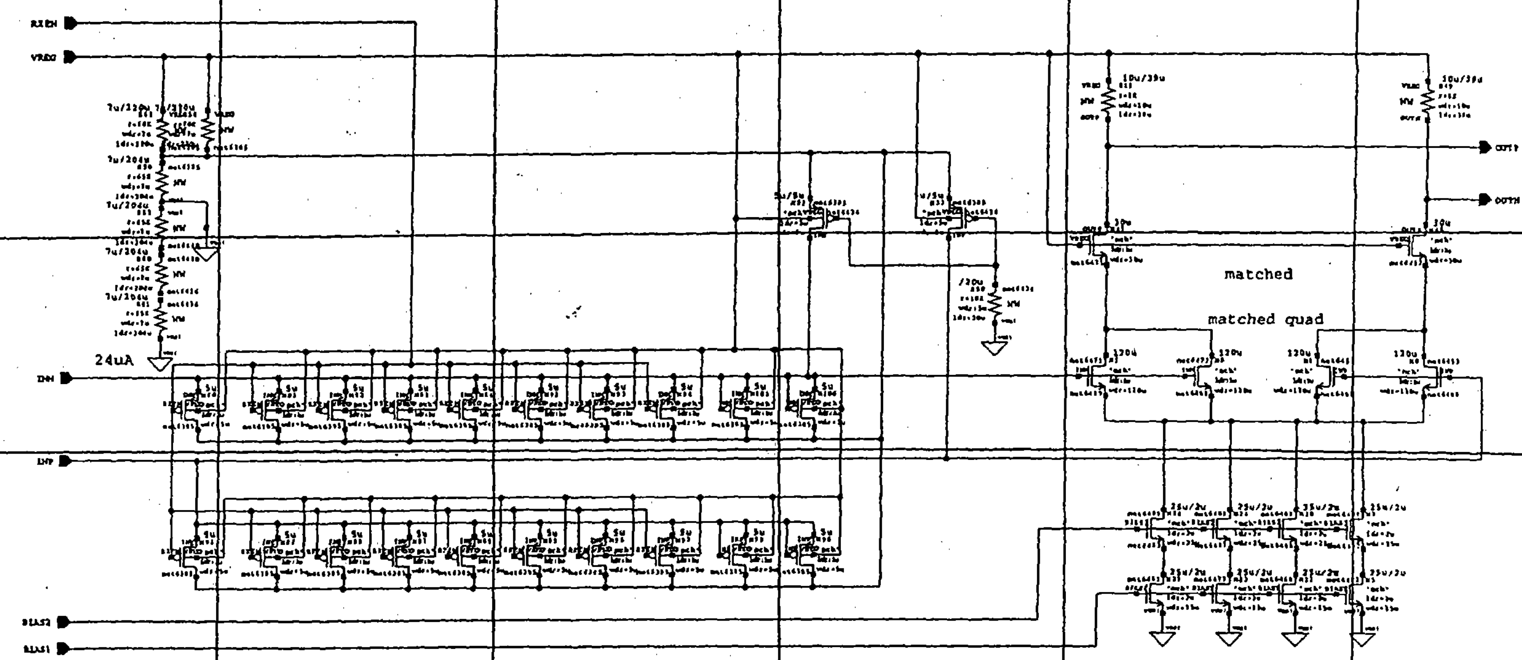


Fig. 8.0103

NOTES: 1. resistors are to be layed out at 50/10 and adjusted down to 39/10 with n+
2. p-channels are adjustable up to 5/100; adjustment is on source side

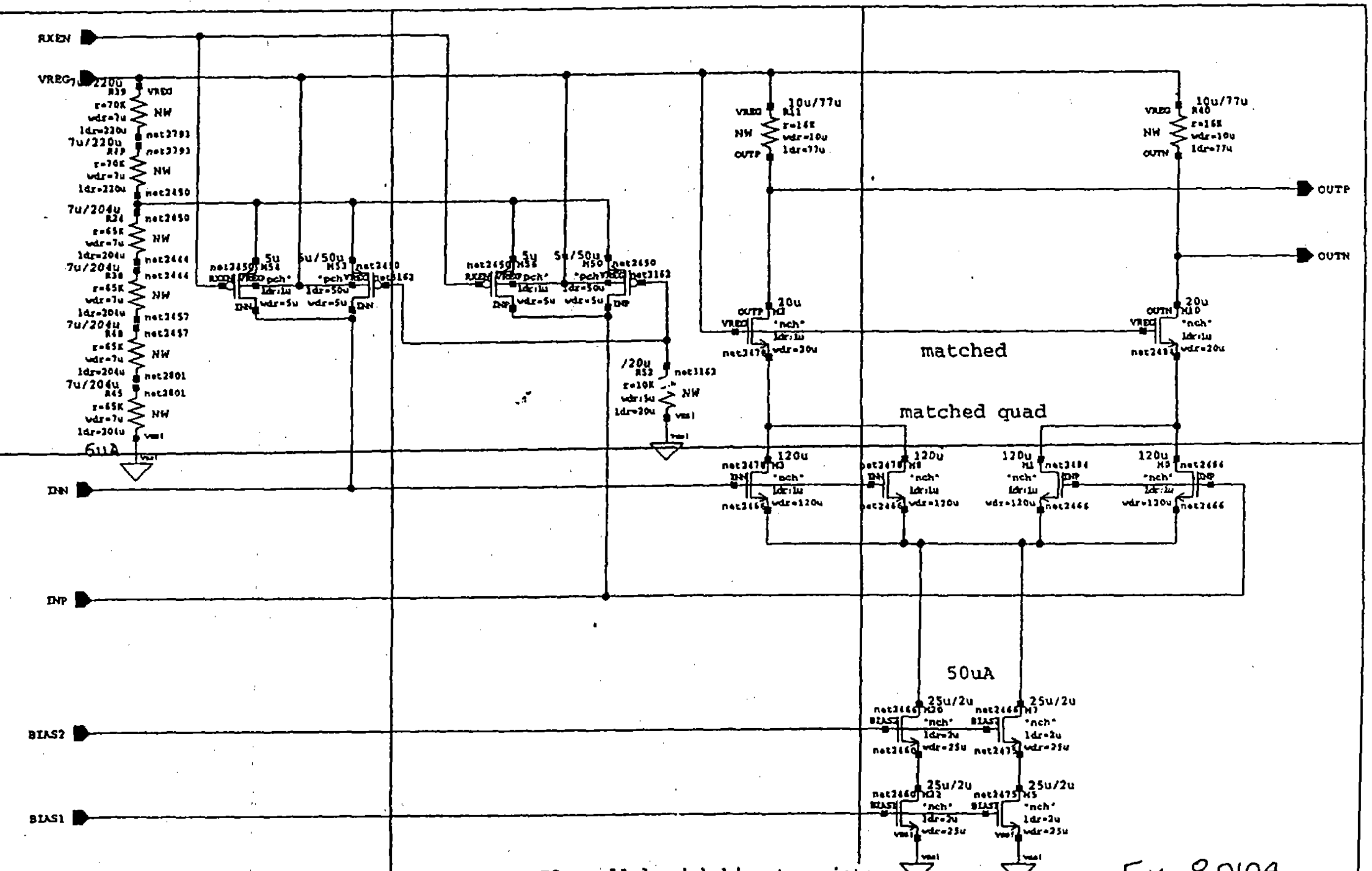
B8: Added quick bias transistors
Reduced L of pch bias devices

MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03		JOTOOLE	
Video Amplifier 1, IBias=124uA			
Av(diff)=4.8 (13.7dB)			
103reva/videoampl		B8	rll
Dec 16 13:40:53 1995			

8.0104AA	8.0104AB	8.0104AC
8.0104BA	8.0104BB	8.0104BC

Fig 8.0104



B8: added quick bias transistors

FIG 8,0104

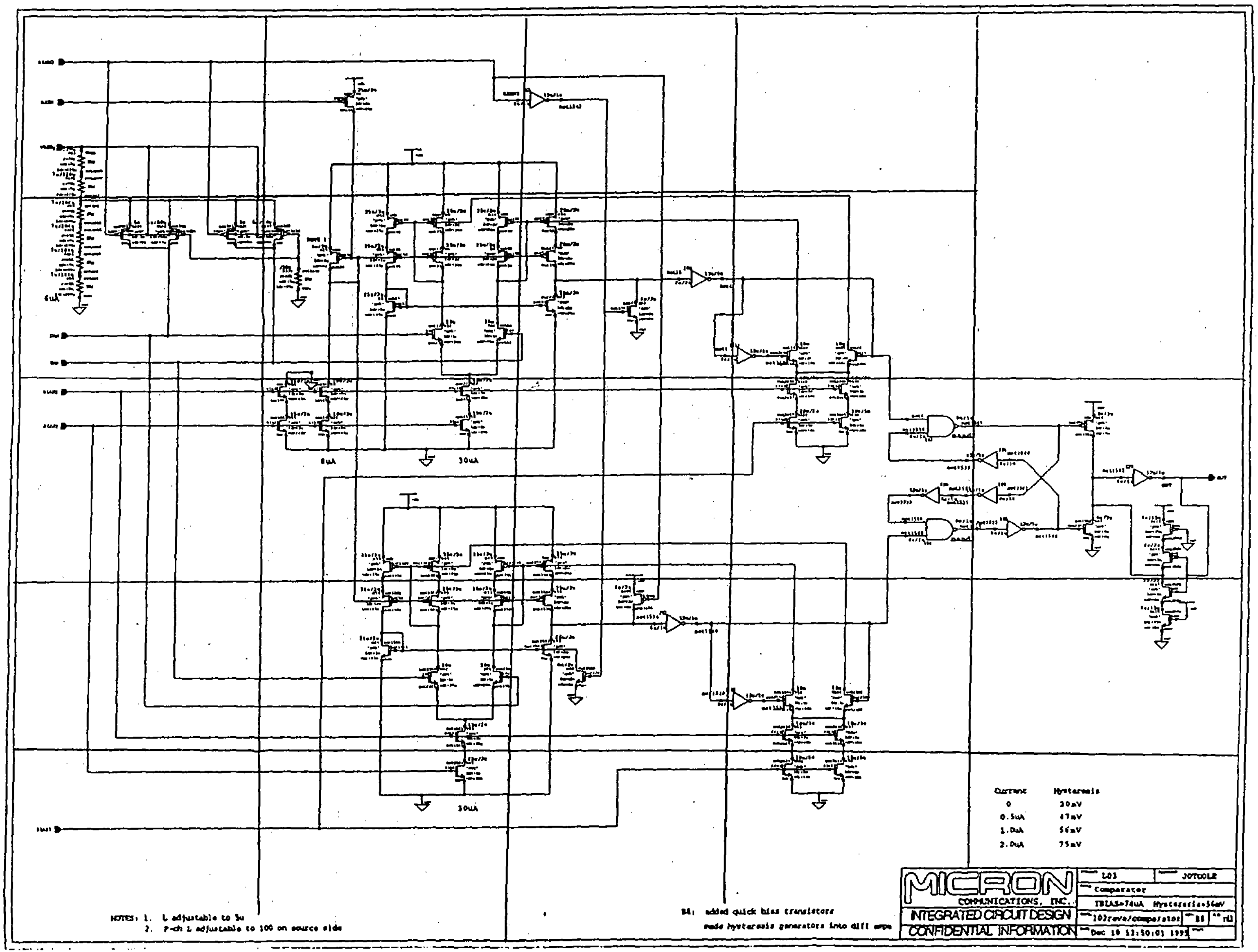
NOTES:
1. resistors are to be layed out at 100/10 and adjusted down to 77/10 with n+
2. p-channels are adjustable up to 5/100; adjustment is on the source side.

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Video Amplifier 2, IBias=56uA Av(diff)=5.6 (15dB)	
NAME: 103reva/videoamp2	REV: B8 SIZE: A
DATE: Dec 16 13:42:25 1995	SHEET:

8.0105AA	8.0105AB	8.0105AC	8.0105AD	
8.0105BA	8.0105BB	8.0105BC	8.0105BD	
8.0105CA	8.0105CB	8.0105CC	8.0105CD	8.0105CE
8.0105DA	8.0105DB	8.0105DC	8.0105DD	8.0105DE
8.0105EA	8.0105EB	8.0105EC	8.0105ED	

Fig 8.0105



Current	Hysteresis
0	30mV
0.5uA	47mV
1.0uA	56mV
2.0uA	75mV

NOTES: 1. L adjustable to 5u
2. P-ch L adjustable to 100 on source side

B4: added quick bias transistors
made hysteresis generators into diff amps

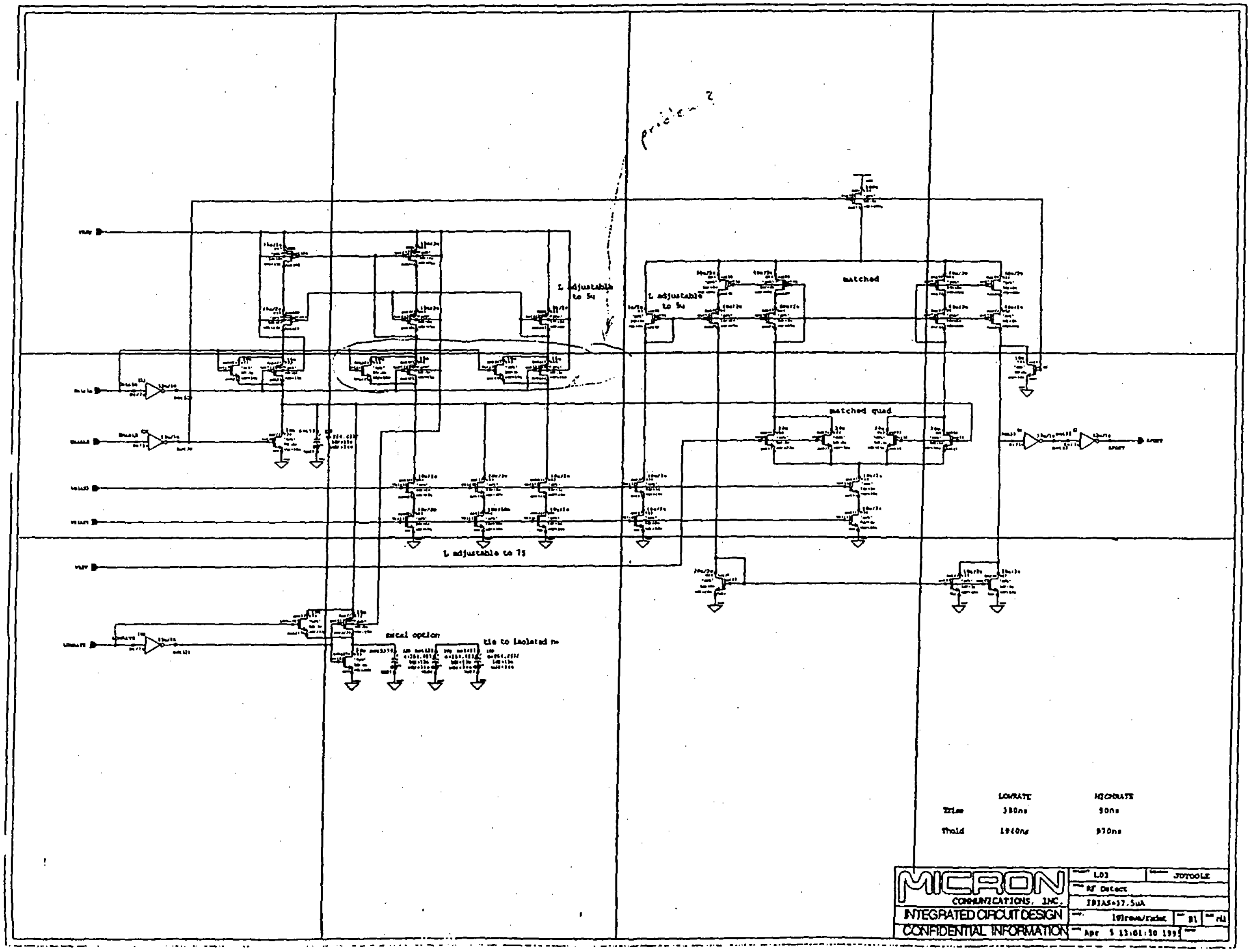
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
JOTOOLE
Comparator
IBIAS=74uA Hysteresis=56mV
103revb/comparator
B8
n1
Dec 19 12:50:03 1995

F1G. 8.0105

8.0106AA	8.0106AB	8.0106AC	8.0106AD
8.0106BA	8.0106BB	8.0106BC	8.0106BD
8.0106CA	8.0106CB	8.0106CC	8.0106CD

FIG 8.0106



	LOWRATE	HIGHRATE
Trise	380ns	90ns
Thold	1940ns	970ns

MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
JOTOOLE
RF Detect
IBIAS=37.5uA
10Trans/radet
Apr 5 13:01:30 1995

FIG. 8.0106

8.0107AA	8.0107AB	8.0107AC	8.0107AD	8.0107AE	8.0107AF	8.0107AG	8.0107AH	8.0107AI	8.0107AJ	8.0107AK	8.0107AL	8.0107AM	
8.0107BA	8.0107BB	8.0107BC	8.0107BD	8.0107BE	8.0107BF	8.0107BG	8.0107BH	8.0107BI	8.0107BJ	8.0701BK	8.0107BL	8.0107BM	8.0107BN
8.0107CA	8.0107CB	8.0107CC	8.0107CD	8.0107CE	8.0107CF	8.0107CG	8.0107CH	8.0107CI	8.0107CJ	8.0107CK	8.0107CL	8.0107CM	8.0107CN
8.0107DA	8.0107DB	8.0107DC	8.0107DD	8.0107DE	8.0107DF	8.0107DG	8.0107DH	8.0107DI	8.0107DJ	8.0107DK	8.0107DL	8.0107DM	8.0107DN
8.0107EA	8.0107EB	8.0107EC	8.0107ED	8.0107EE	8.0107EF	8.0107EG	8.0107EH	8.0107EI	8.0107EJ	8.0107EK	8.0107EL	8.0107EM	8.0107EN
8.0107FA	8.0107FB	8.0107FC	8.0107FD	8.0107FE	8.0107FF	8.0107FG	8.0107FH	8.0107FI	8.0107FJ	8.0107FK	8.0107FL	8.0107FM	8.0107FN
8.0107GA	8.0107GB	8.0107GC	8.0107GD	8.0107GE	8.0107GF	8.0107GG	8.0107GH	8.0107GI	8.0107GJ	8.0107GK	8.0107GL	8.0107GM	8.0107GN

Fig. 8.0107

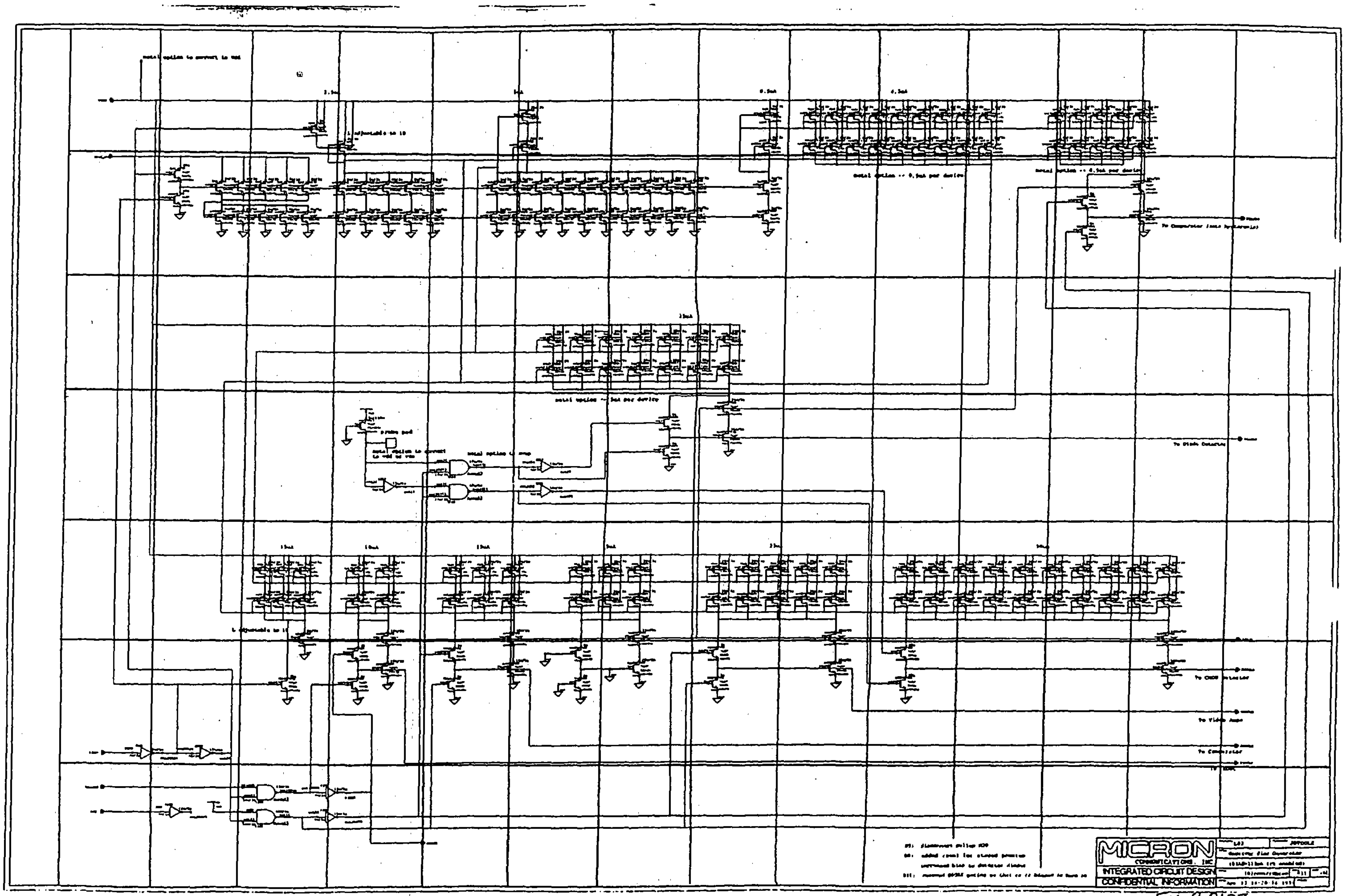

metal option to connect to Vdd
4.5uA
metal option -- 0.5uA per device
metal option -- 4.5uA per device
To Comparator (auto hysteresis)
metal option -- 1uA per device
probe pad
To Diode Detector
To CMOS Detector
To Video Amps
To Comparator
MICRON
COMMUNICATIONS, INC
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

FIG. R.0107

MI40-030

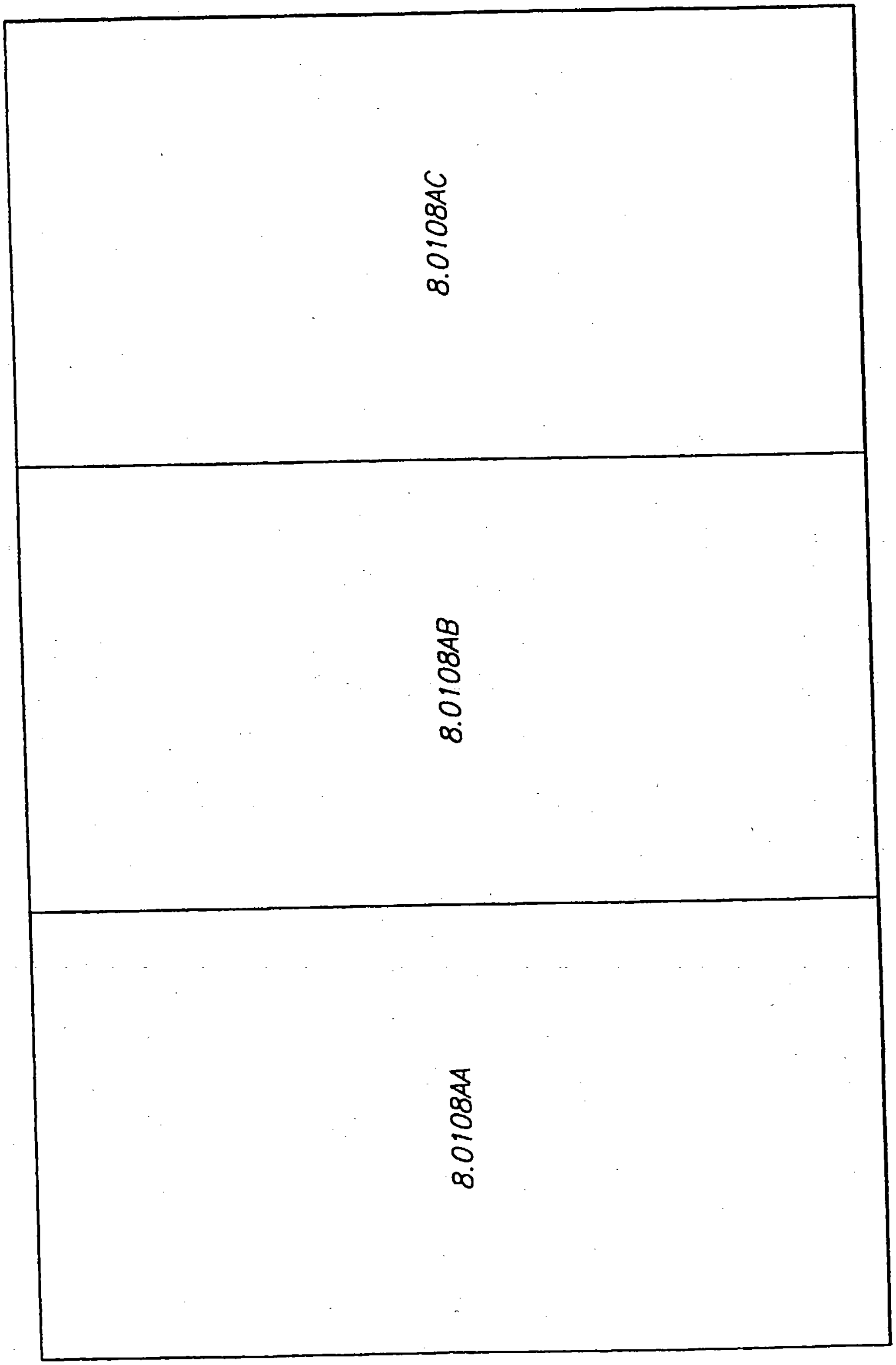


FIG. 8.0108

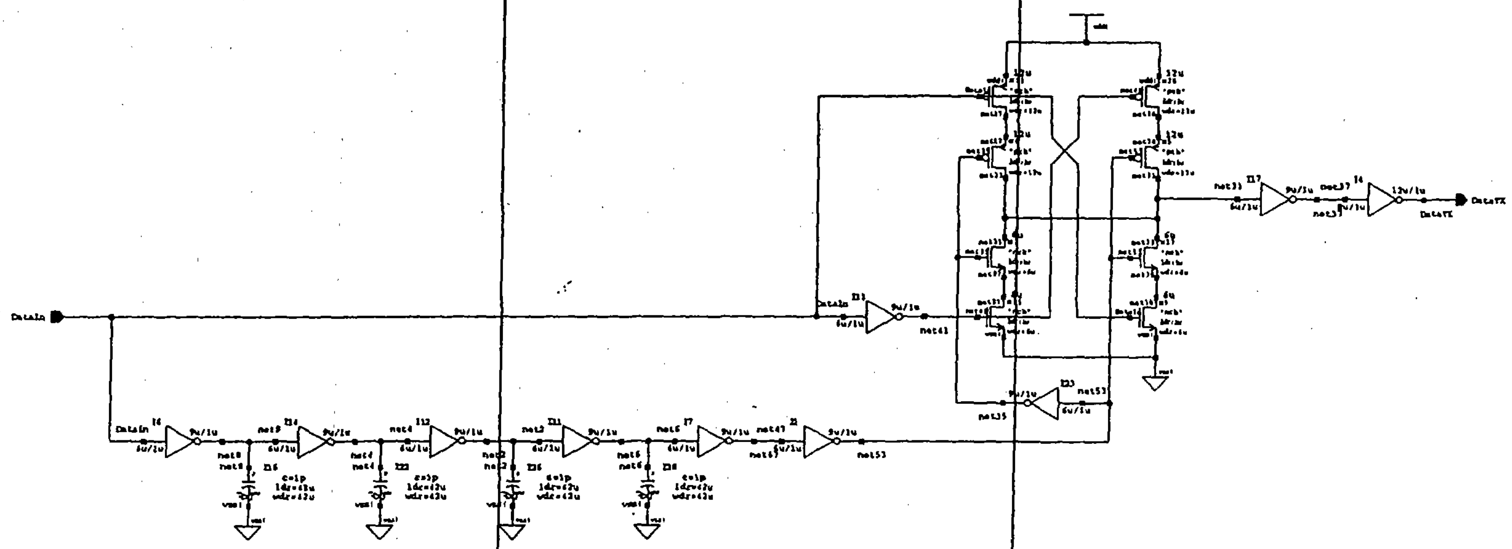


FIG. 8.0108

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03	JOTOOLE
Data Transition Detector	
Output Pulse Width = 40ns (nom	
103reva/datatx	B1 nil
Dec 14 17:11:15 1994	

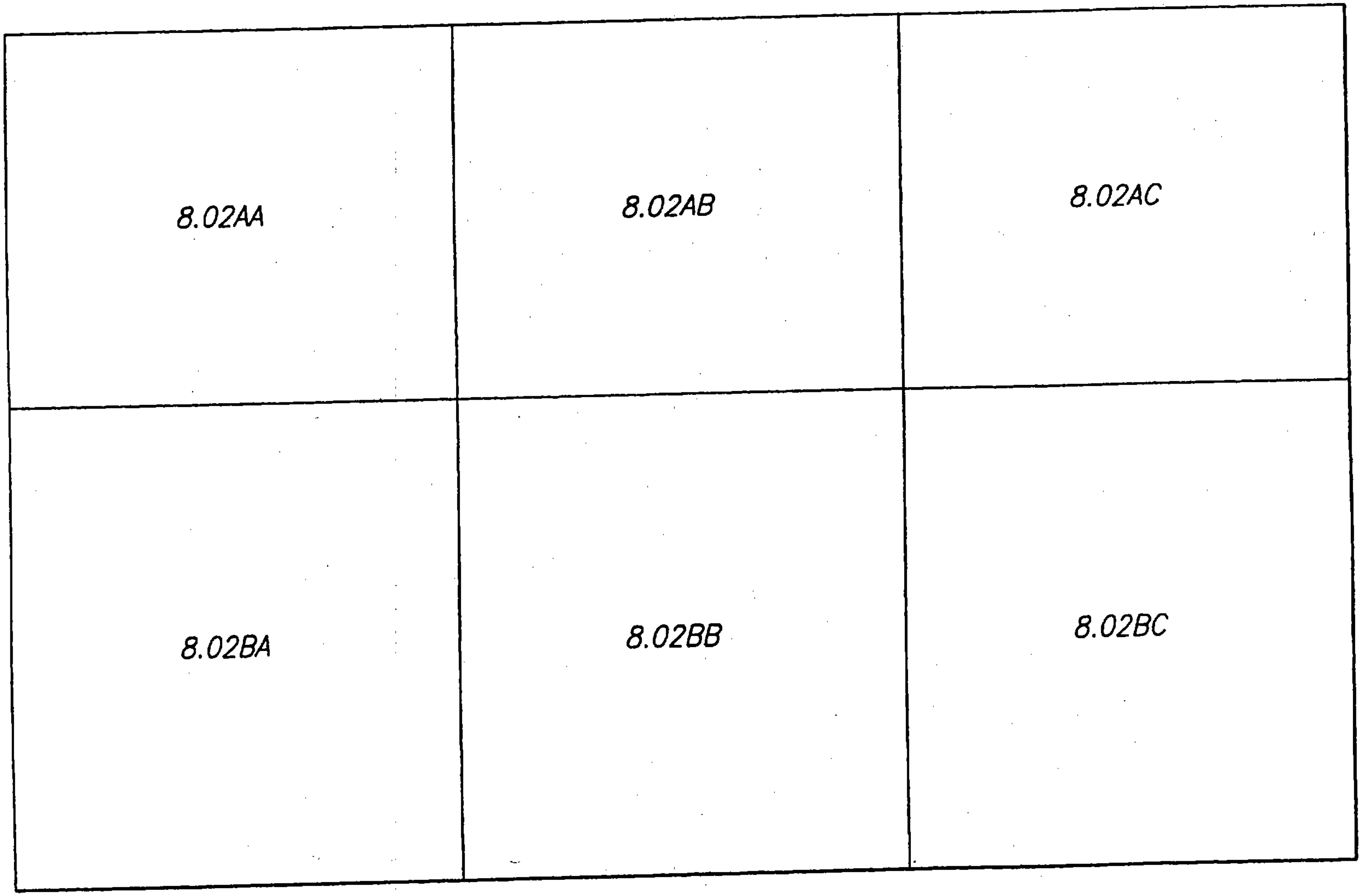


Fig 8.02

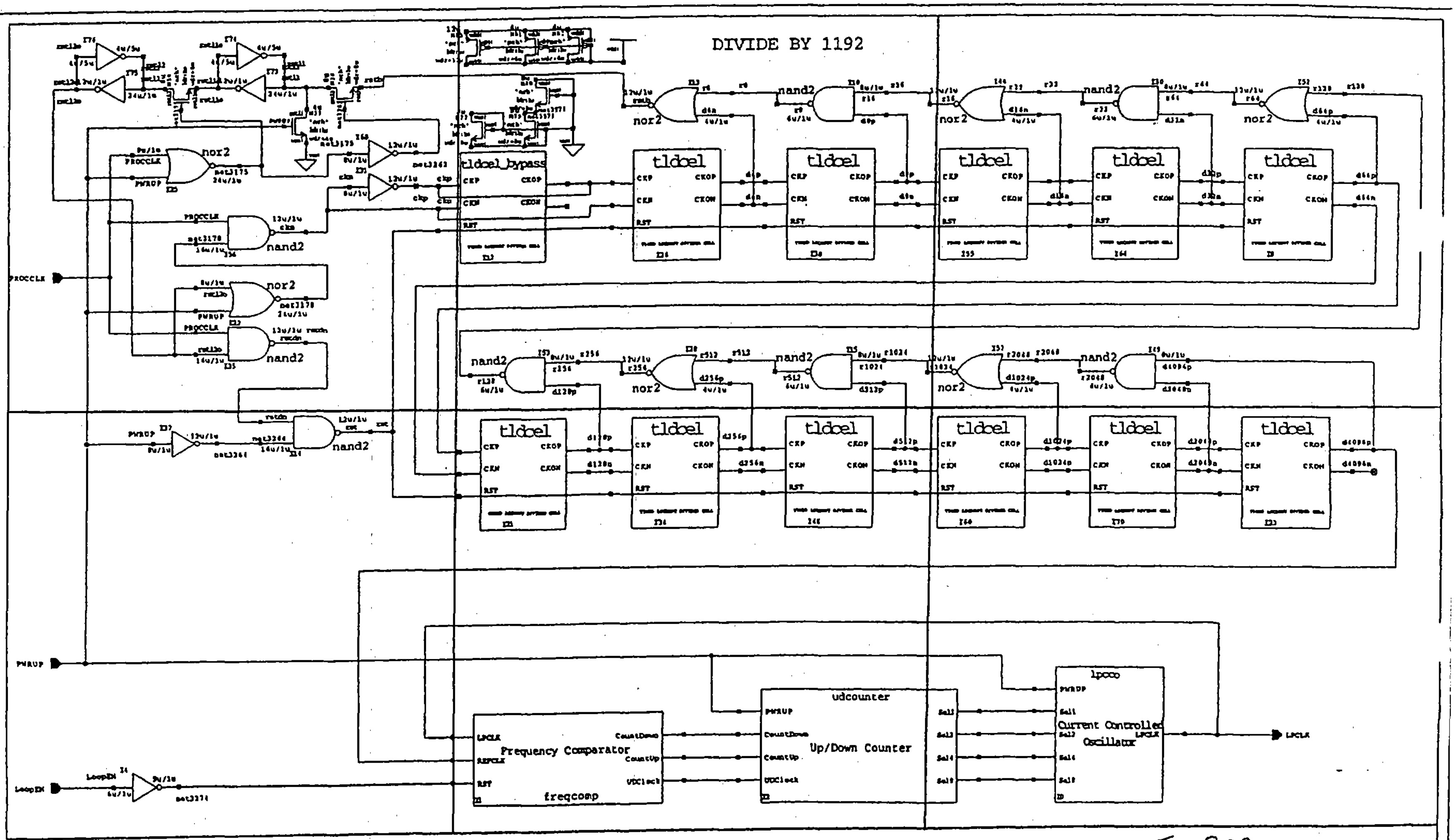


Fig. 8.02

B10: first divider stage bypassed

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
JOTOOLE
Low Power FLL (Isb=55nA typ)
fin=9.5375MHz/fout=8000Hz
103reva/lpfll
B10
nil
Mar 26 16:14:18 1996

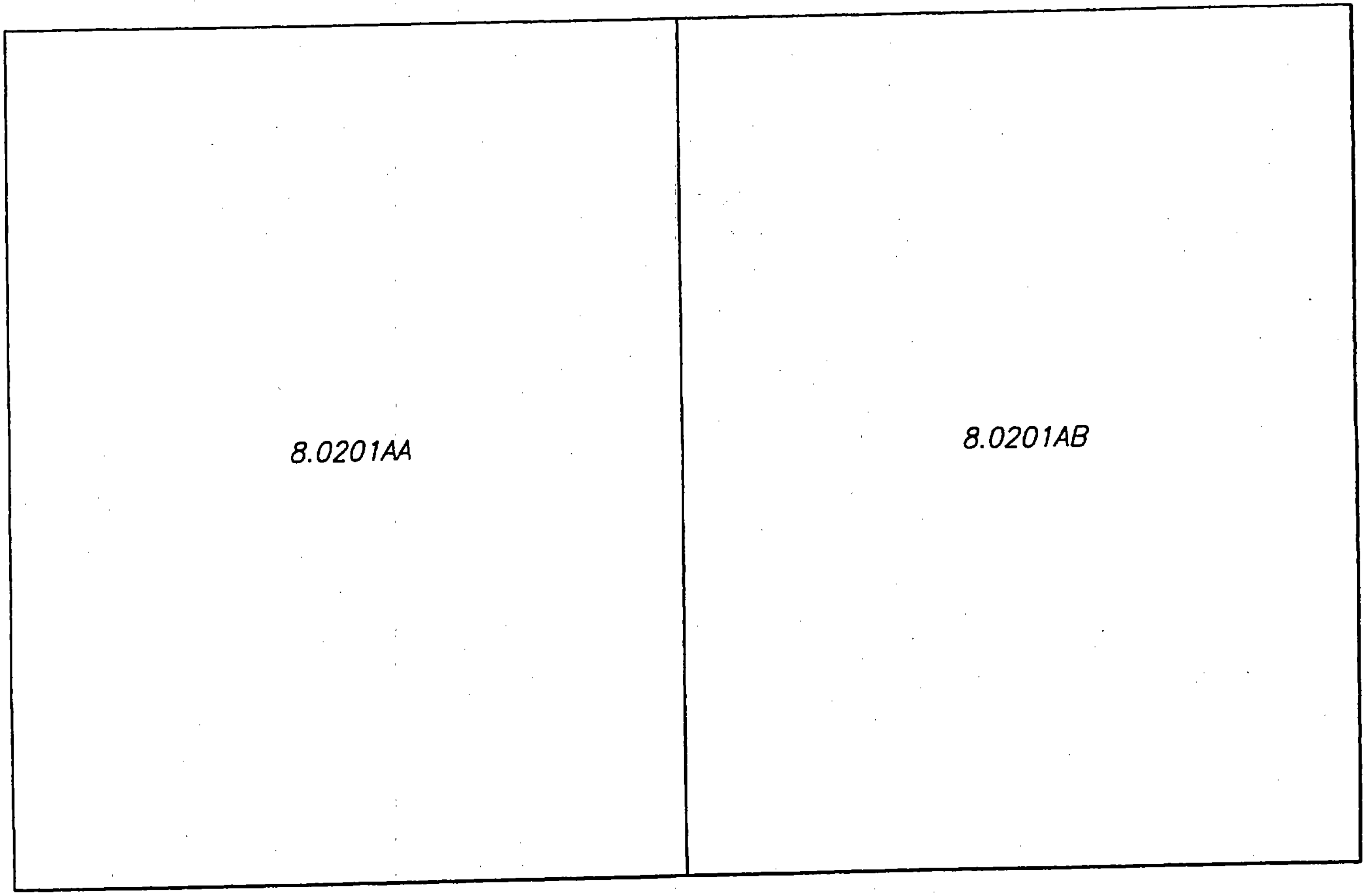


Fig 8.0201

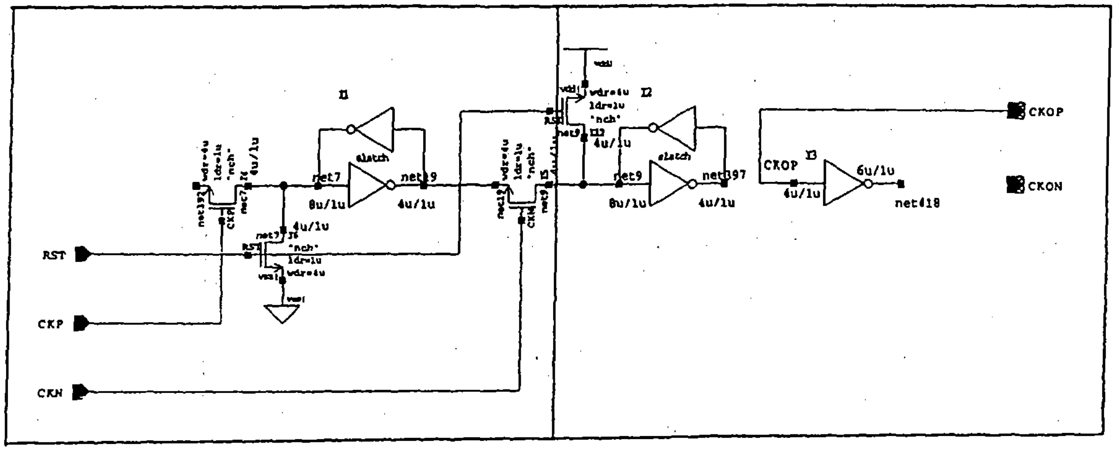


Fig. 8.0201

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Timed Lockout Divider Cell	
NAME: l03reva/tldcel_bypass	REV: B10 SIZE: A
DATE: Mar 26 13:54:47 1996	SHEET:

B10: new cell to bypass 1st counter stage

8.0202AA	8.0202AB	8.0202AC	8.0202AD
8.0202BA	8.0202BB	8.0202BC	8.0202BD
8.0202CA	8.0202CB	8.0202CC	8.0202CD

FIG. 8.0202

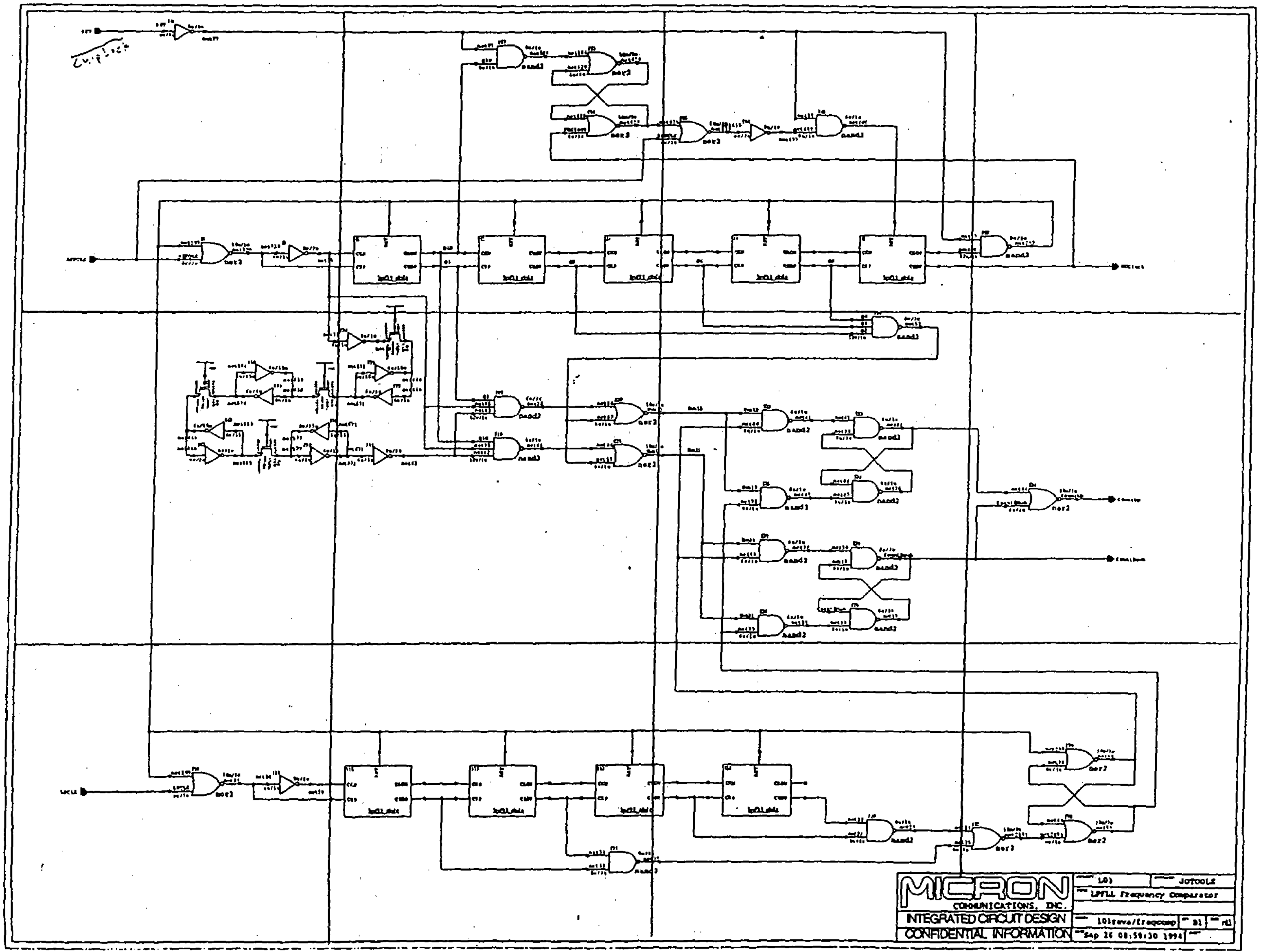
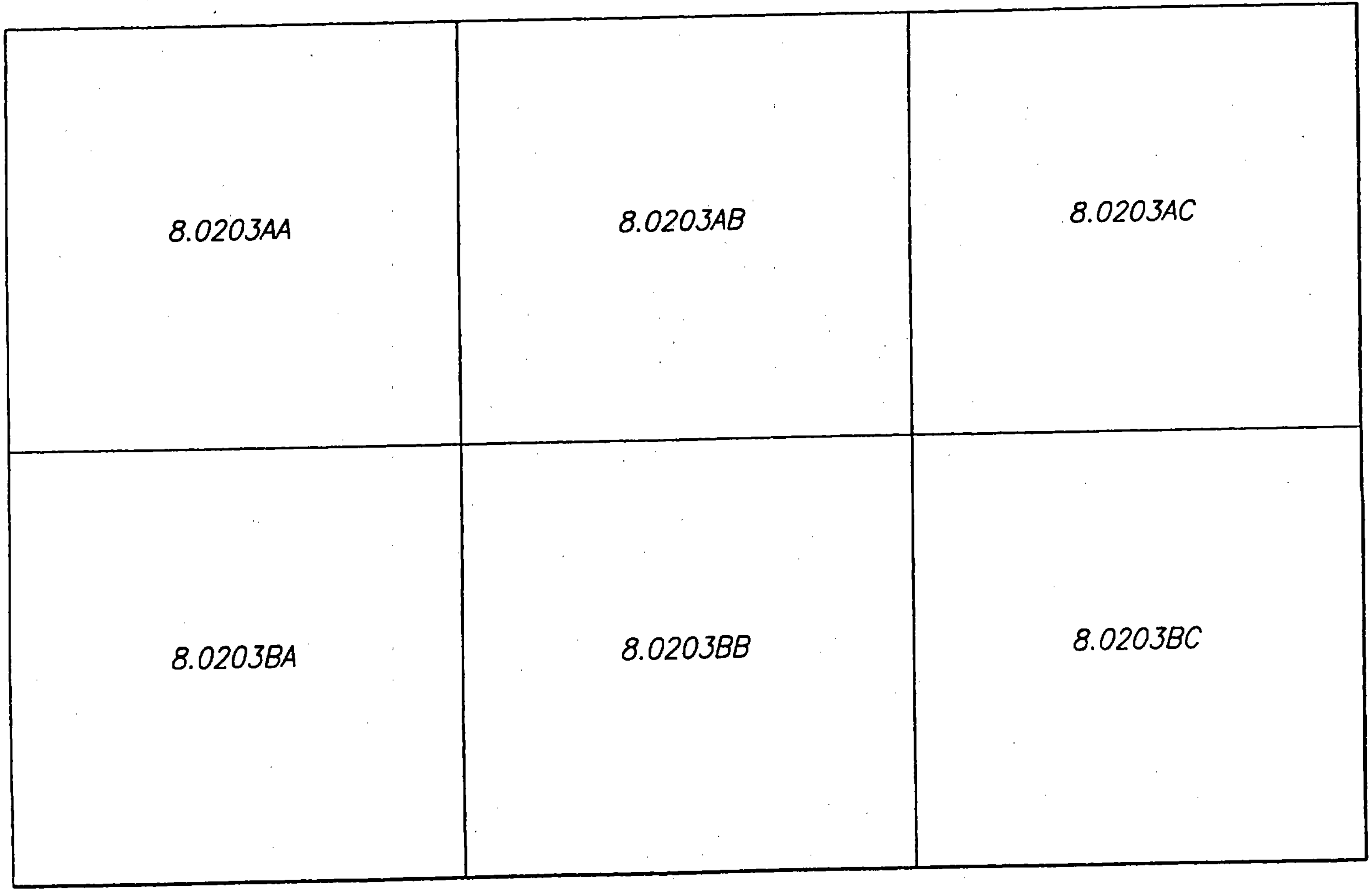
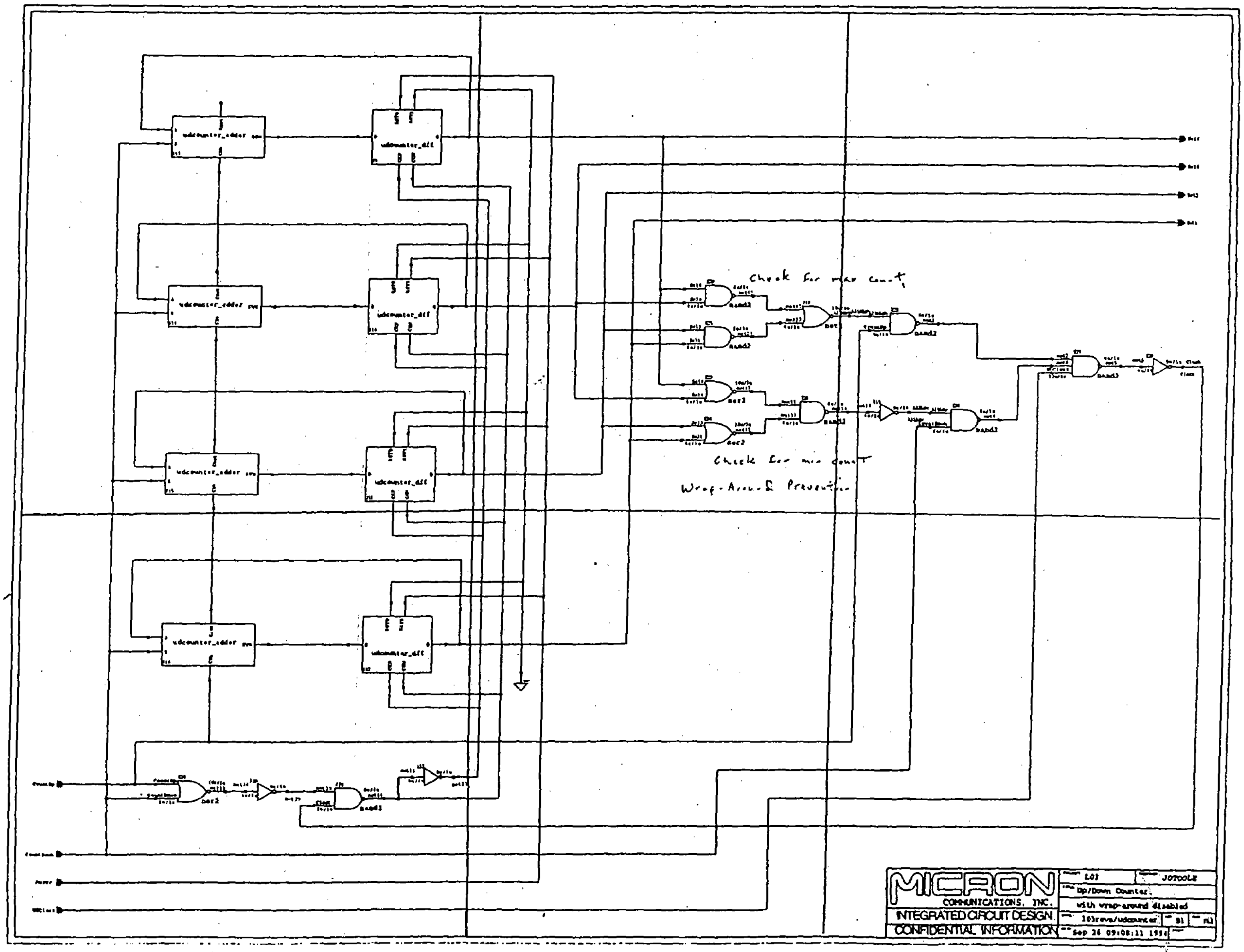

nor2
nand2
nand3
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
LO)
JOTOOLS
LPFLL Frequency Comparator
10)reva/freqcomp
B1
r1
Sep 26 08:58:30 1994

FiG. 8.0202



8.0203AA	8.0203AB	8.0203AC
8.0203BA	8.0203BB	8.0203BC

FIG. 8.0203



Check for max count

Check for min count

Wrap-Around Prevention

FIG. 8.0203

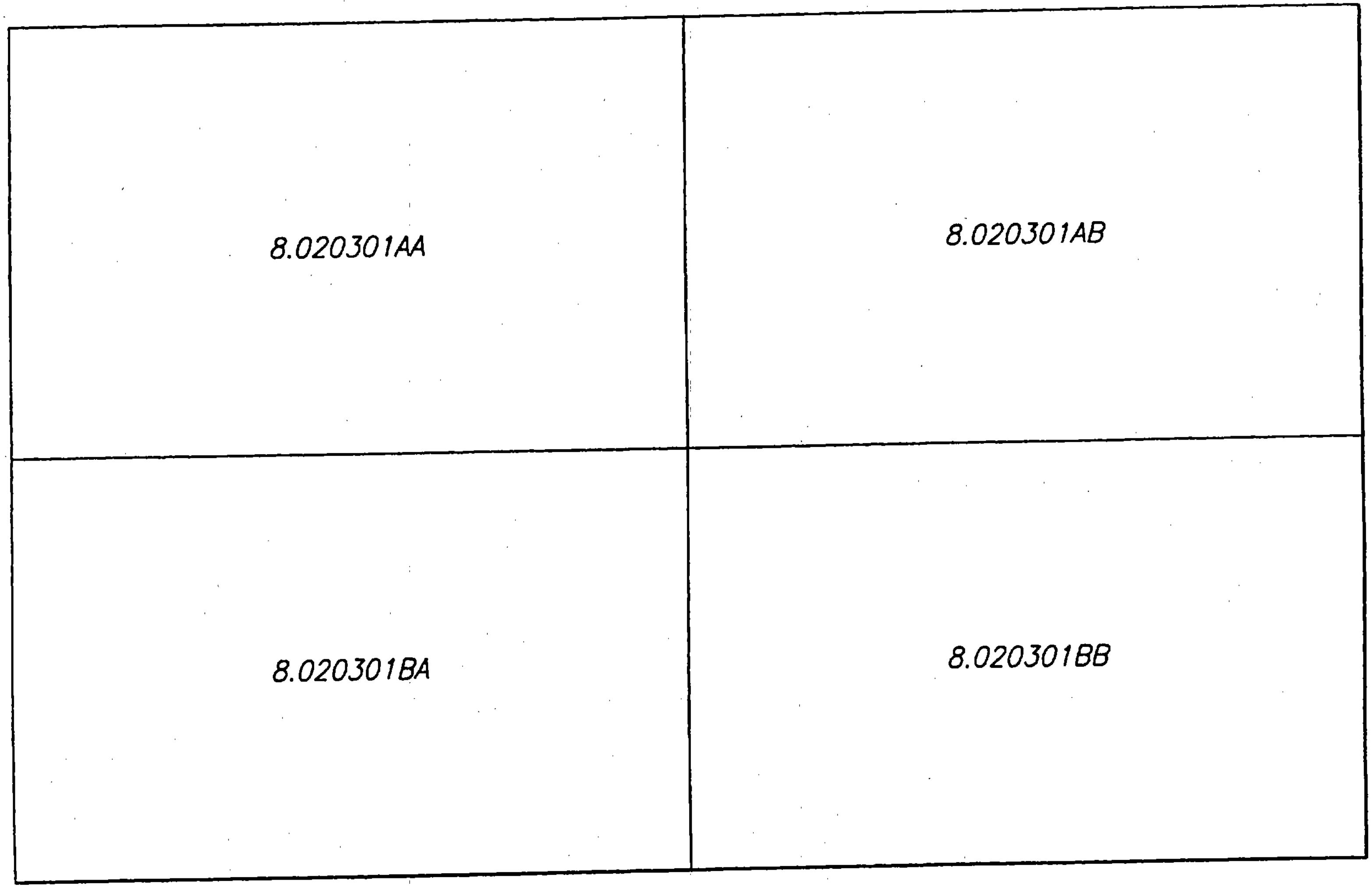
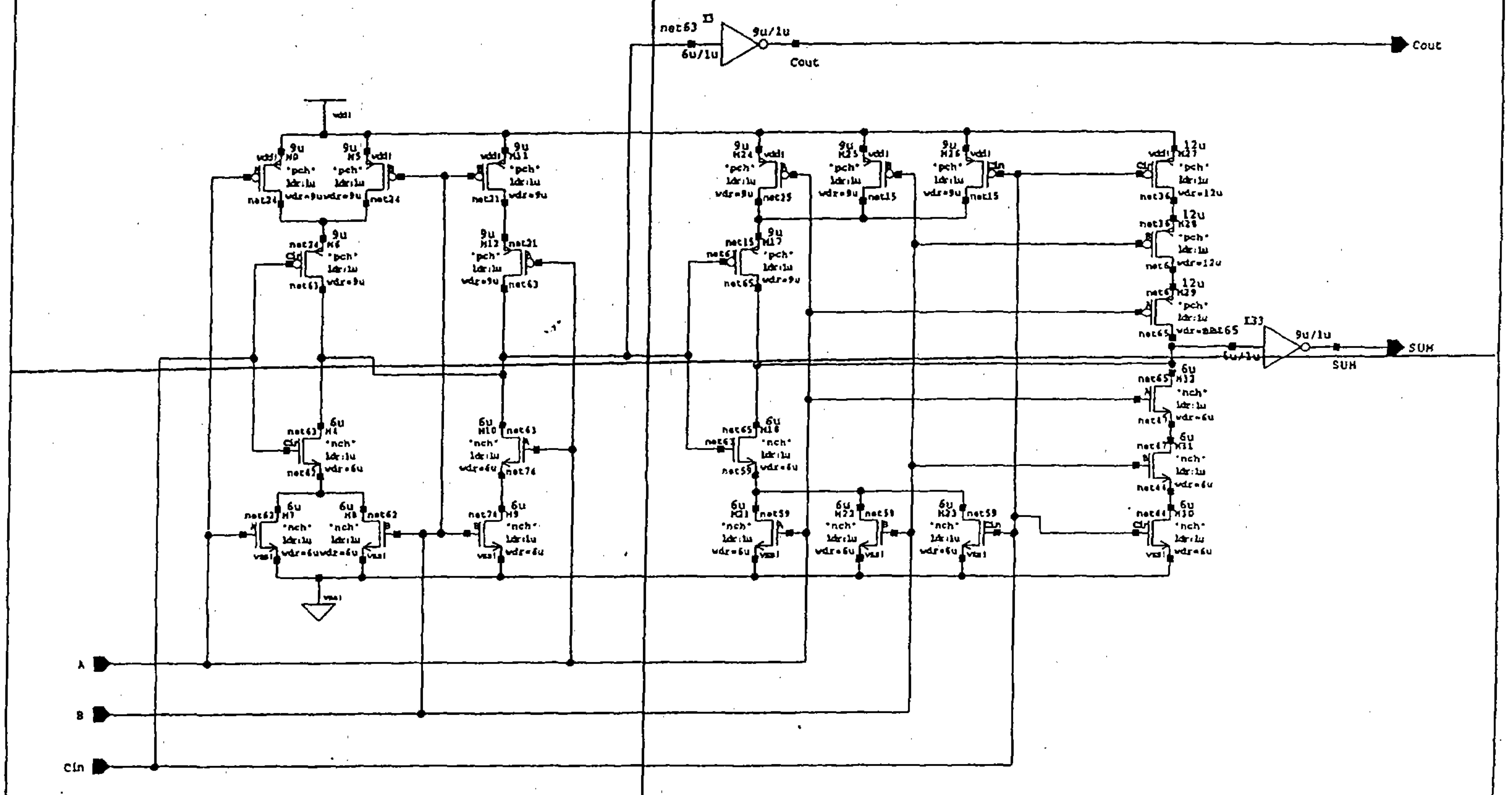


Fig 8.020301



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: UD Counter Adder
NAME: l03reva/udcounter_adder
REV: B1
SIZE: A
DATE: Sep 26 09:08:56 1994
SHEET:

FIG. 8.020301

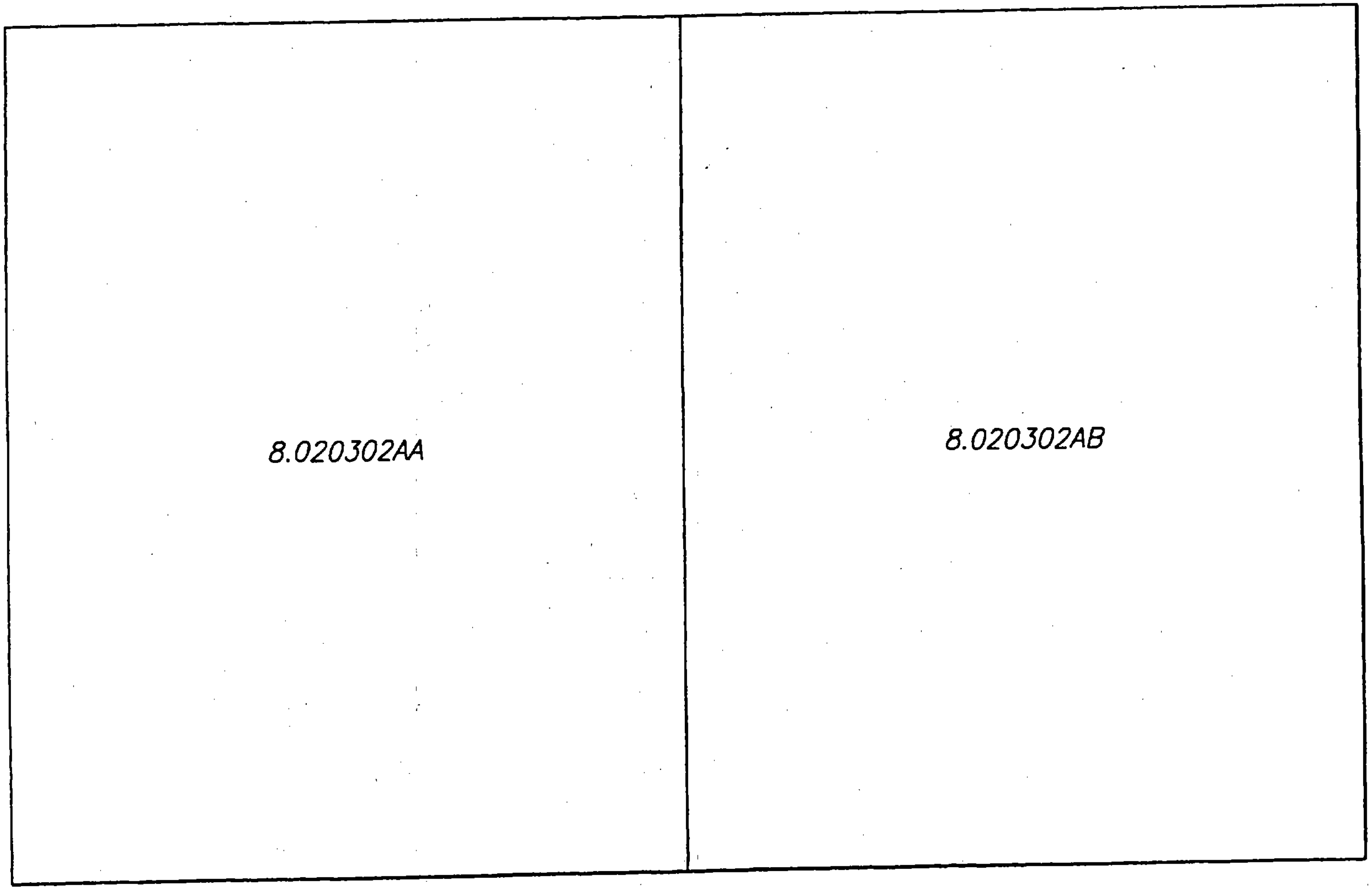
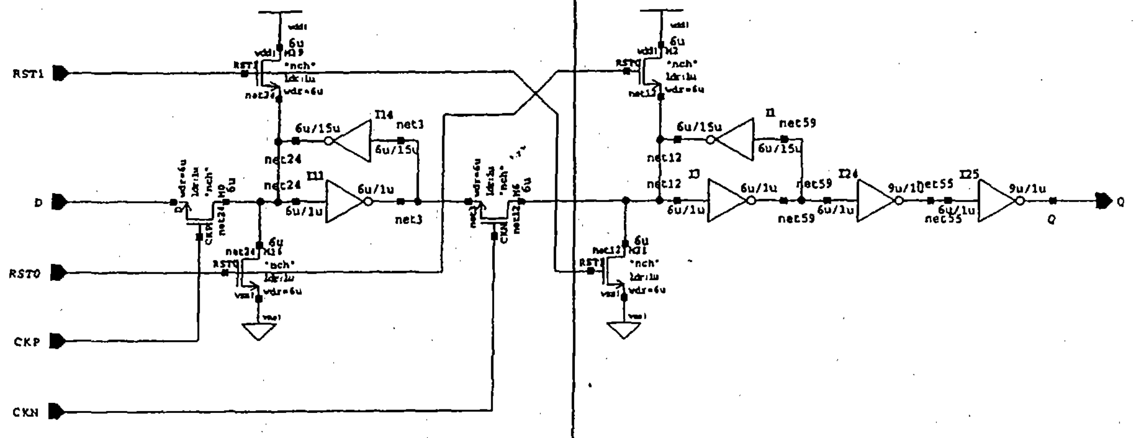


Fig. 8.020302



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: LPFLL U/D Counter D Flip Flop	
NAME: l03reva/udcounter_dff	REV: B1 SIZE: A
DATE: Sep 26 09:09:40 1994	SHEET:

FIG. 8.020302

8.0204AA	8.0204AB	8.0204AC	8.0204AD	8.0204AE	8.0204AF	8.0204AG	8.0204AH	8.0204AI	8.0204AJ
8.0204BA	8.0204BB	8.0204BC	8.0204BD	8.0204BE	8.0204BF	8.0204BG	8.0204BH	8.0204BI	8.0204BJ
8.0204CA	8.0204CB	8.0204CC	8.0204CD	8.0204CE	8.0204CF	8.0204CG	8.0204CH	8.0204CI	
8.0204DA	8.0204DB	8.0204DC	8.0204DD	8.0204DE	8.0204DF	8.0204DG	8.0204DH	8.0204DI	
8.0204EA	8.0204EB	8.0204EC	8.0204ED	8.0204EE	8.0204EF	8.0204EG	8.0204EH	8.0204EI	8.0204EJ

FIG 8.0204

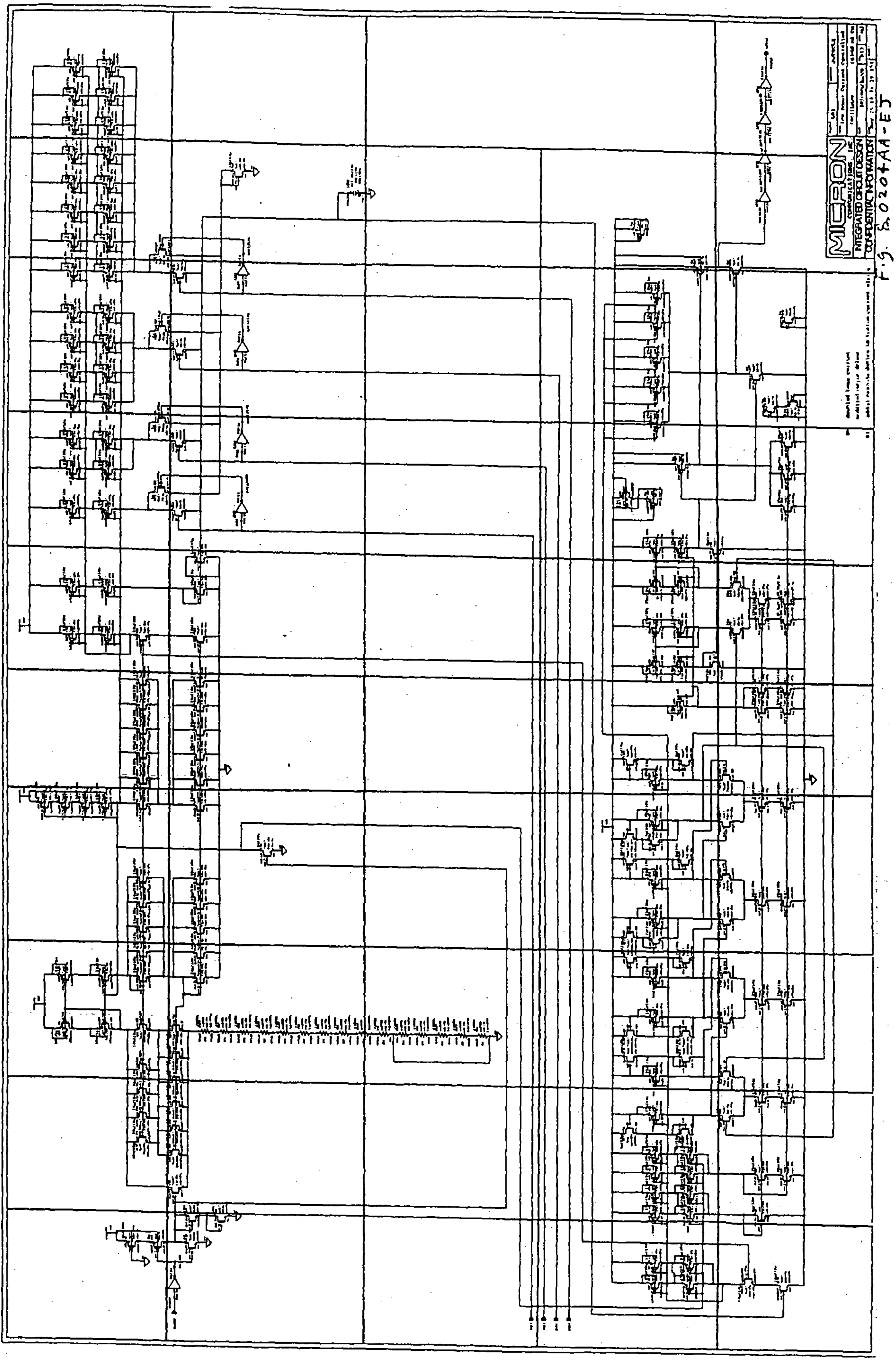
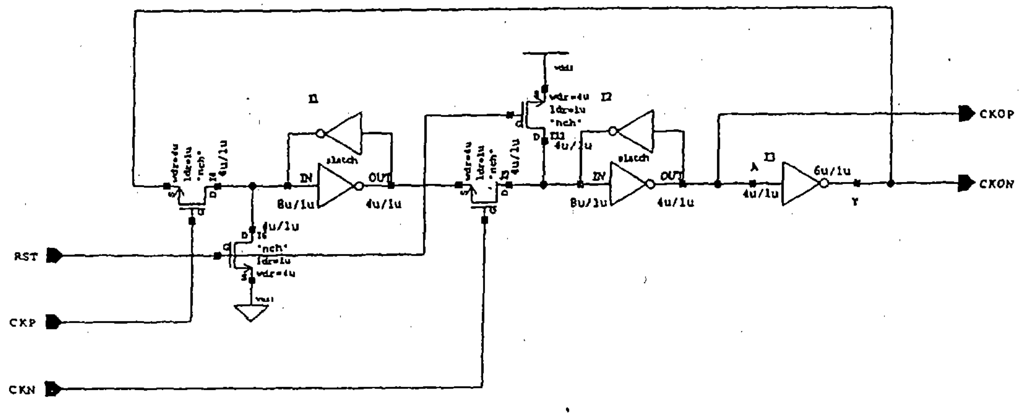


Fig. 6 0204AA-EJ



12/29/92

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: Timed Lockout Divider Cell
NAME: 103reva/tldcel
REV:
SIZE: A
DATE: Sep 22 15:26:56 1994
SHEET:

~~[illegible]~~
F168.0205

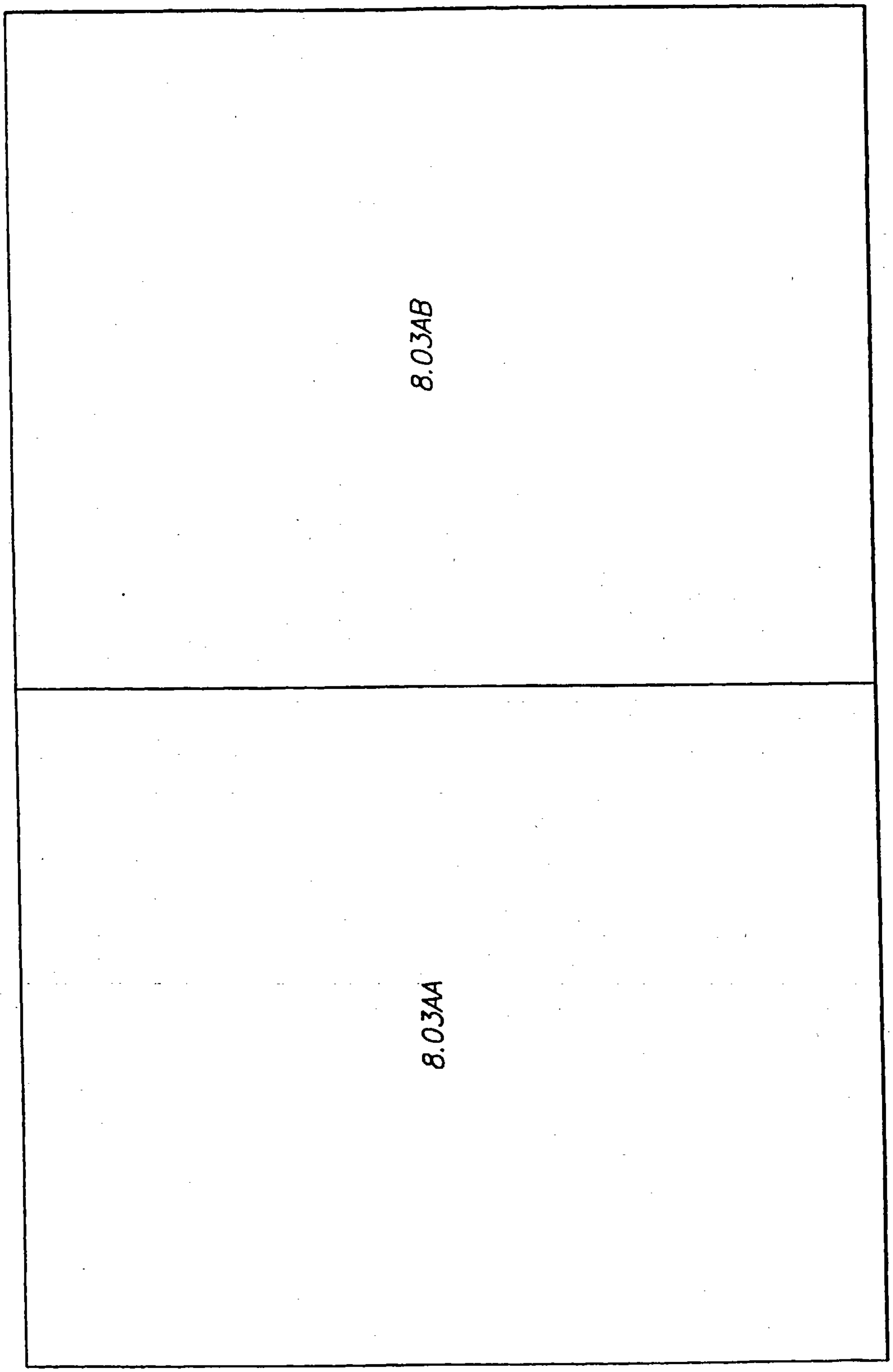
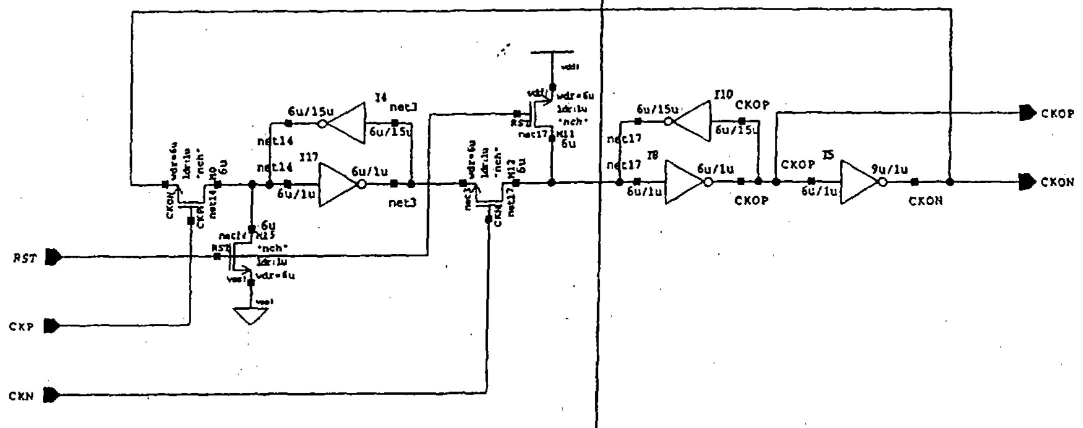


FIG. 8.03



MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: LPFLL Counter Bit	
NAME: 103reva/lpfll_cbit	REV: B1 SIZE: A
DATE: Sep 26 08:59:33 1994	SHEET:

FIG. 8.03

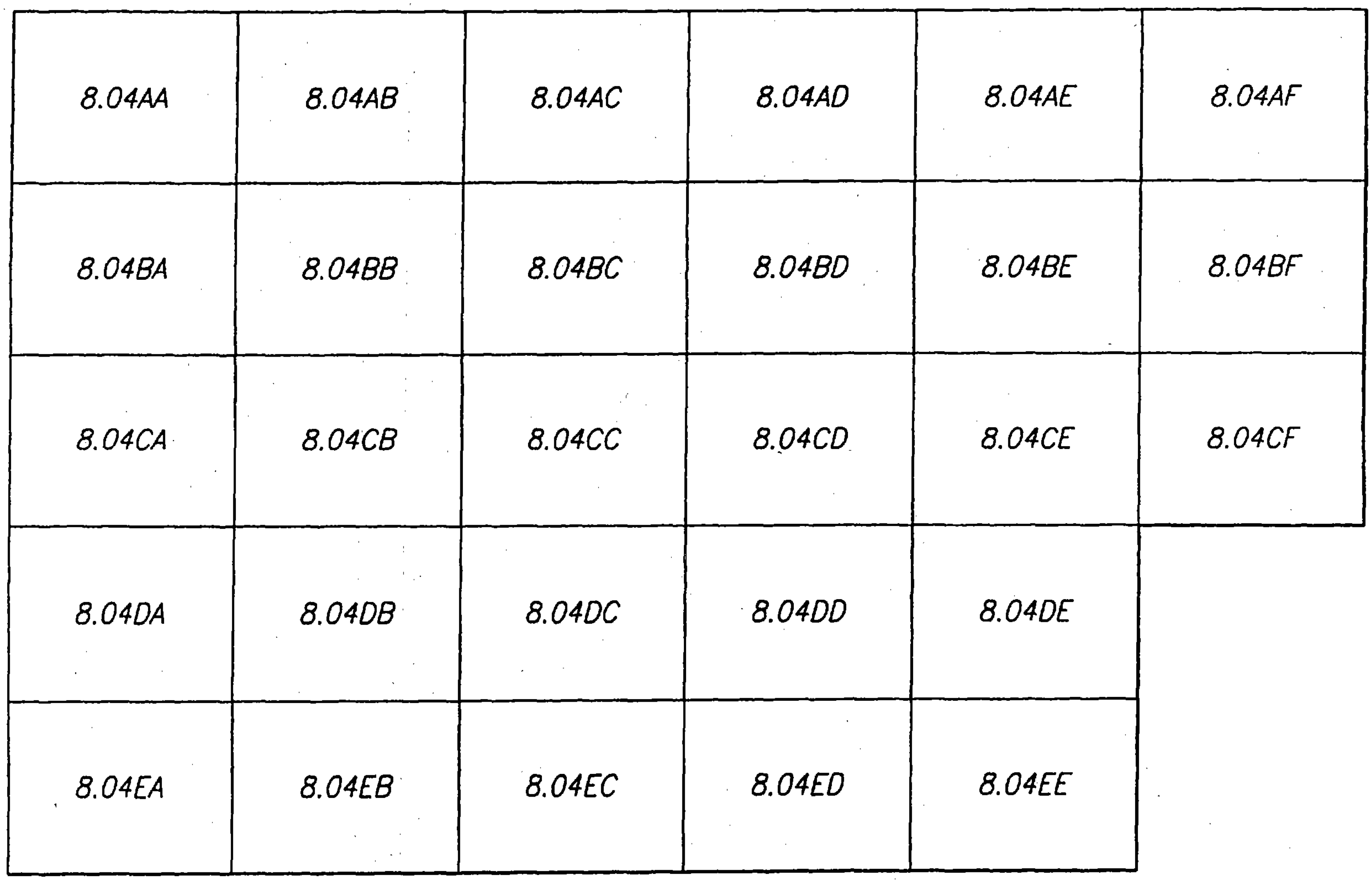

8.04AA
8.04AB
8.04AC
8.04AD
8.04AE
8.04AF
8.04BA
8.04BB
8.04BC
8.04BD
8.04BE
8.04BF
8.04CA
8.04CB
8.04CC
8.04CD
8.04CE
8.04CF
8.04DA
8.04DB
8.04DC
8.04DD
8.04DE
8.04EA
8.04EB
8.04EC
8.04ED
8.04EE

Fig. 8.04

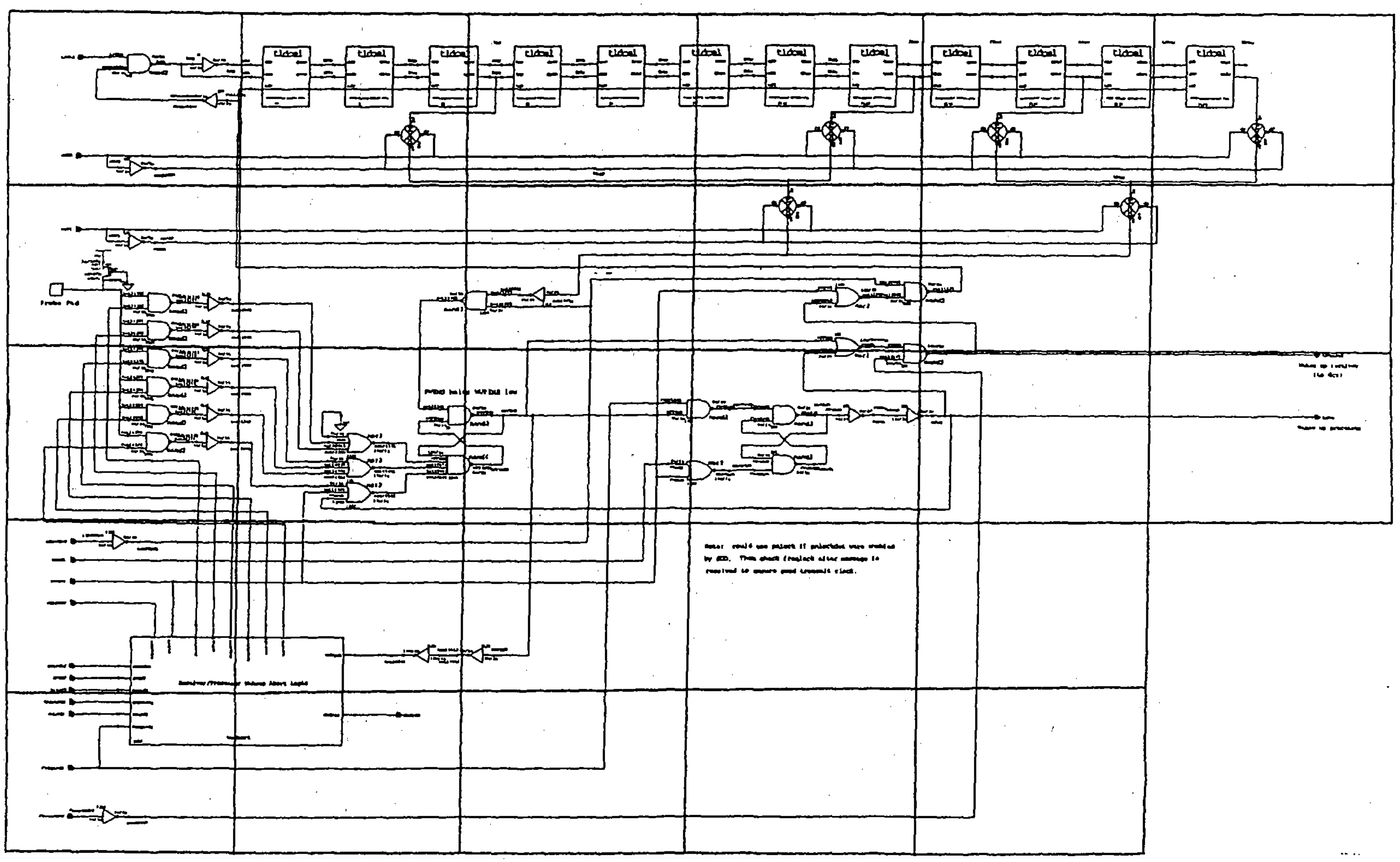


FIG. 8.04

MICRON
COMMUNICATIONS, INC
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

8.0401AA	8.0401AB	8.0401AC	8.0401AD	8.0401AE
8.0401BA	8.0401BB	8.0401BC	8.0401BD	8.0401BE
8.0401CA	8.0401CB	8.0401CC	8.0401CD	8.0401CE
8.0401DA	8.0401DB	8.0401DC	8.0401DD	8.0401DE

Fig. 8.0401

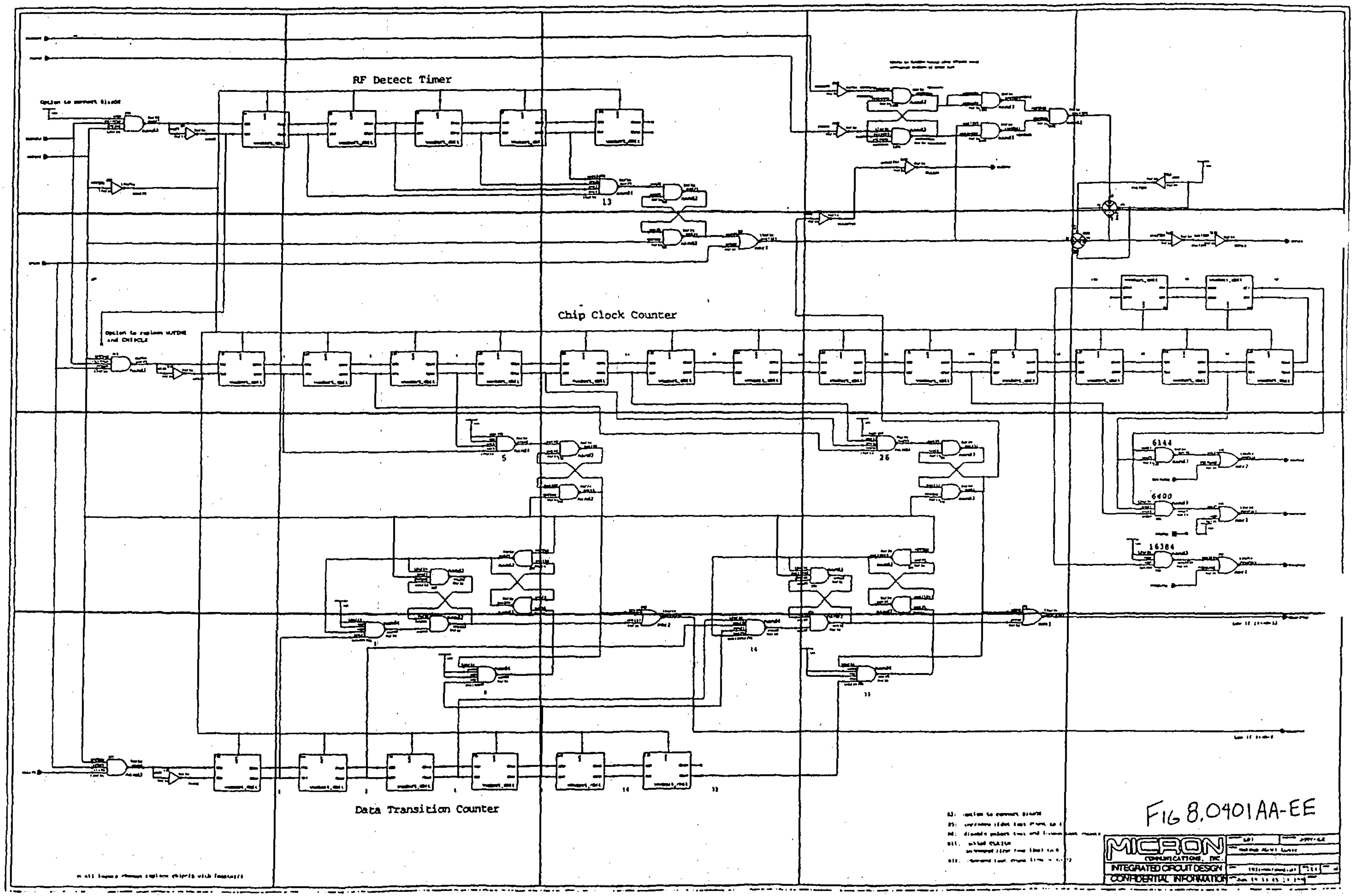


FIG 8.0401AA-EE

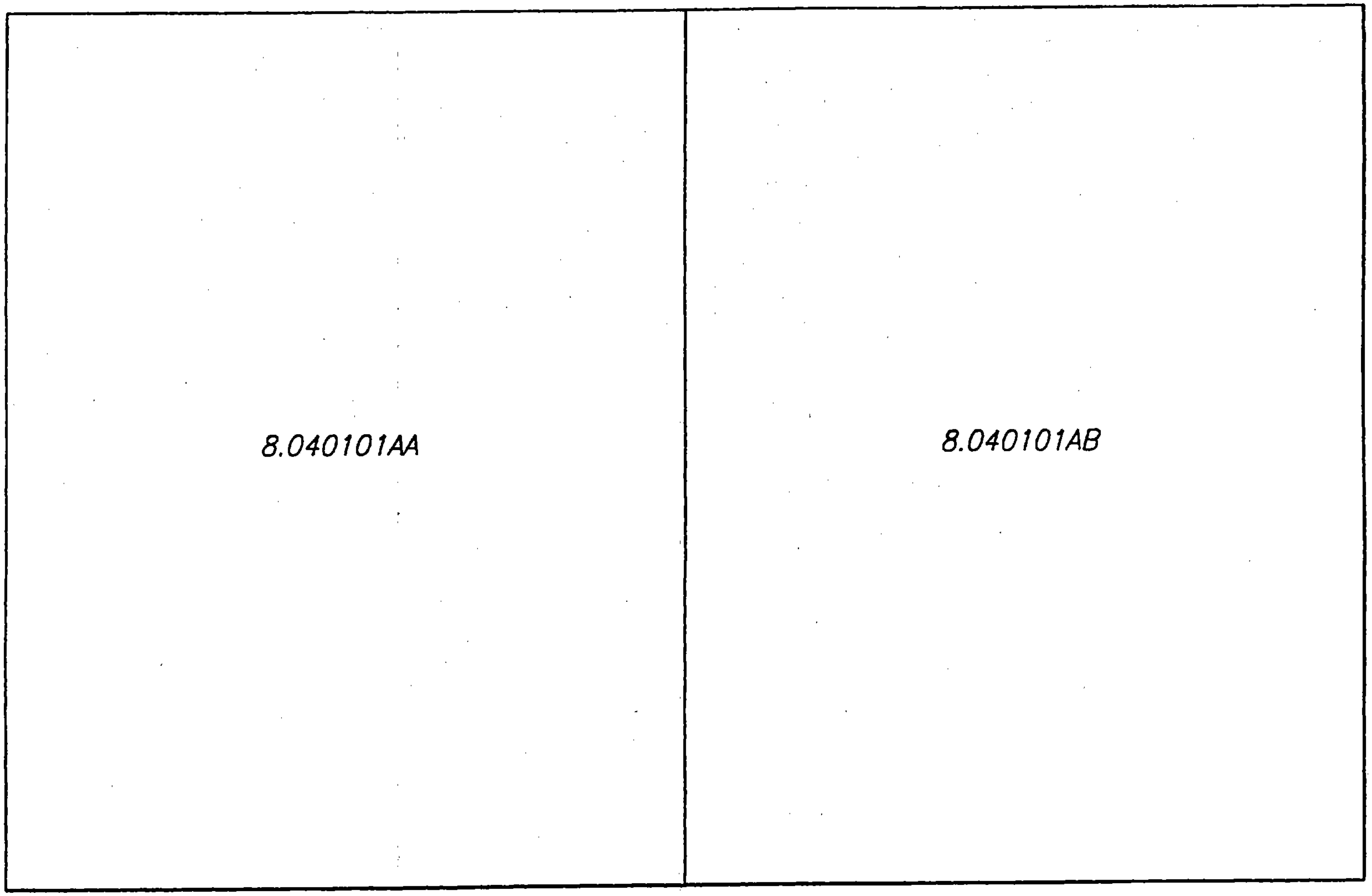
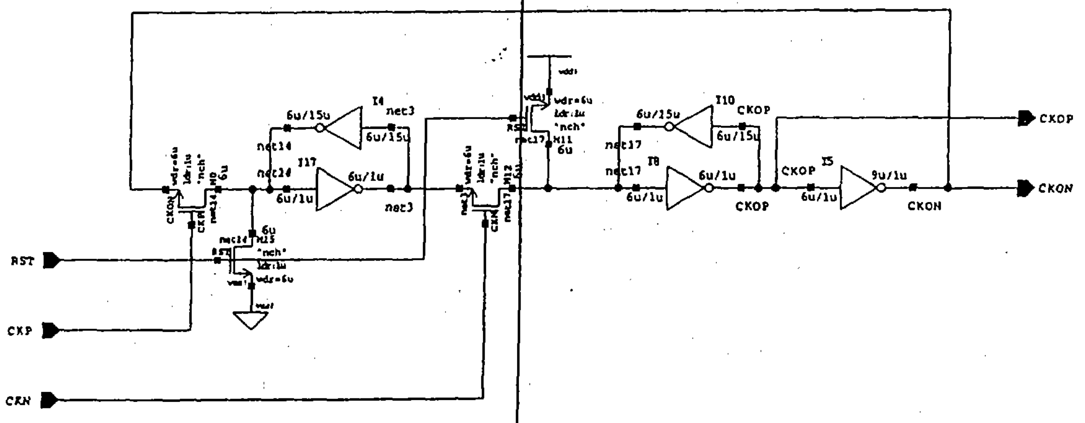


Fig 8.040101



MICRON

COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

PROJECT: L03			DESIGNER: JOTOOLE		
TITLE: Wakeup Abort Logic Counter Bit					
NAME: l03reva/wuabort_cbit		REV: B1		SIZE: A	
DATE: Sep 26 08:40:51 1994			SHEET:		

FIG. 8.090101

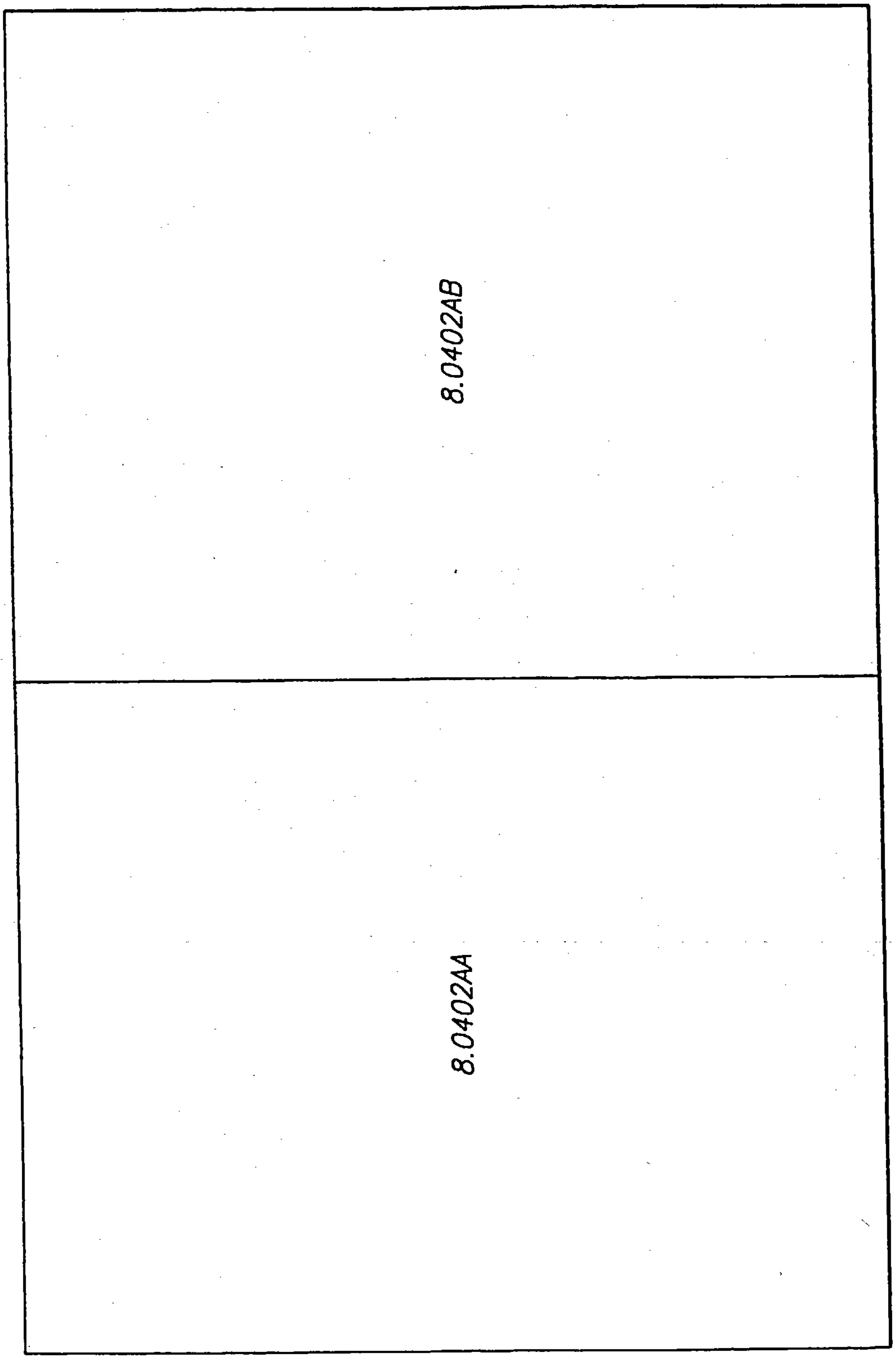
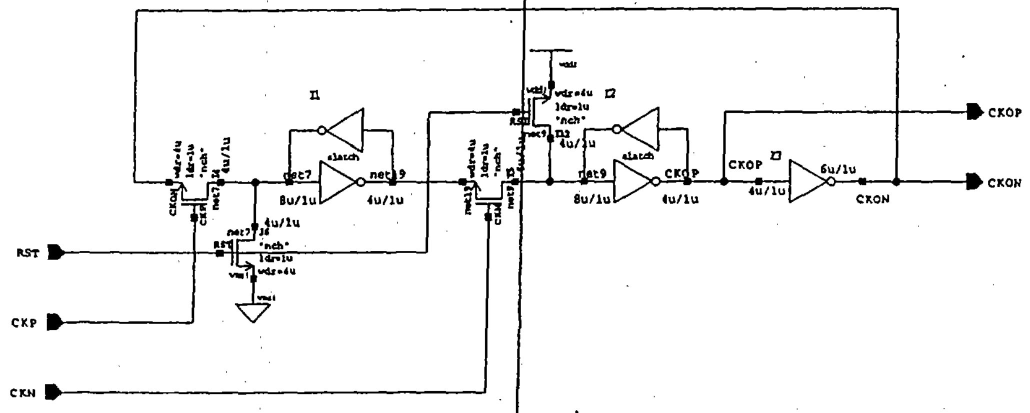


Fig 8.0402



12/29/92

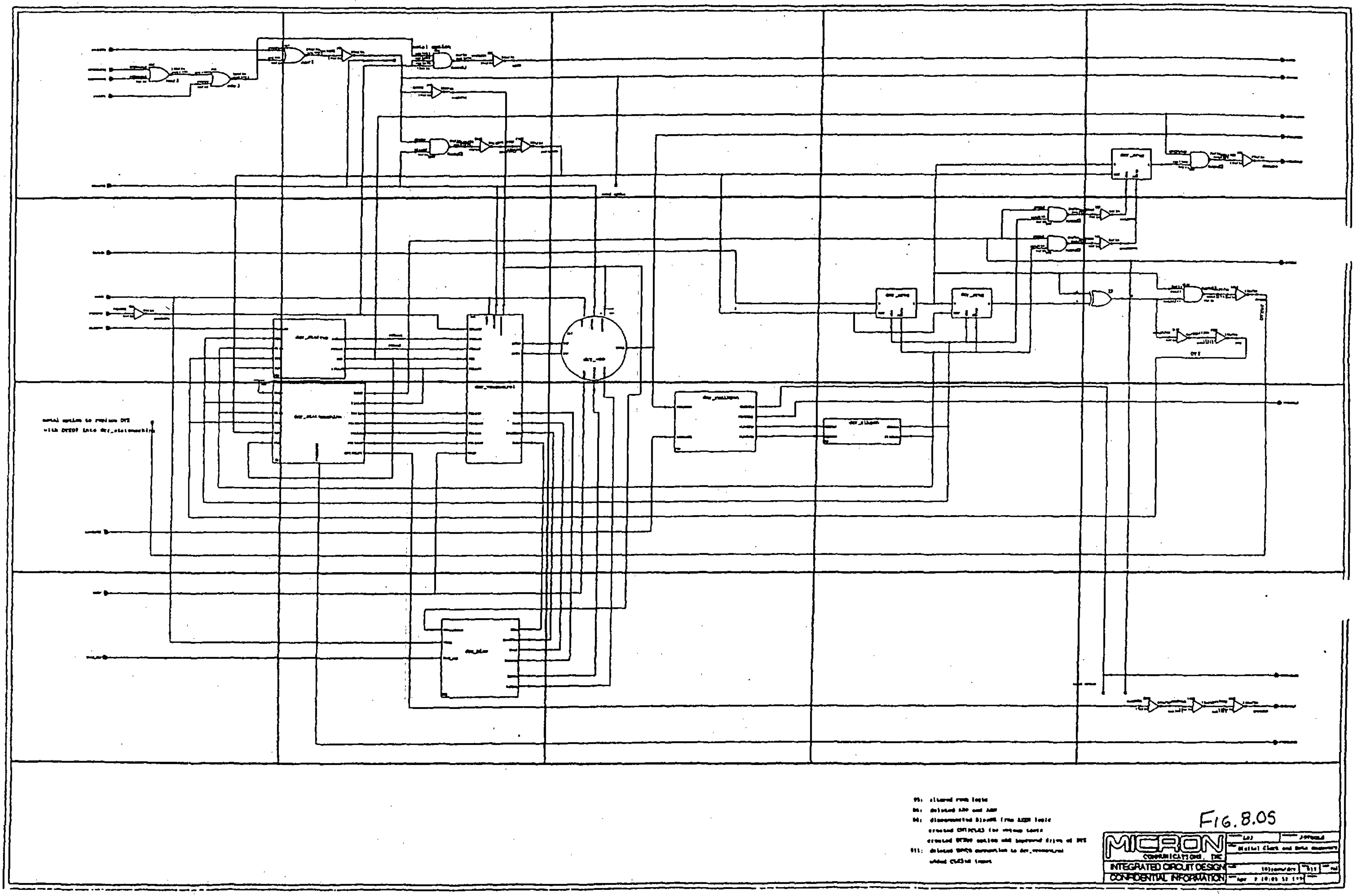
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: Timed Lockout Divider Cell
NAME: 103reva/tldcel
REV:
SIZE: A
DATE: Sep 22 15:26:56 1994
SHEET:

FIG. 8.0402

8.05AA	8.05AB	8.05AC	8.05AD	8.05AE
8.05BA	8.05BB	8.05BC	8.05BD	8.05BE
8.05CA	8.05CB	8.05CC	8.05CD	8.05CE
8.05DA	8.05DB	8.05DC	8.05DD	8.05DE

Fig 8.05


metal option to replace DYZ
with DFZOF into dcr_statemachine
dcr_vco
dcr_statemachine
dcr_vcocontrol
dcr_pulsegen
dcr_blkgen
dcr_blim
dcr_dffp
05: altered [illegible] logic
06: deleted [illegible] and [illegible]
08: disconnected [illegible] from [illegible] logic
created [illegible] for [illegible] tests
created [illegible] option and improved drive of DYZ
011: deleted [illegible] connection to dcr_vcocontrol
added [illegible] input
MICRON
COMMUNICATIONS, INC
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
Digital Clock and Data Recovery

F16. 8.05

8.0501AA	8.0501AB	8.0501AC	8.0501AD	8.0501AE
8.0501BA	8.0501BB	8.0501BC	8.0501BD	8.0501BE

Fig 8.0501

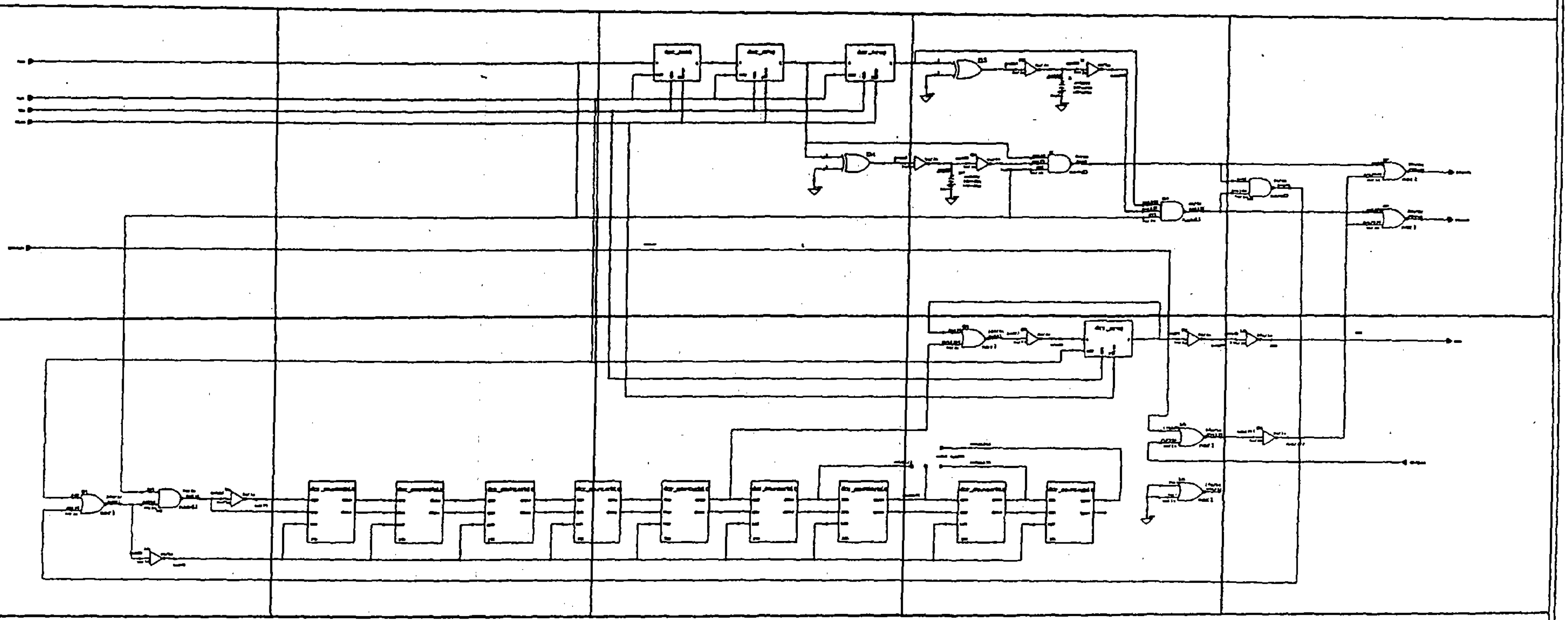


FIG. 8.0501

MICRON
COMMUNICATIONS, INC
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

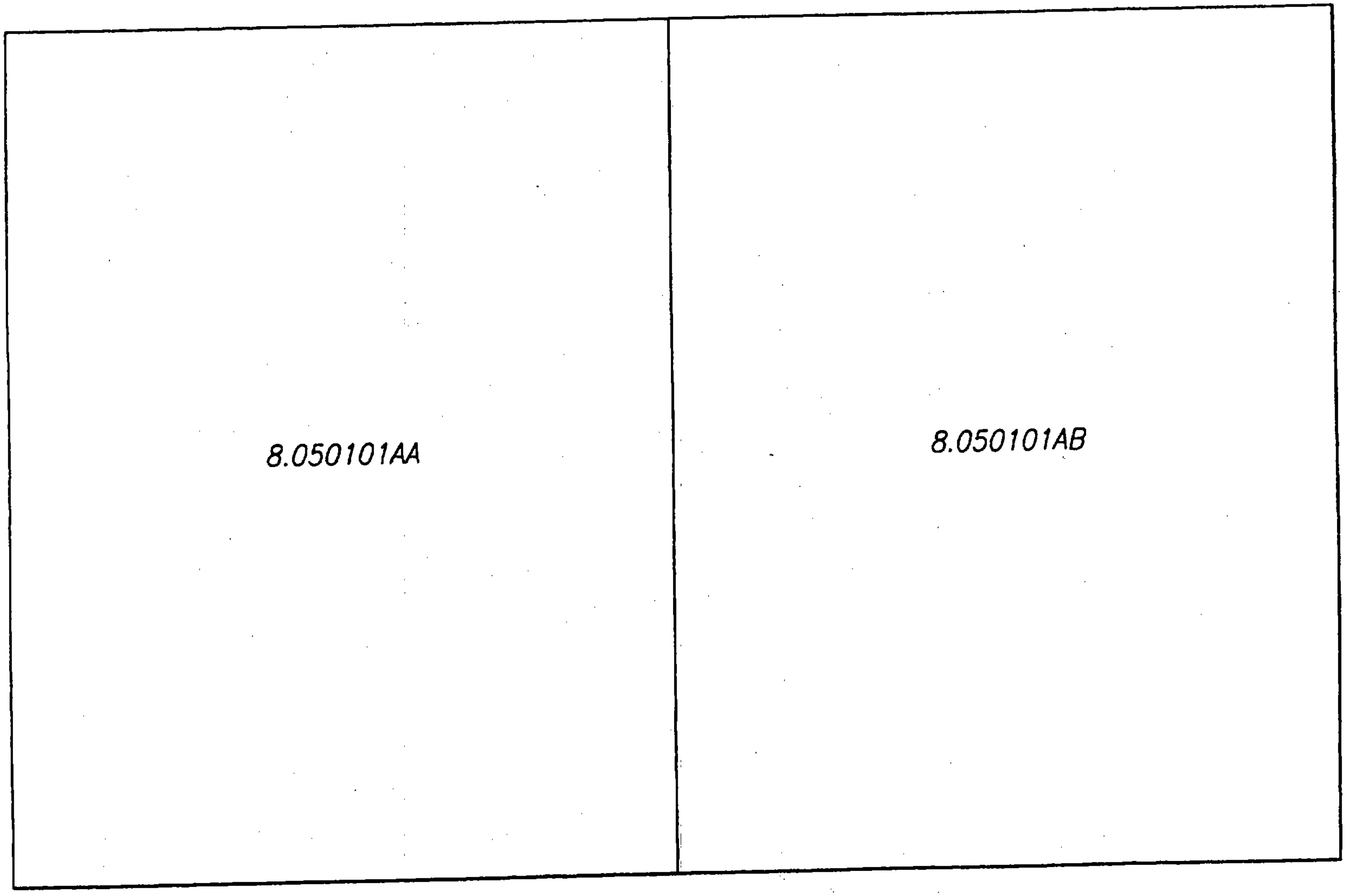
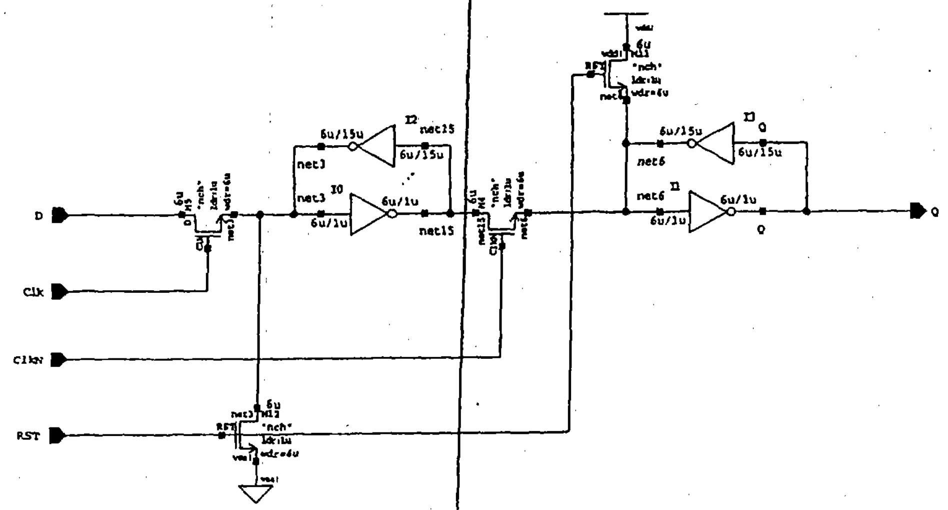


FIG 8.050101



MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: LC3		DESIGNER: JOTOOLE	
TITLE: Shift Register Cell			
NAME: 103reva/dcr_sreg		REV: B1	SIZE: A
DATE: Aug 31 14:25:03 1994		SHEET:	

FIG. 8.050101

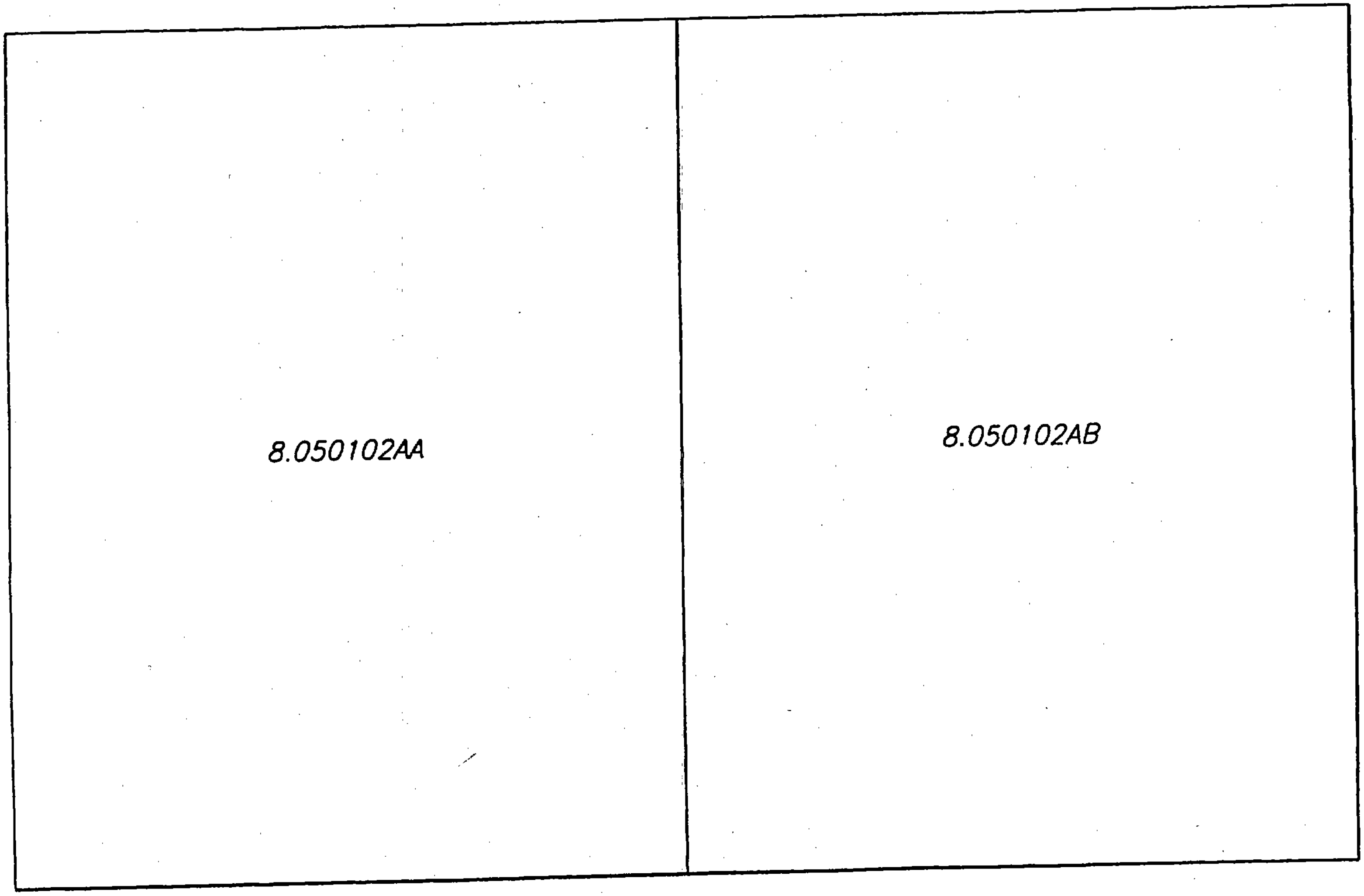
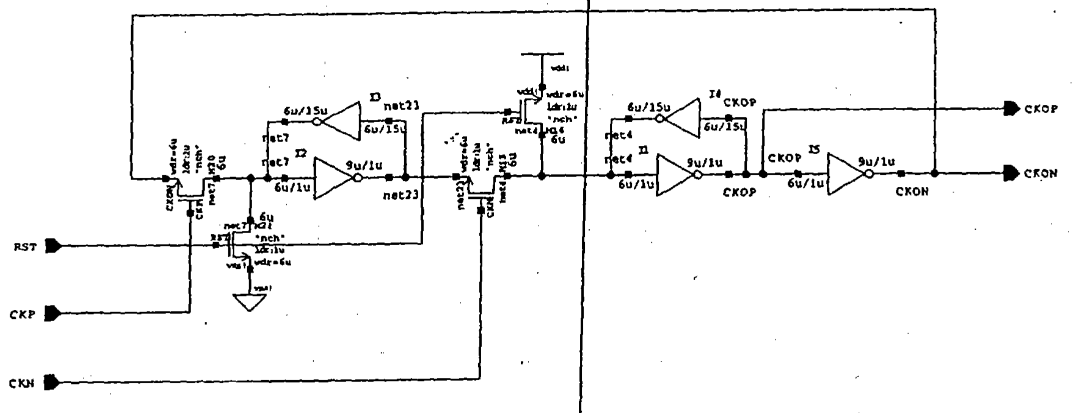


Fig 8.050102



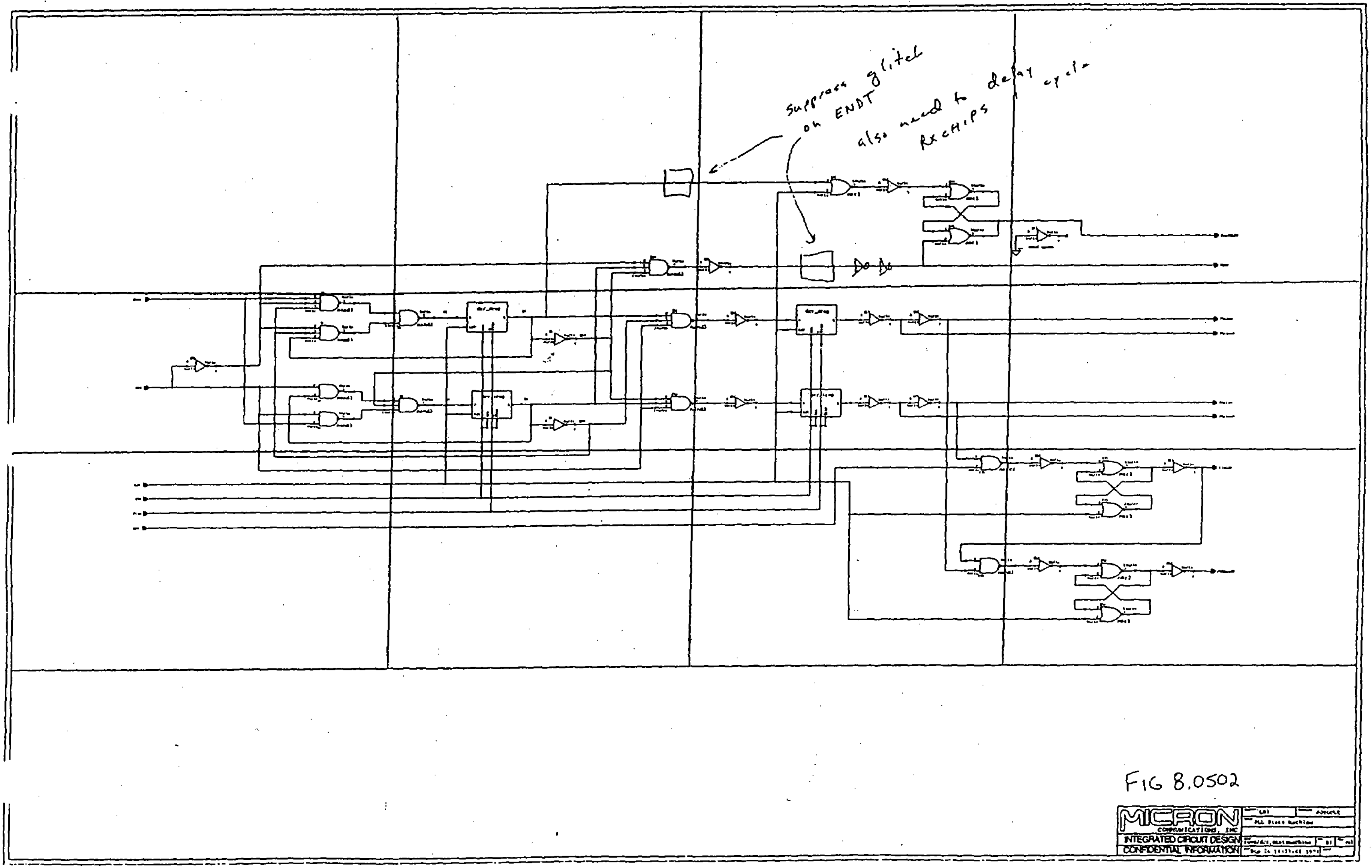
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Counter Bit	
NAME: l03reva/dcr_counterbit	REV: B1 SIZE: A
DATE: Sep 26 09:26:35 1994	SHEET:

FIG. 8.050102

8.0502AD	8.0502BD	8.0502CD
8.0502AC	8.0502BC	8.0502CC
8.0502AB	8.0502BB	8.0502CB
8.0502AA	8.0502BA	8.0502CA

Fig 8.0502



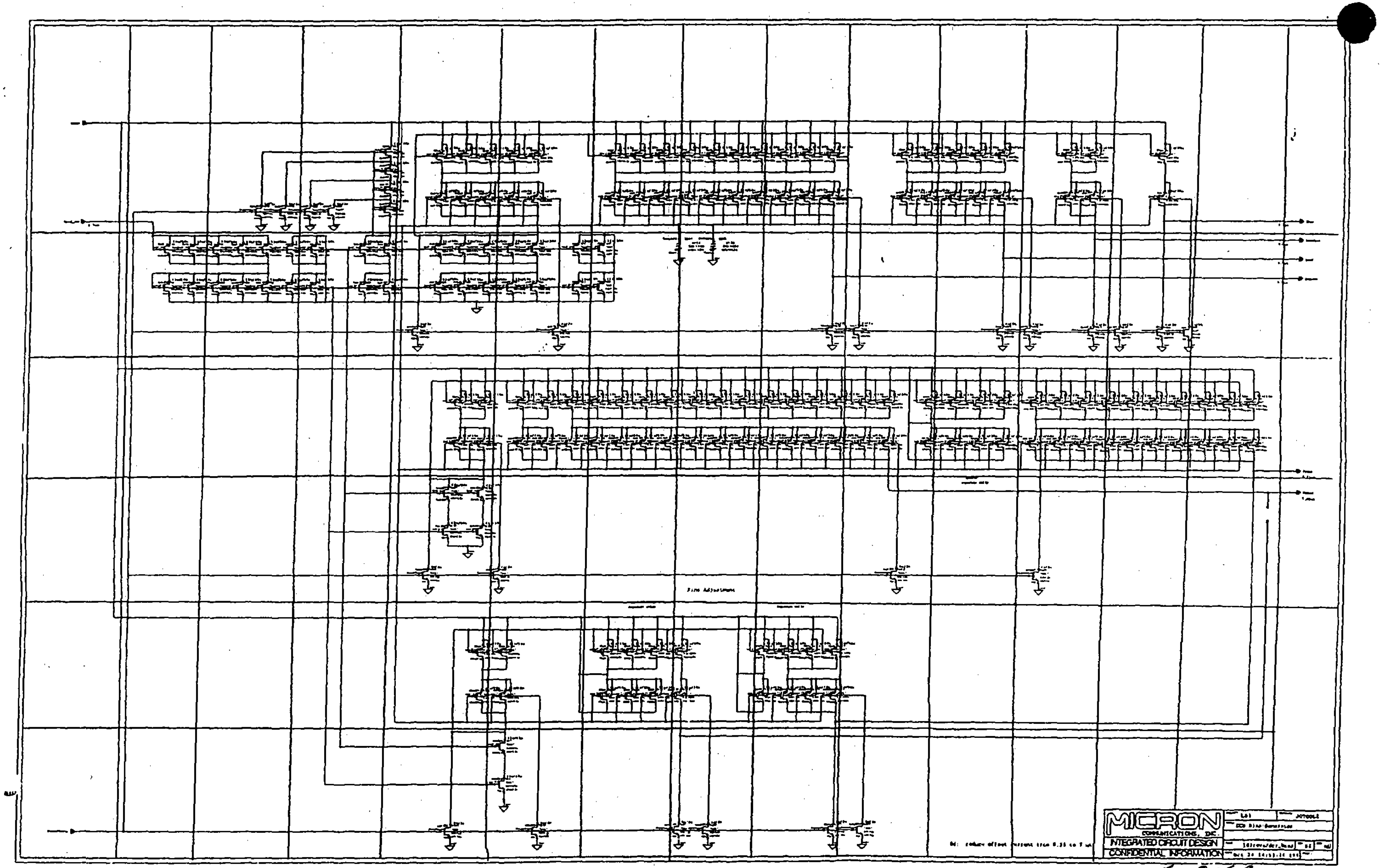
Suppress glitch on ENDT

also need to delay RxCHIPS 1 cycle

FIG 8.0502

8.0503AA	8.0503AB	8.0503AC	8.0503AD	8.0503AE	8.0503AF	8.0503AG	8.0503AH	8.0503AI	8.0503AJ	8.0503AK	8.0503AL	8.0503AM	8.0503AN	8.0503AO
8.0503BA	8.0503BB	8.0503BC	8.0503BD	8.0503BE	8.0503BF	8.0503BG	8.0503BH	8.0503BI	8.0503BJ	8.0503BK	8.0503BL	8.0503BM	8.0503BN	8.0503BO
8.0503CA	8.0503CB	8.0503CC	8.0503CD	8.0503CE	8.0503CF	8.0503CG	8.0503CH	8.0503CI	8.0503CJ	8.0503CK	8.0503CL	8.0503CM	8.0503CN	8.0503CO
8.0503DA	8.0503DB	8.0503DC	8.0503DD	8.0503DE	8.0503DF	8.0503DG	8.0503DH	8.0503DI	8.0503DJ	8.0503DK	8.0503DL	8.0503DM	8.0503DN	8.0503DO
8.0503EA	8.0503EB	8.0503EC	8.0503ED	8.0503EE	8.0503EF	8.0503EG	8.0503EH	8.0503EI	8.0503EJ	8.0503EK	8.0503EL	8.0503EM	8.0503EN	
8.0503FA	8.0503FB	8.0503FC	8.0503FD	8.0503FE	8.0503FF	8.0503FG	8.0503FH	8.0503FI	8.0503FJ	8.0503FK	8.0503FL	8.0503FM	8.0503FN	

Fig 8.0503


MICRON
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INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
Fine Adjustment

FIG. 8.0503

8.0504AA	8.0504AB	8.0504AC	8.0504AD	
8.0504BA	8.0504BB	8.0504BC	8.0504BD	
8.0506CA	8.0504CB	8.0504CC	8.0504CD	8.0504CE
8.0504DA	8.0504DB	8.0504DC	8.0504DD	8.0504DE
8.0504EA	8.0504EB	8.0504EC	8.0504ED	8.0504EE

Fig 8.0504

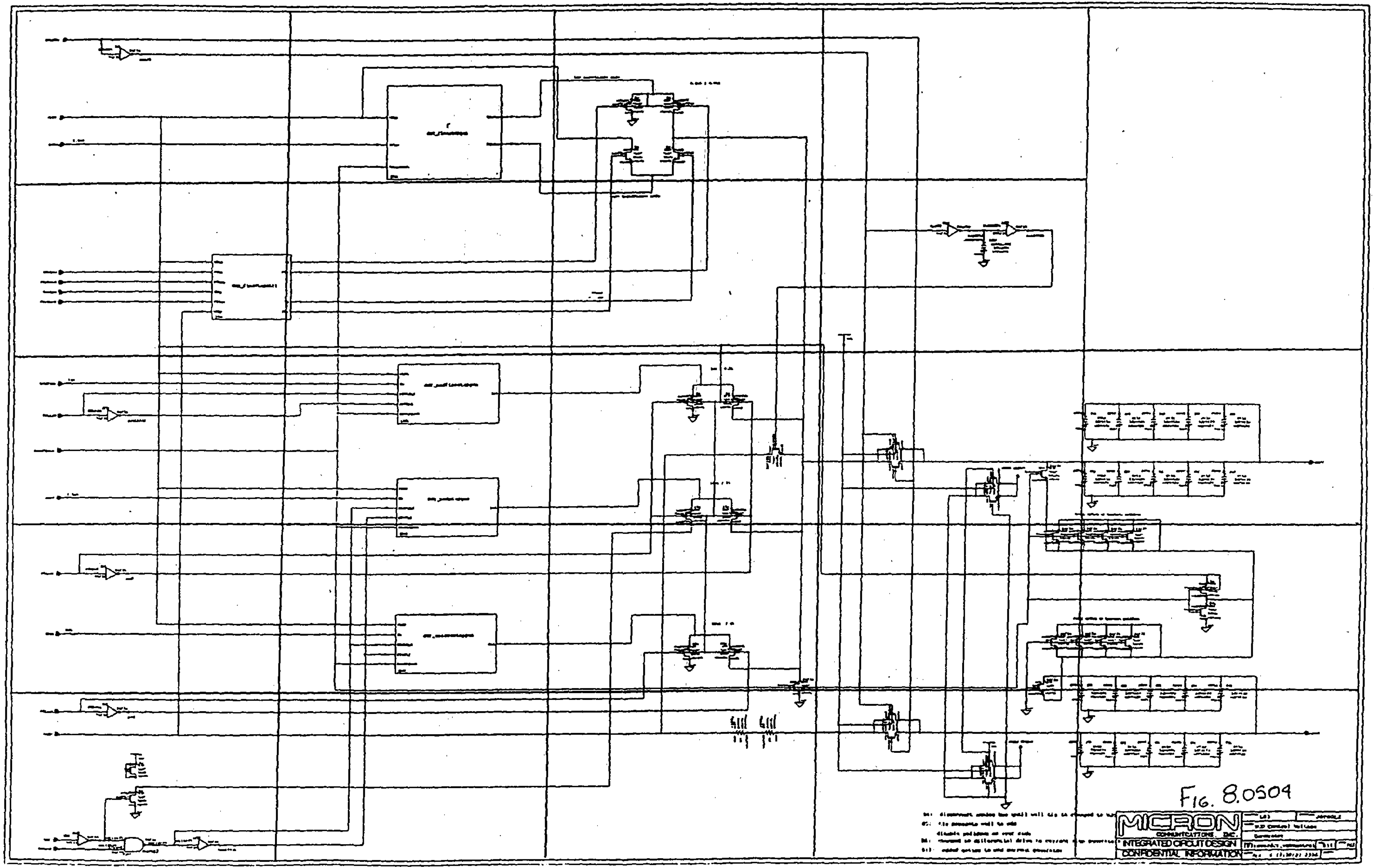
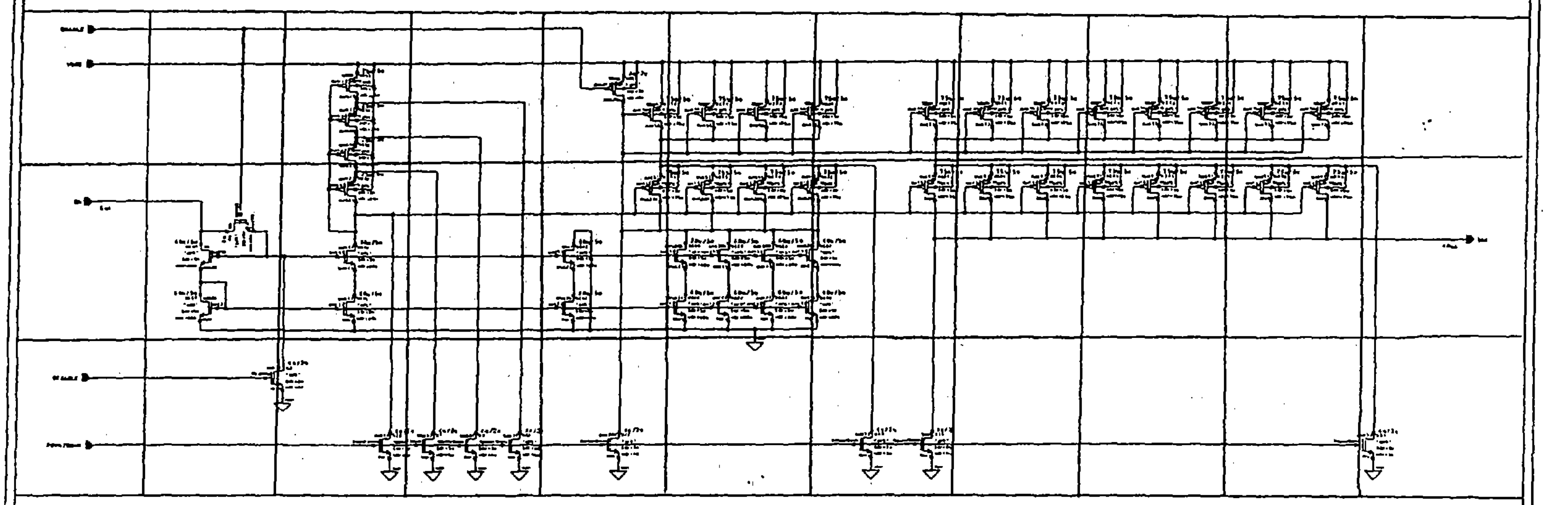
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

FIG. 8.0504

8.050401AA	8.050401AB	8.050401AC	8.050401AD	8.050401AE	8.050401AF	8.050401AG	8.050401AH	8.050401AI	8.050401AJ	
8.050401BA	8.050401BB	8.050401BC	8.050401BD	8.050401BE	8.050401BF	8.050401BG	8.050401BH	8.050401BI	8.050401BJ	8.050401BK
8.050401CA	8.050401CB	8.050401CC	8.050401CD	8.050401CE	8.050401CF	8.050401CG	8.050401CH	8.050401CI	8.050401CJ	8.050401CK

Fig 8.050401



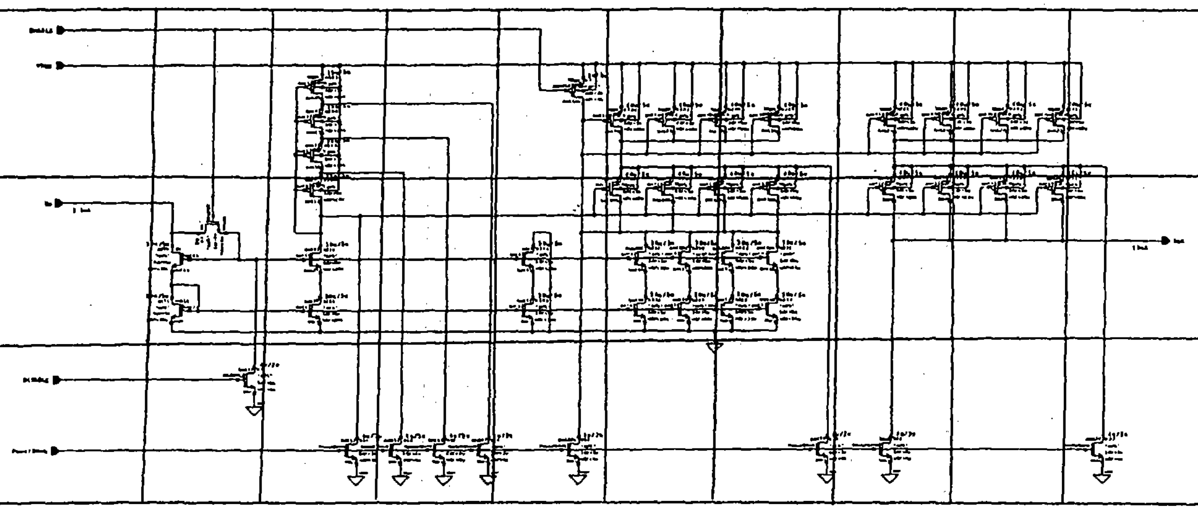
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

LO3	JOTOOLE
Coarse Step Generator	
[illegible]	
[illegible]/dcr_coarsestepgen	01
Sep 26 09:29:43 199[illegible]	

FIG 8.050401

8.050402AA	8.050402AB	8.050402AC	8.050402AD	8.050402AE	8.050402AF	8.050402AG	8.050402AH	8.050402AI	8.050402AJ
8.050402BA	8.050402BB	8.050402BC	8.050402BD	8.050402BE	8.050402BF	8.050402BG	8.050402BH	8.050402BI	8.050402BJ
8.050402CA	8.050402CB	8.050402CC	8.050402CD	8.050402CE	8.05040CF	8.050402CG	8.050402CH	8.050402CI	8.050402CJ

Fig 8.050402



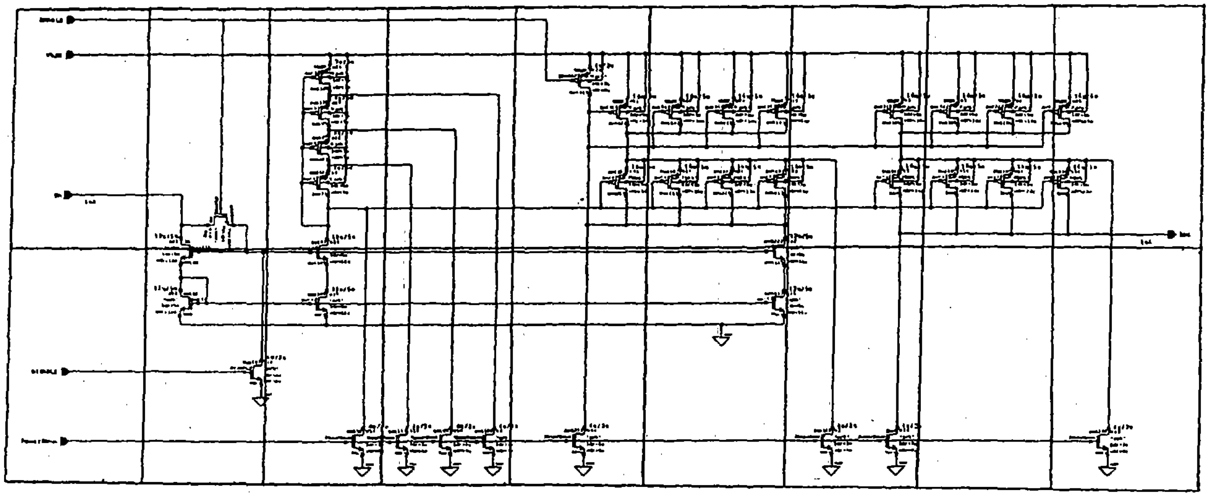
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03	JOTOOLE
Medium Step Generator	
2k	
/tava/dcr_medstepgen	B1 | n1
Sep 26 09:30:35 199	

FIG. 8.050402

8.050403AA	8.050403AB	8.050403AC	8.050403AD	8.050403AE	8.050403AF	8.050403AG	8.050403AH	8.050403AI
8.050403BA	8.050403BB	8.050403BC	8.050403BD	8.050403BE	8.050403BF	8.050403BG	8.050403BH	8.050403BI

Fig 8.050403



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN,
CONFIDENTIAL INFORMATION

L03
JOTOOLE
Medium Fine Step Generator
0.2µ
w2/dcr_medfinestepgen
01
n1
Sep 26 09:31:18 1996

Fig. 8.050403

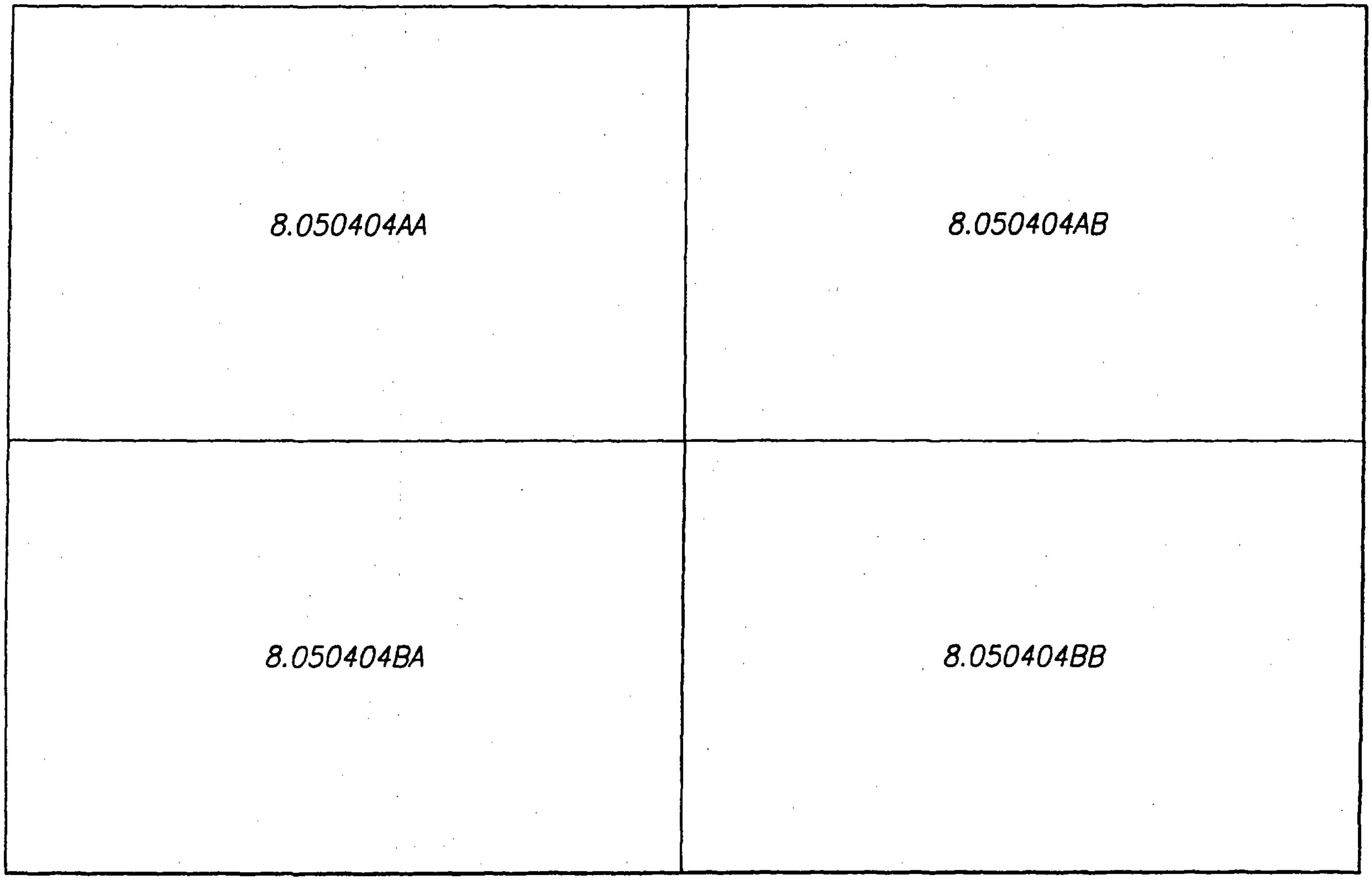
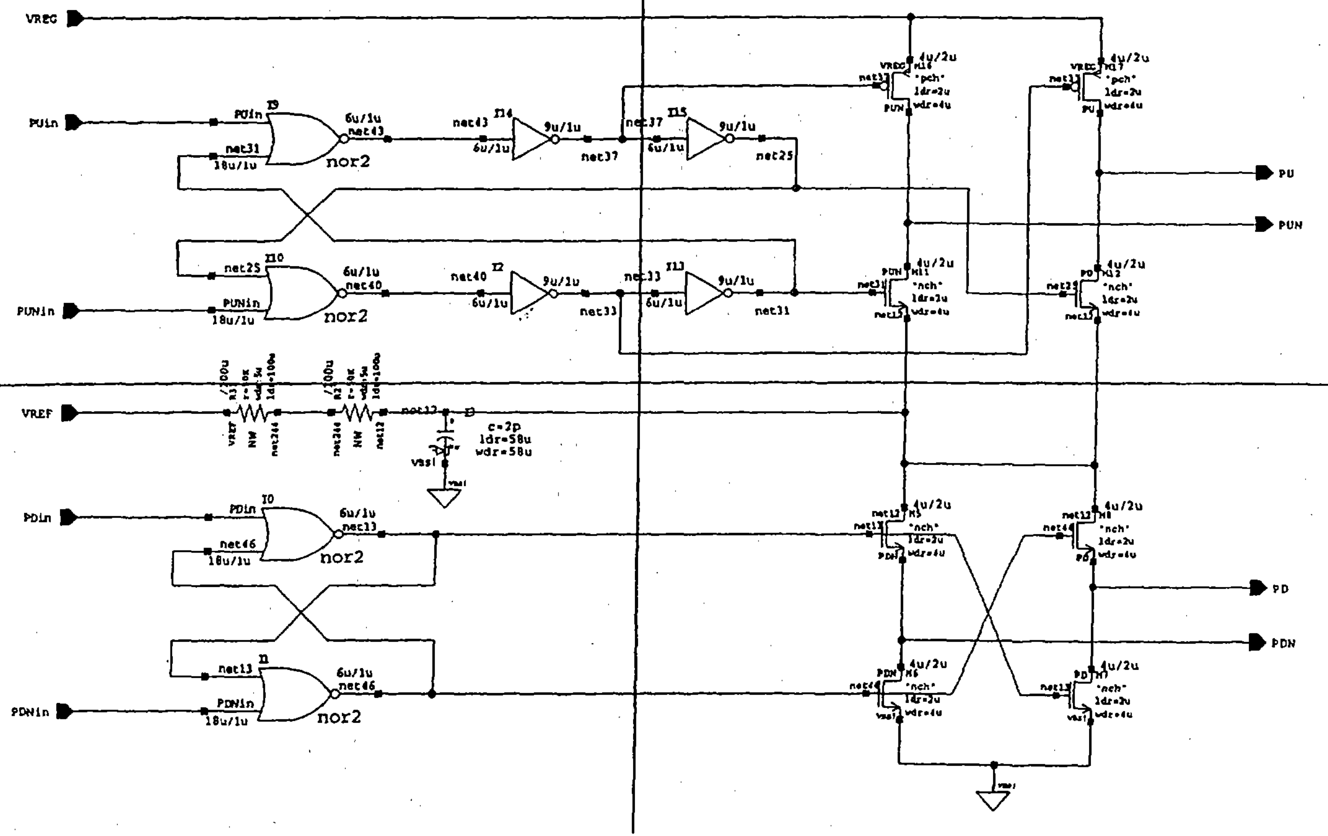


FIG 8.050404



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: DCR Fine Step Controller			
NAME: l03reva/dcr_finestepctrl	REV: B1	SIZE: A	
DATE: Sep 26 09:32:11 1994	SHEET:		

FIG. 8.050909

8.050405AA	8.050405AB	8.050405AC	8.050405AD	8.050405AE	8.050405AF	8.050405AG	8.050405AH	8.050405AI	8.050405AJ	8.050405AK	8.050405AL	8.050405AM
8.050405BA	8.050405BB	8.050405BC	8.050405BD	8.050405BE	8.050405BF	8.050405BG	8.050405BH	8.050405BI	8.050405BJ	8.050405BK	8.050405BL	8.050405BM
8.050405CA	8.050405CB	8.050405CC	8.050405CD	8.050405CE	8.050405CF	8.050405CG	8.050405CH	8.050405CI	8.050405CJ	8.050405CK	8.050405CL	8.050405CM
8.050405DA	8.050405DB	8.050405DC	8.050405DD	8.050405DE	8.050405DF	8.050405DG	8.050405DH	8.050405DI	8.050405DJ			
8.050405EA	8.050405EB	8.050405EC	8.050405ED	8.050405EE	8.050405EF	8.050405EG	8.050405EH	8.050405EI	8.050405EJ			

Fig 8.050405

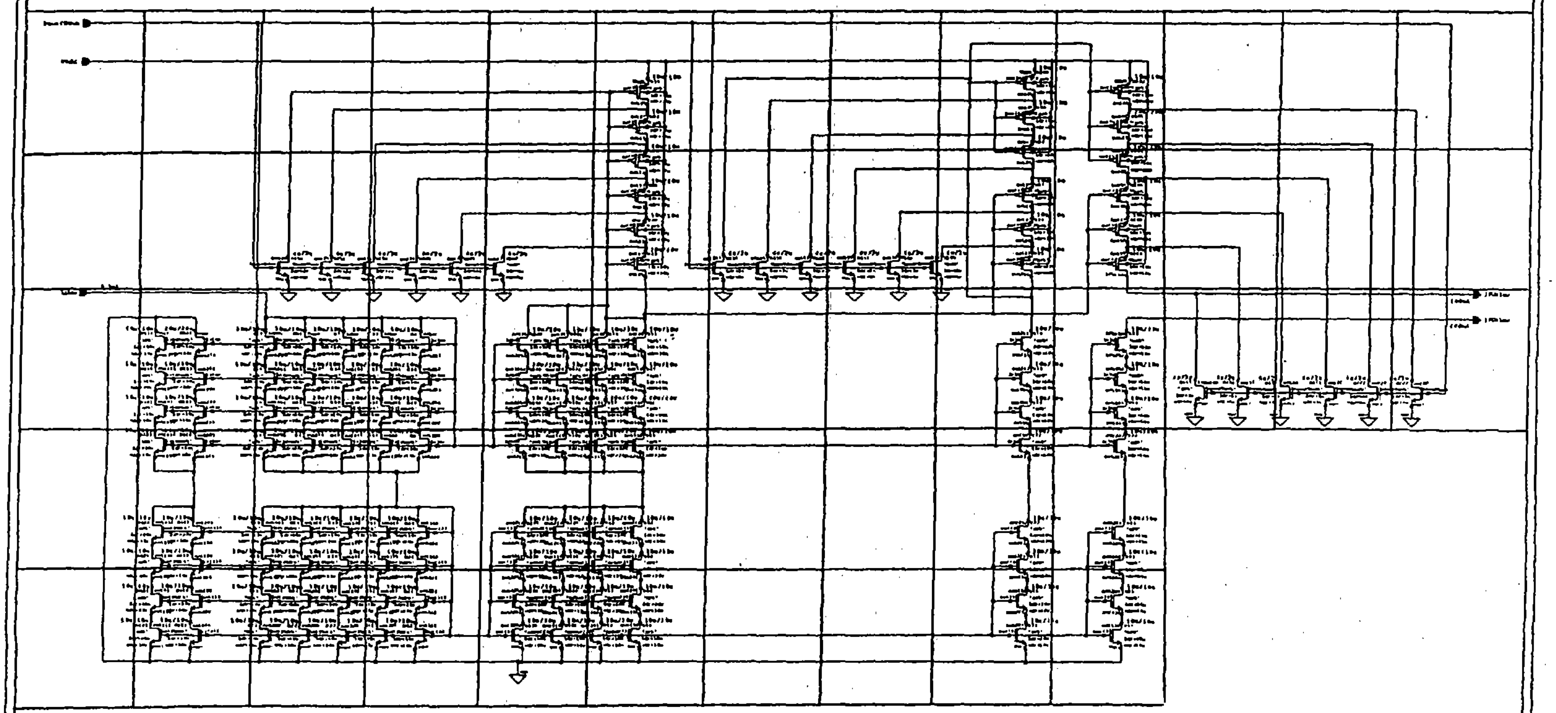


FIG 8.050405

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L01
JOTOOLE
Fine Step Generator
0.03%
@Treva/dcr_finestepgen
B1
r1
Sep 26 09:33:00 1996

8.0505AA	8.0505AB	8.0505AC	8.0505AD	8.0505AE	8.0505AF	8.0505AG	8.0505AH	8.0505AI	8.0505AJ	8.0505AK	8.0505AL	8.0505AM	8.0505AN
8.0505BA	8.0505BB	8.0505BC	8.0505BD	8.0505BE	8.0505BF	8.0505BG	8.0505BH	8.0505BI	8.0505BJ	8.0505BK	8.0505BL	8.0505BM	8.0505BN
8.0505CA	8.0505CB	8.0505CC	8.0505CD	8.0505CE	8.0505CF	8.0505CG	8.0505CH	8.0505CI	8.0505CJ	8.0505CK	8.0505CL	8.0505CM	8.0505CN
8.0505DA	8.0505DB	8.0505DC	8.0505DD	8.0505DE	8.0505DF	8.0505DG	8.0505DH	8.0505DI	8.0505DJ	8.0505DK	8.0505DL	8.0505DM	8.0505DN
8.0505EA	8.0505EB	8.0505EC	8.0505ED	8.0505EE	8.0505EF								

Fig 8.0505

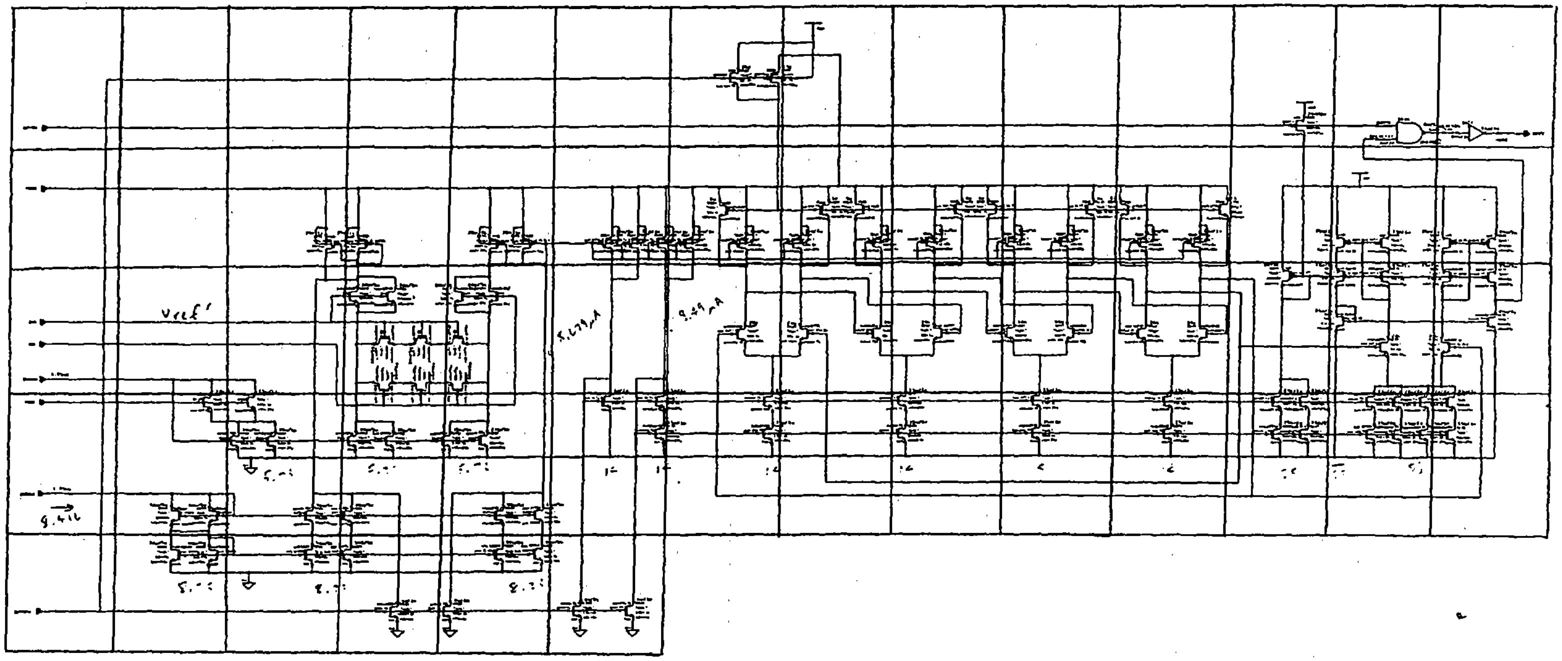


FIG. 8.0505

238μA

MICRON
COMMUNICATIONS, INC
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

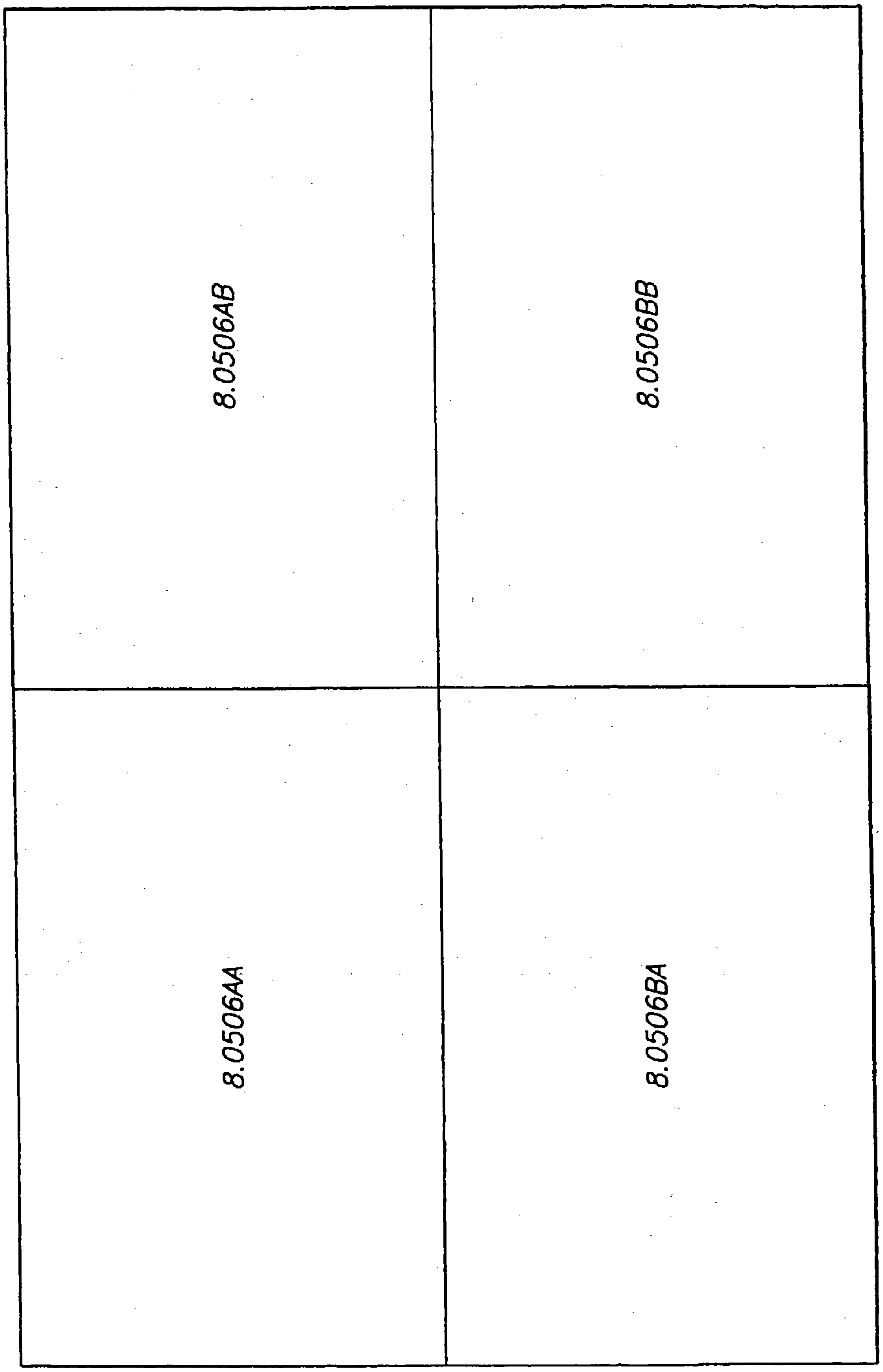
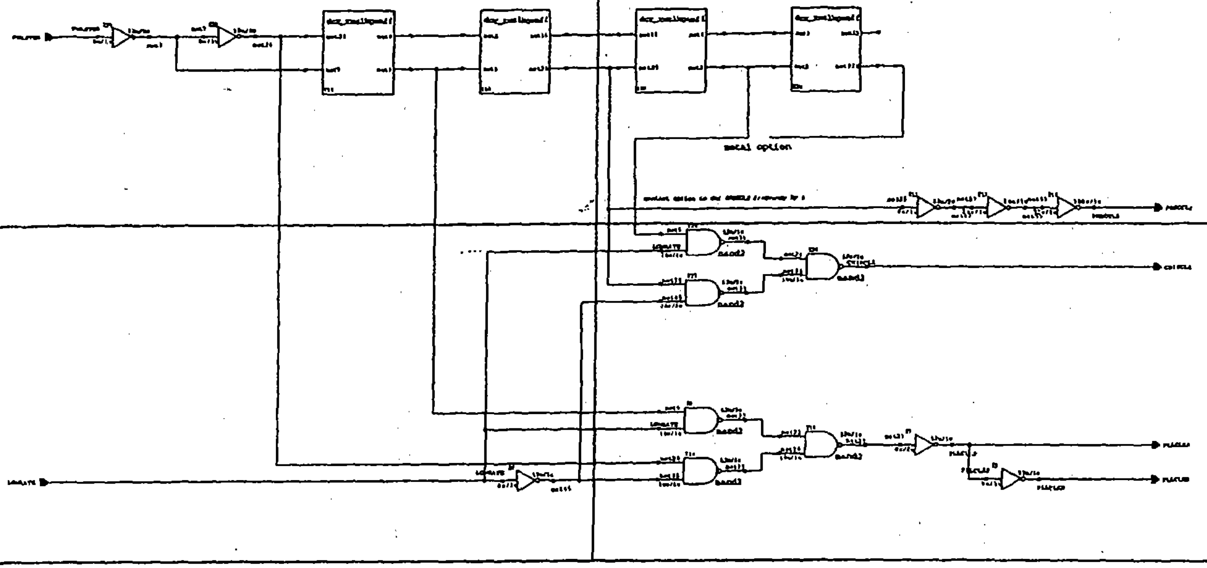


Fig 8.0506



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
JOTOOLE
RX Clock Generator
f=9.538/4.769MHz
l03revs/dcr_rxclkgen
81
Jan 2 14:36:58 1995

FIG. 8.0506

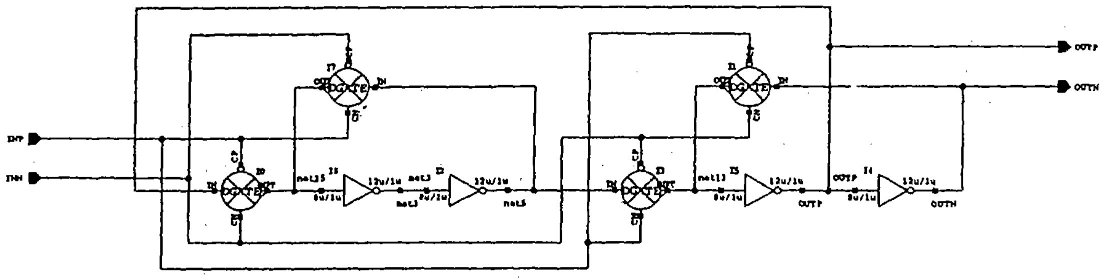


Fig. 8.050601

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
JOTOOLE
Rx Clock Generator
Flip-Flop
l03reva/dcr_rxclkgenff
B1
nil
Sep 26 09:36:05 1994

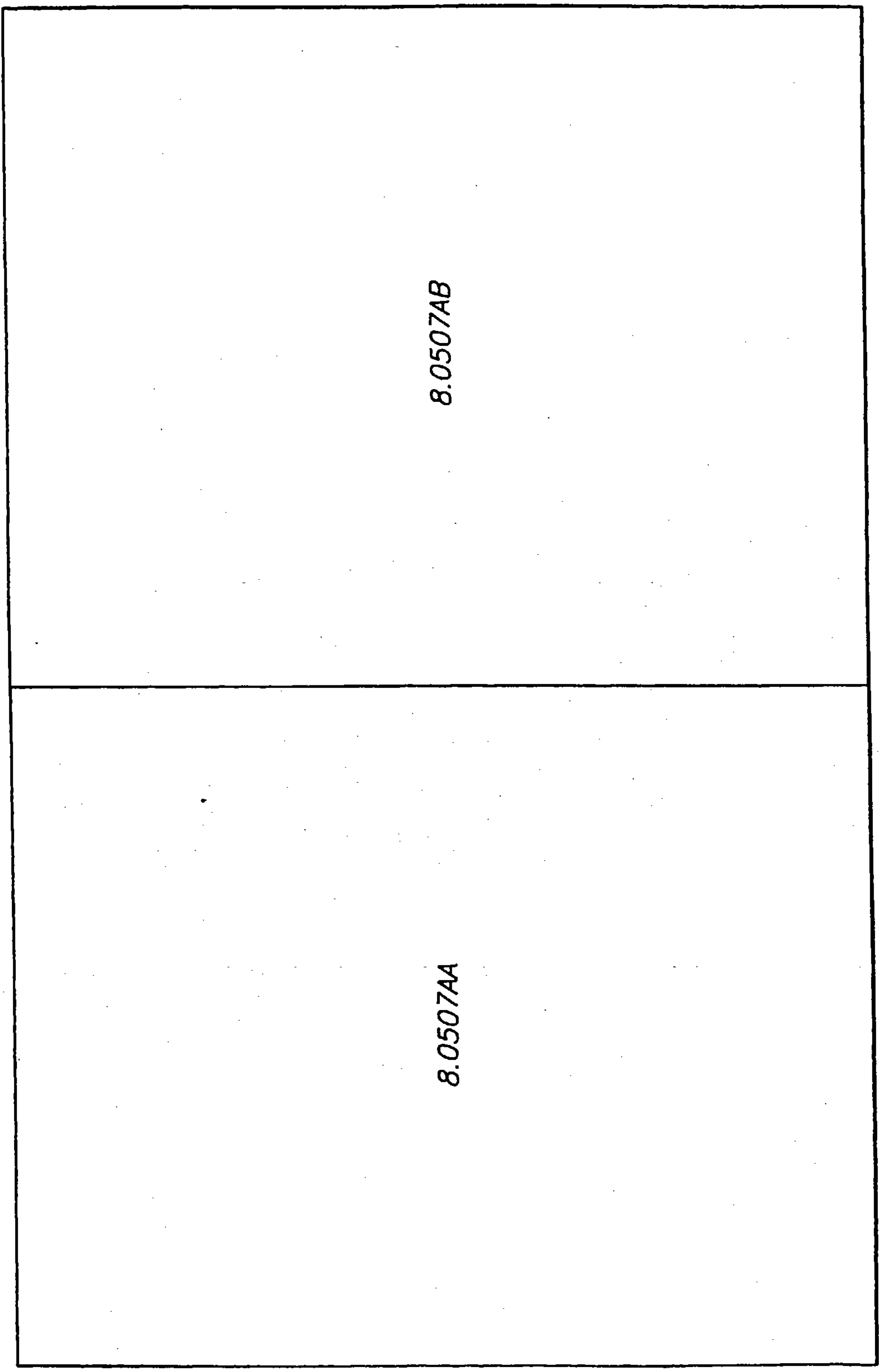
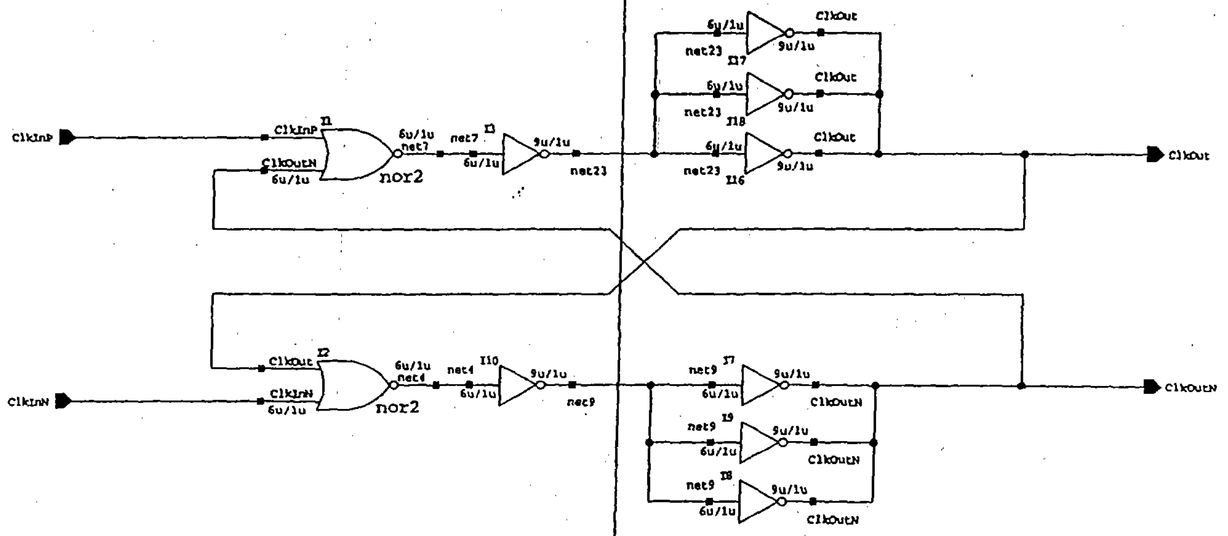


FIG. 8.0507



B8: increased drive at expense of non-overlap time

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: PLL Non-overlapping Clock Generator
NAME: 103reva/dcr_clkgen
REV: B8
SIZE: A
DATE: Jan 3 14:04:11 1996
SHEET:

FIG. 8.0507

8.06AA	8.06AB	8.06AC	8.06AD
8.06BA	8.06BB	8.06BC	8.06BD
8.06CA	8.06CB	8.06CC	8.06CD
8.06DA	8.06DB	8.06DC	8.06DD
8.06EA	8.06EB	8.06EC	8.06ED

FIG 8.06

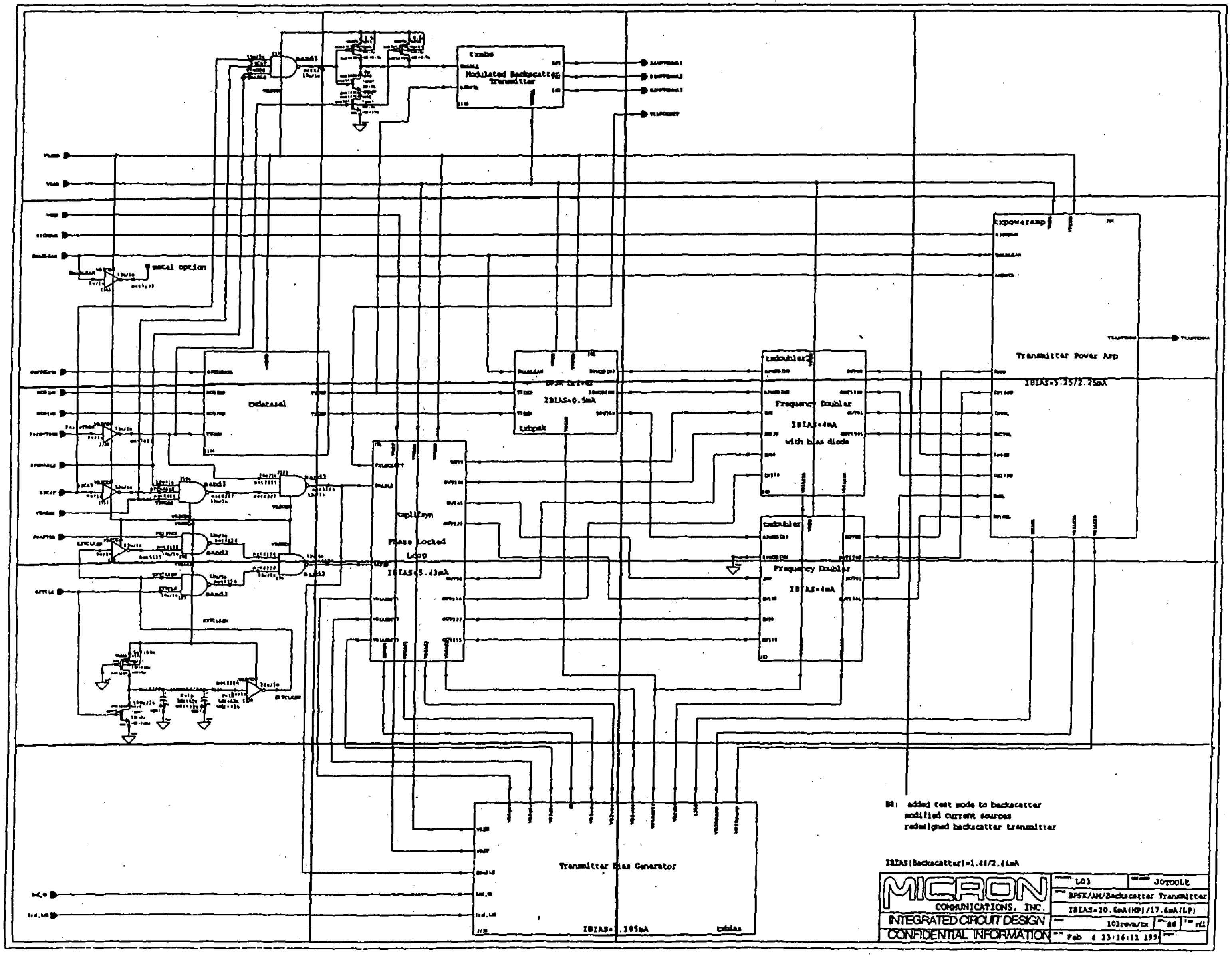

txmbs
Modulated Backscatter Transmitter
metal option
txdatasel
txbpsk
BPSK Driver
IBIAS=0.5mA
txpllsyn
Phase Locked Loop
IBIAS=5.43mA
txdoubler2
Frequency Doubler
IBIAS=4mA
with bias diode
txdoubler
Frequency Doubler
IBIAS=4mA
txpoweramp
Transmitter Power Amp
IBIAS=5.35/2.25mA
Transmitter Bias Generator
IBIAS=1.385mA
txbias
B8: added test mode to backscatter
modified current sources
redesigned backscatter transmitter
IBIAS(Backscatter)=1.44/2.44mA
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
JOTOOLE
BPSK/AM/Backscatter Transmitter
IBIAS=20.6mA(HP)/17.6mA(LP)
103revb/tx
B8
Feb 4 13:16:11 199

FIG. 8.06

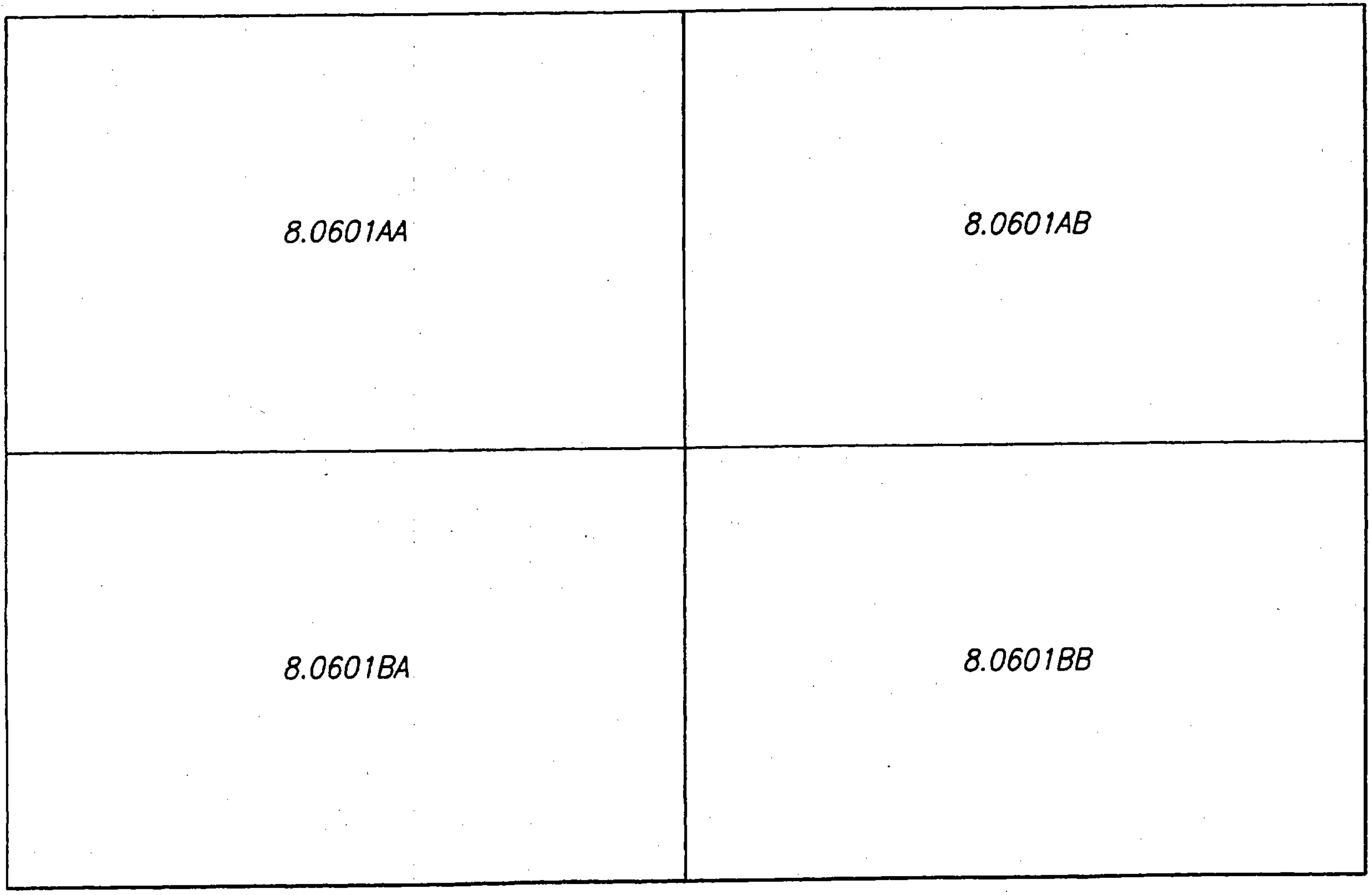
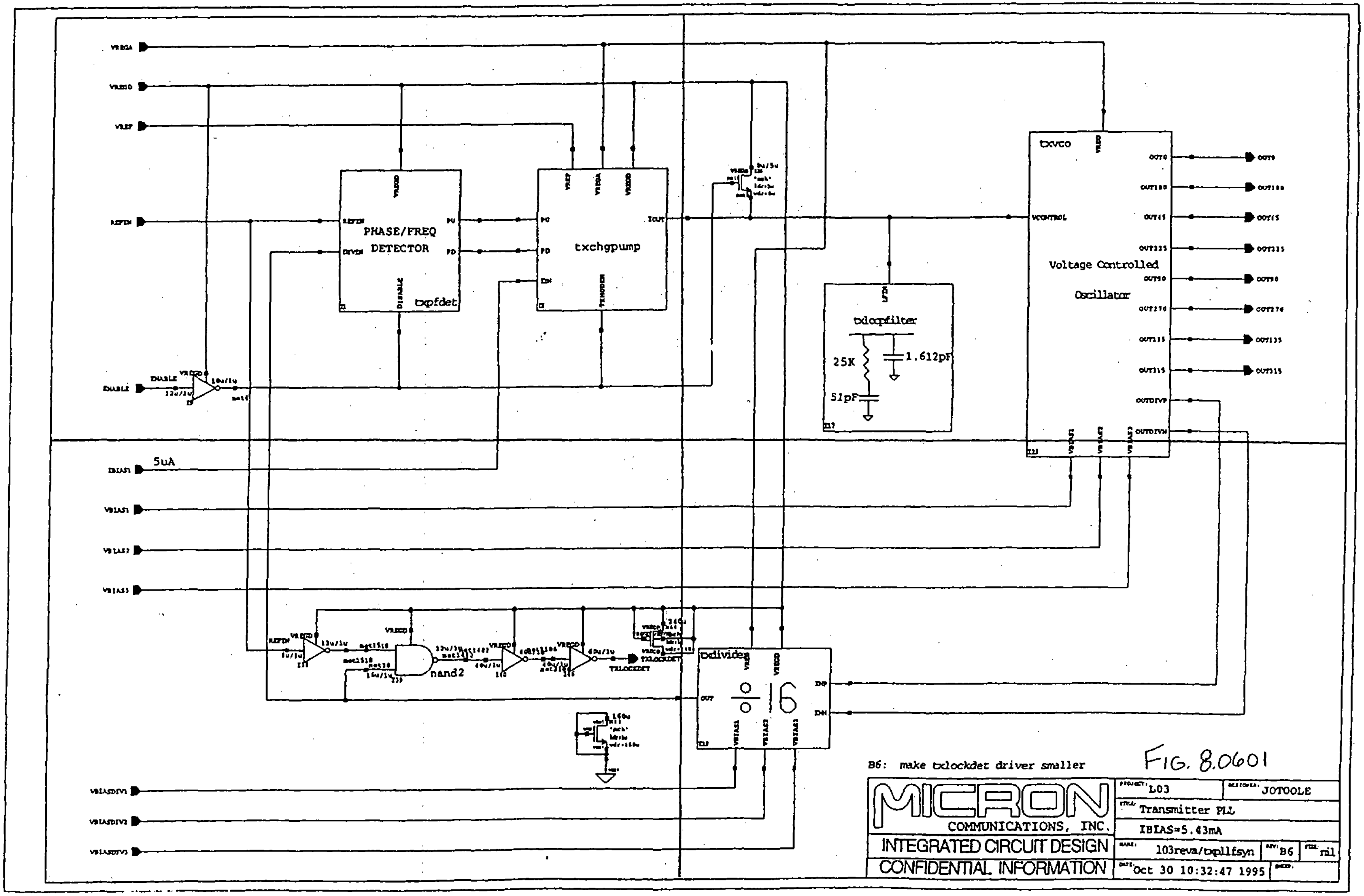


Fig 8.0601



B6: make txlockdet driver smaller

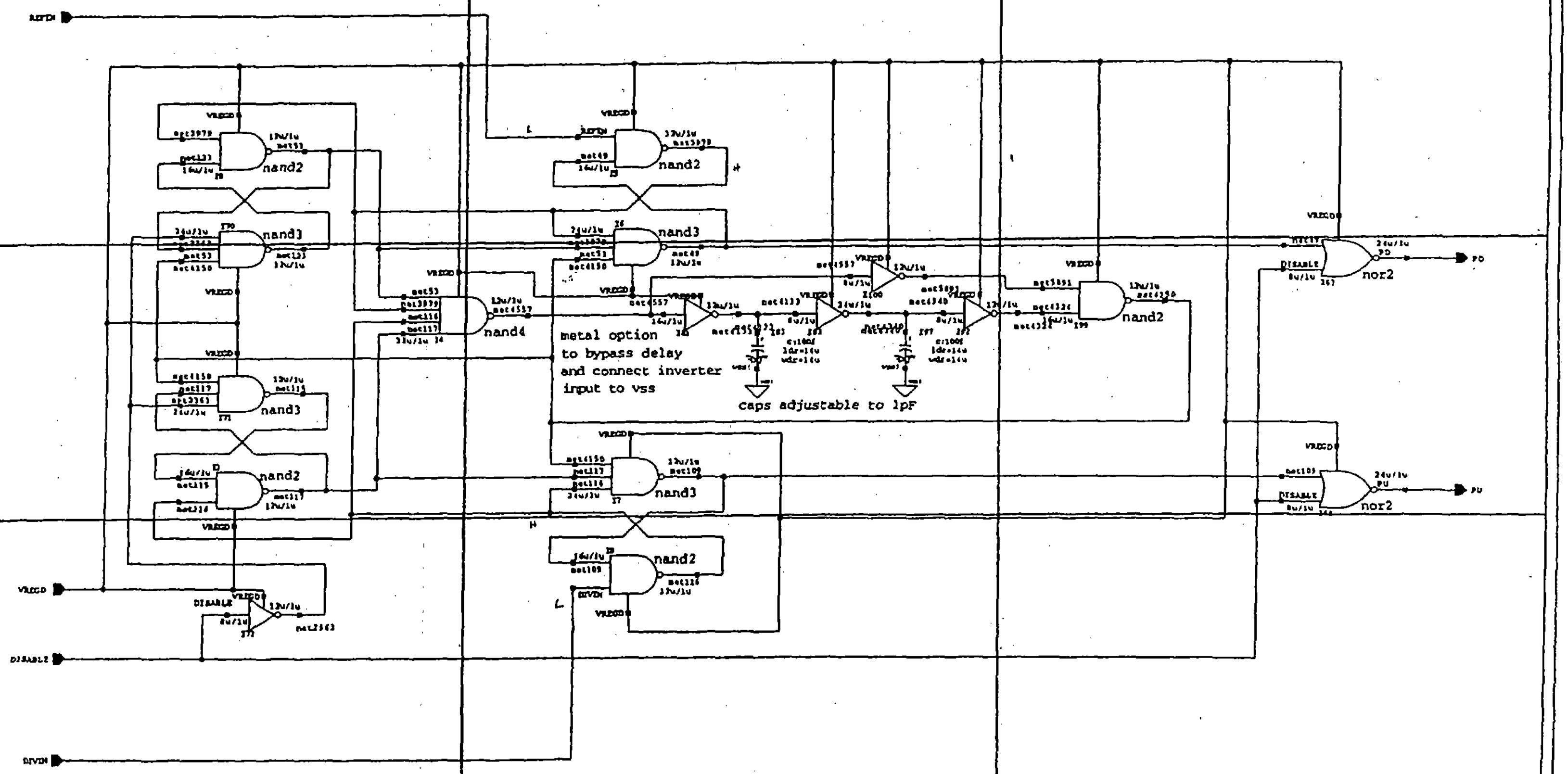
FIG. 8.0601

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Transmitter PLL	
IBIAS=5.43mA	
NAME: 103reva/txpllfsyn	REV: B6 · SIZE: nil
DATE: Oct 30 10:32:47 1995	SHEET:

8.060101AA	8.060101AB	8.060101AC
8.060101BA	8.060101BB	8.060101BC
8.060101CA	8.060101CB	8.060101CC

Fig 8.060101



metal option
to bypass delay
and connect inverter
input to vss

caps adjustable to 1pF

FIG. 8.060101

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
JOTOOLE
TX Phase/Frequency Detector
103reva/txpfdet
B1
nil
Mar 29 16:00:53 1995

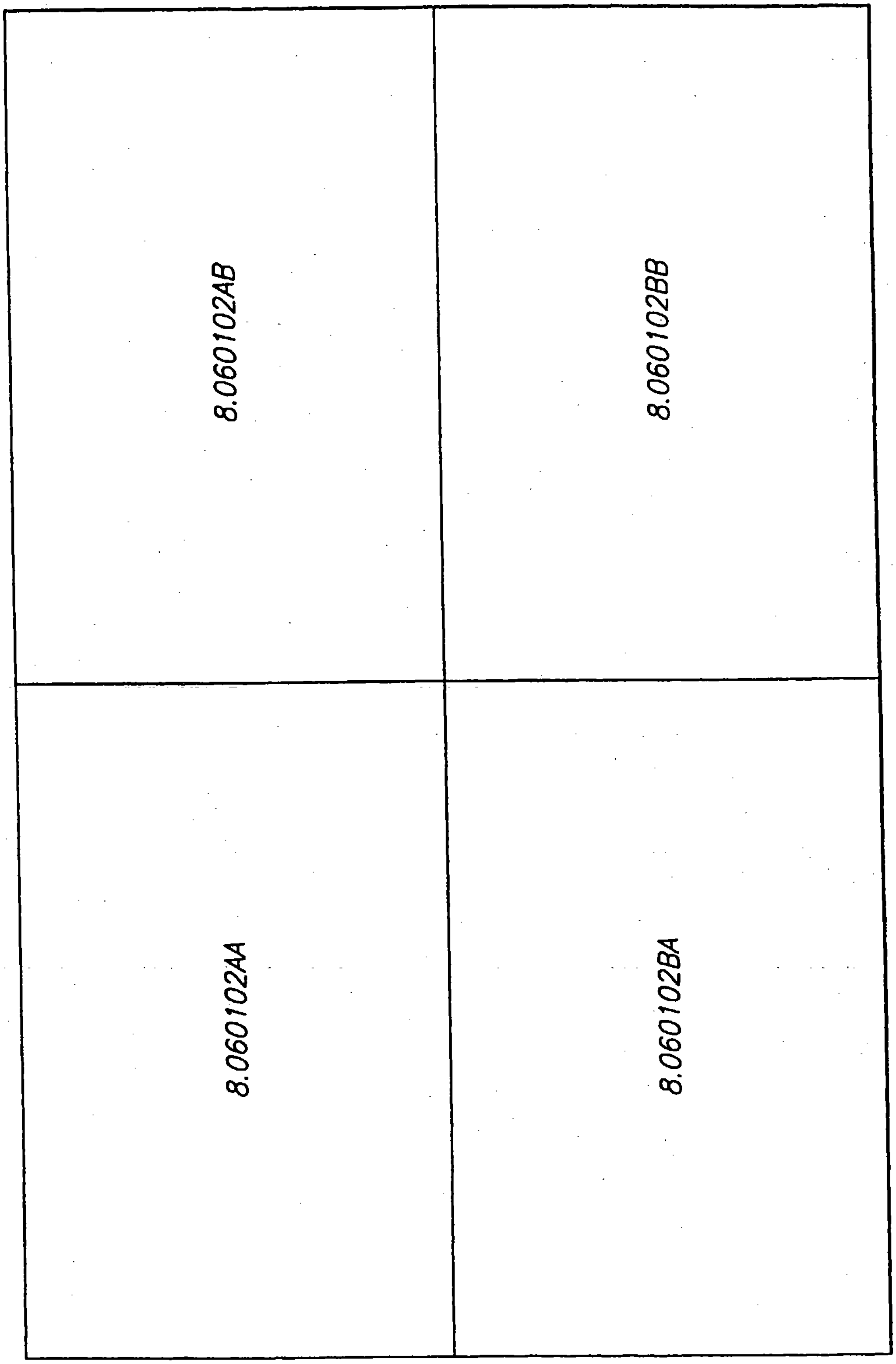
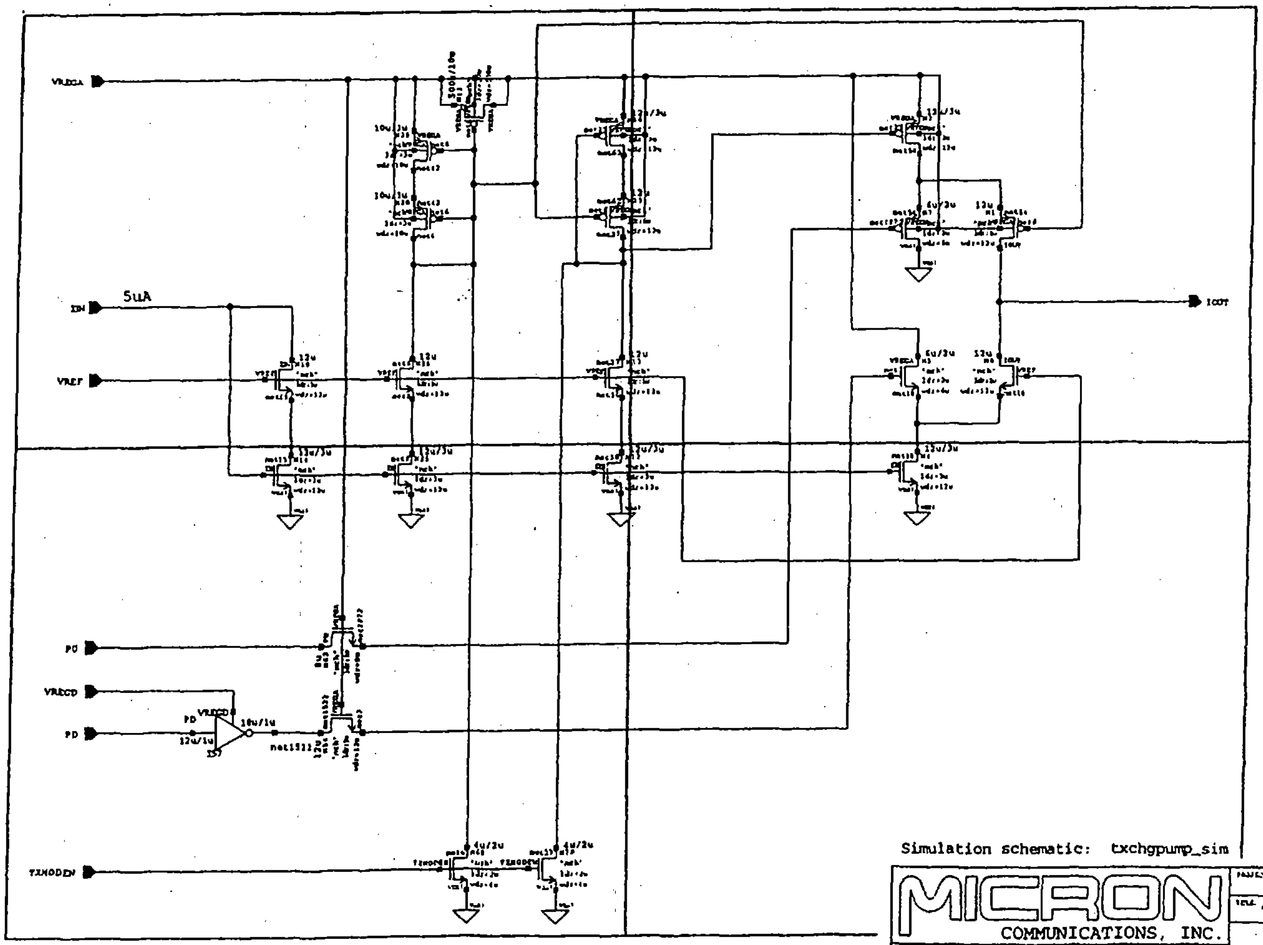


Fig 8.060102



Simulation schematic: txchgpump_sim

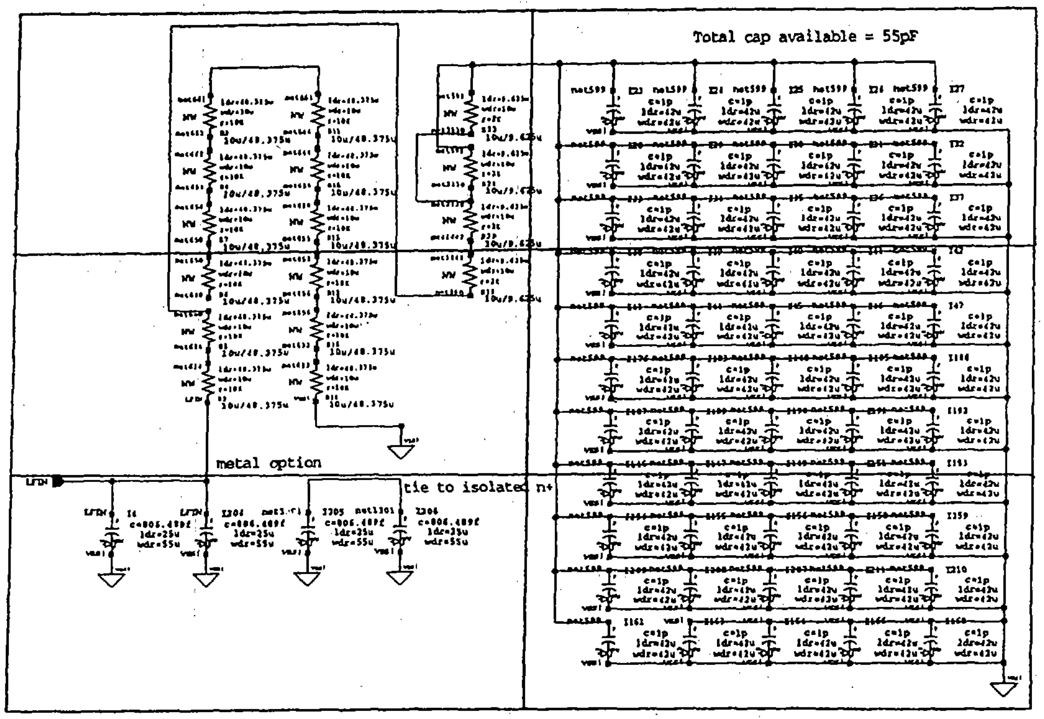
FIG. 8.060102

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: TX PLL Charge Pump	
NAME: 103reva/txchgpump	REV: B1
DATE: Feb 28 09:55:50 1995	

8.060103AA	8.060103AB
8.060103BA	8.060103BB
8.060103CA	8.060103CB

Fig 8.060103



B2: moved extra caps to biasok

B8: moved 2 2K resistors to txmbs

FIG. 8.060103

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03	JOTOOLE
TX PLL Loop Filter	
BW=700KHz PM=60deg	
103reva/txloopfilter	B8 nil
Feb 5 14:40:11 1996	

8.060104AA	8.060104AB	8.060104AC
8.060104BA	8.060104BB	8.060104BC
8.060104CA	8.060104CB	8.060104CC
8.060104DA	8.060104DB	8.060104DC

Fig 8.060104

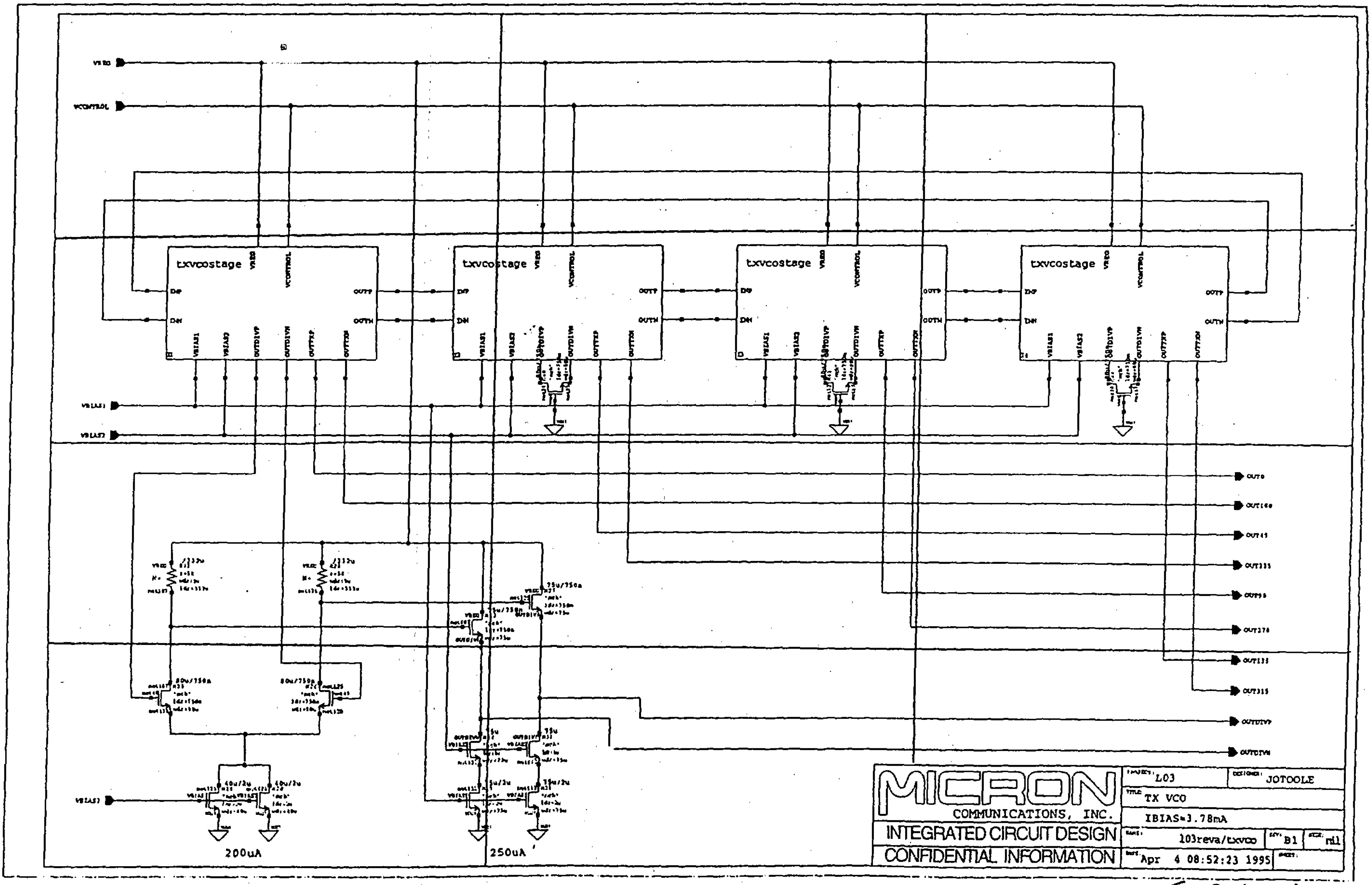
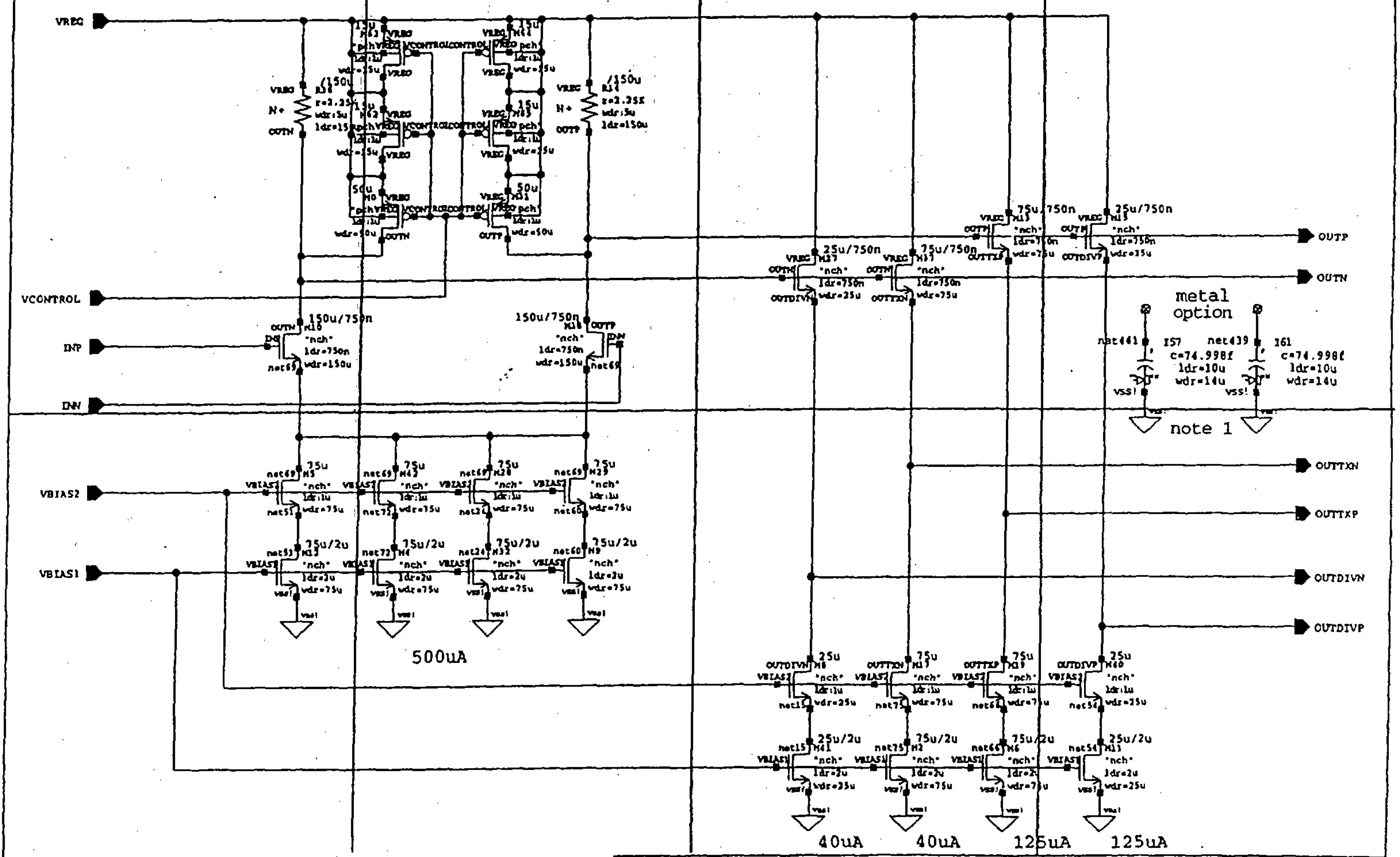

VREG
VCONTROL
VBIAS1
VBIAS2
txvcostage
INP
INN
OUTP
OUTN
VREG
VCONTROL
VBIAS1
VBIAS2
OUTDIVP
OUTDIVN
OUTTXP
OUTTXN
OUT0
OUT180
OUT45
OUT225
OUT90
OUT270
OUT135
OUT315
OUTDIVP
OUTDIVN
200uA
250uA
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
JOTOOLE
TX VCO
IBIAS=3.78mA
103reva/txvco
B1
nil
Apr 4 08:52:23 1995

FIG. 8.060104

8.06010401AA	8.06010401AB	8.06010401AC	8.06010401AD
8.06010401BA	8.06010401BB	8.06010401BC	8.06010401BD

Fig 8.06010401



Notes: 1. Caps are used for 915MHz metal option.
Allow L adjustment up to 24.75um.
(Poly option for 1.4GHz)
Tie each to an isolated n+ region.

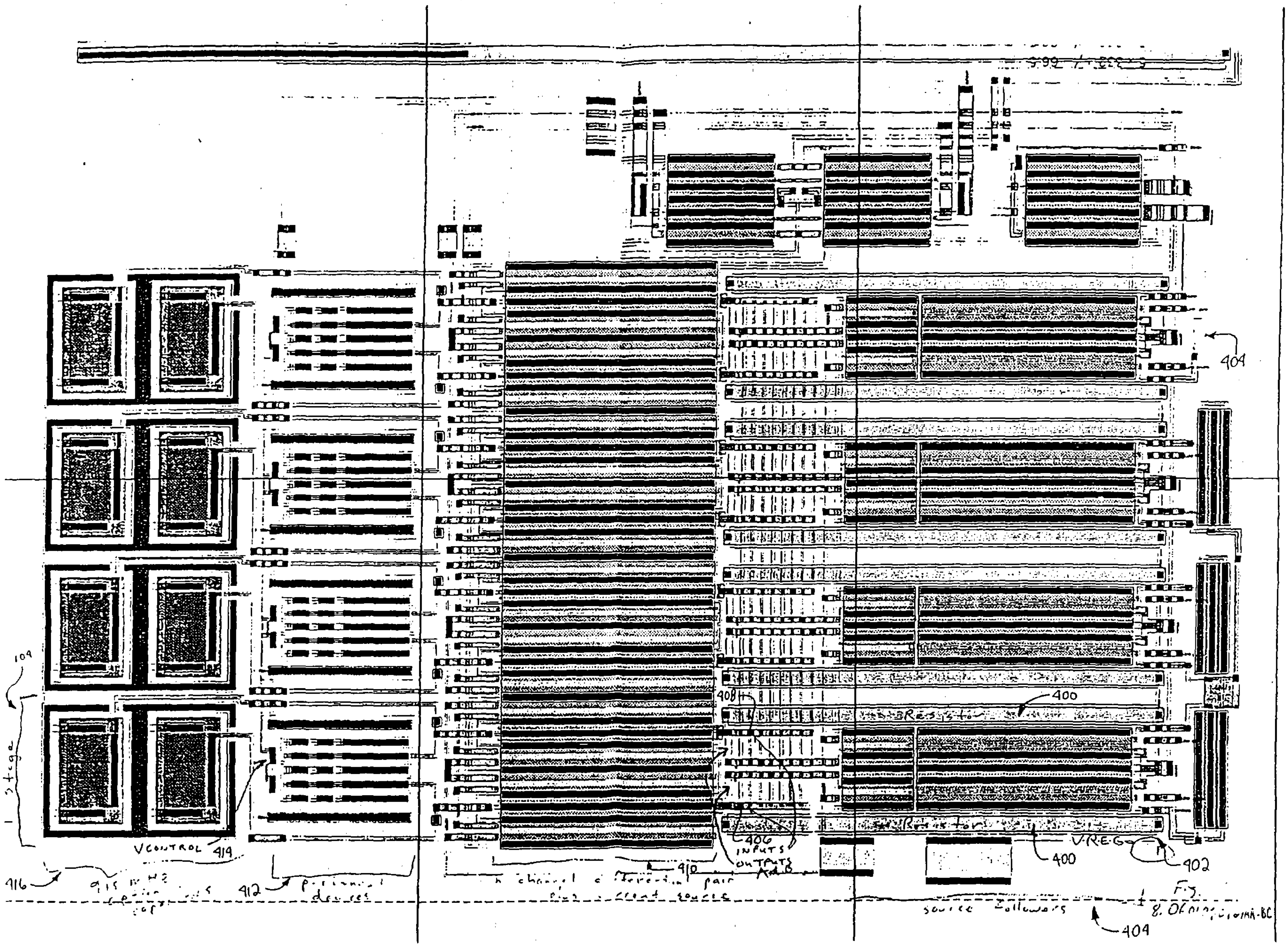
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: TX VCO Stage	
IBIAS=833uA	
NAME: 103reva/txvcostage	REV: B1 SIZE: A
DATE: Apr 26 17:02:22 1995	SHEET:

~~FIG.8.06010401~~
FIG.8.06010401

8.0601040101AA	8.0601040101AB	8.0601040101AC
8.0601040101BA	8.0601040101BB	8.0601040101BC

Fig 8.0601040101



404
400
Resistor
400
VREG
902
408
406
INPUTS
OUTPUTS A&B
410
n channel differential pair
plus current source
412
p-channel devices
VCONTROL
414
416
915 MHz
cap
104
stage
source followers
404

Fig. 8. Of [illegible]

8.060105AA	8.060105AB	8.060105AC	8.060105AD
8.060105BA	8.060105BB	8.060105BC	8.060105BD
8.060105CA	8.060105CB	8.060105CC	8.060105CD
8.060105DA	8.060105DB	8.060105DC	8.060105DD

Fig 8.060105

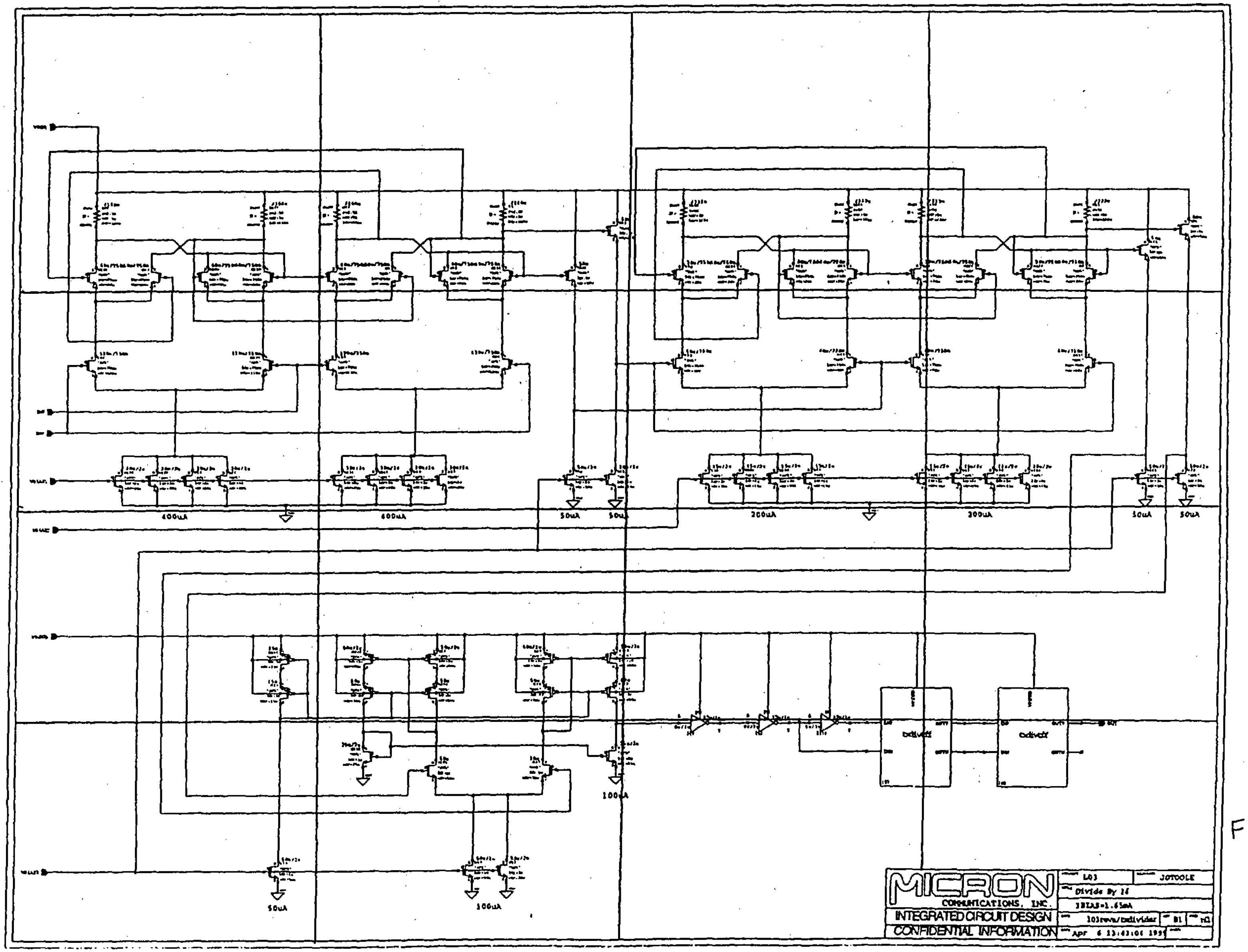

400uA
400uA
50uA
50uA
200uA
200uA
50uA
50uA
100uA
50uA
100uA
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
JOTOOLE
Divide By 16
IBIAS=1.65mA
103revs/txdivider
01
Apr 6 13:43:06 199

FIG. 8.060105

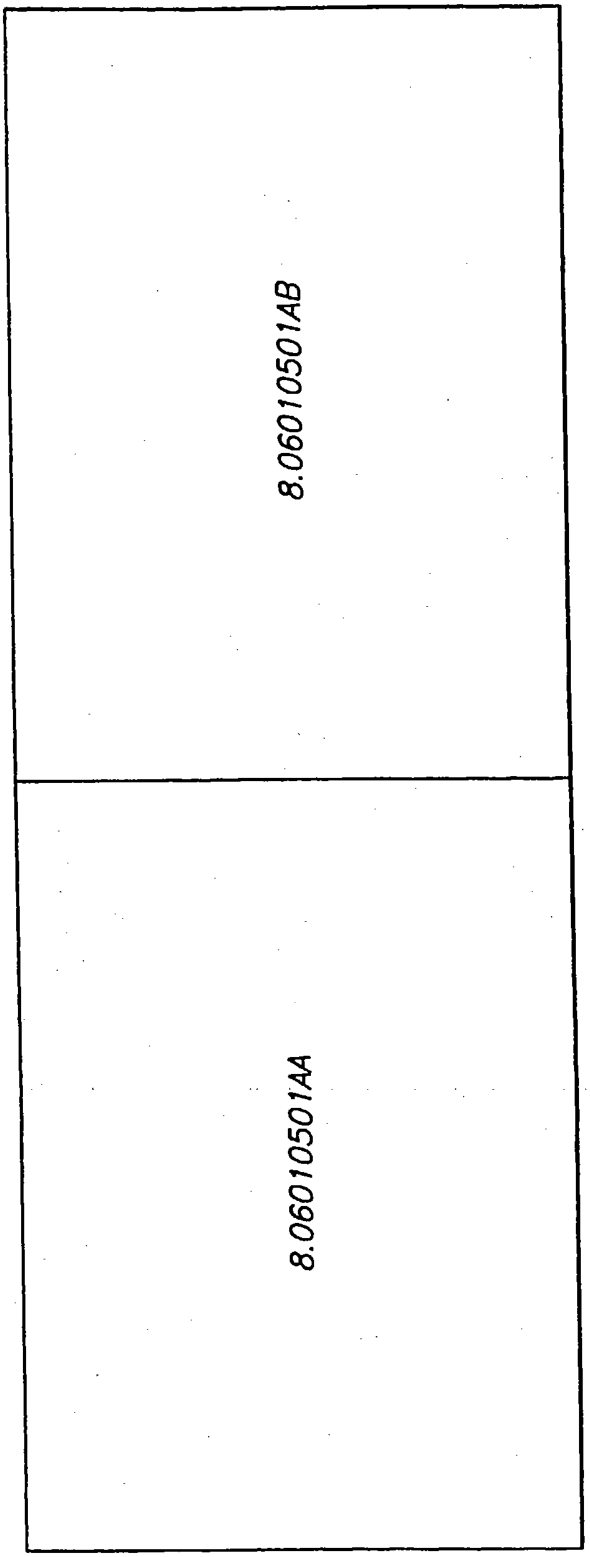
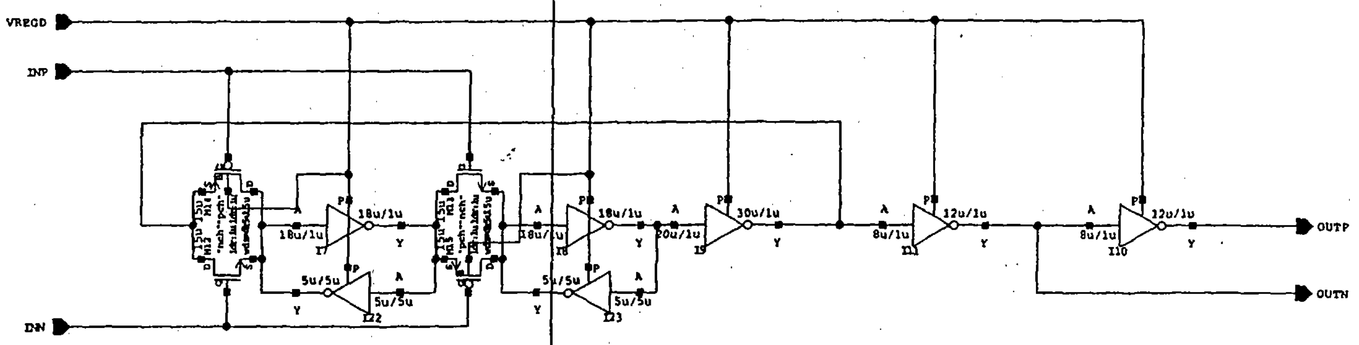


Fig 8.06010501



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: Divider Flip-flop			
NAME: 103reva/txdivtff	REV: B1	SIZE: A	
DATE: Mar 30 09:47:12 1995	SHEET:		

FIG. 8.06010501

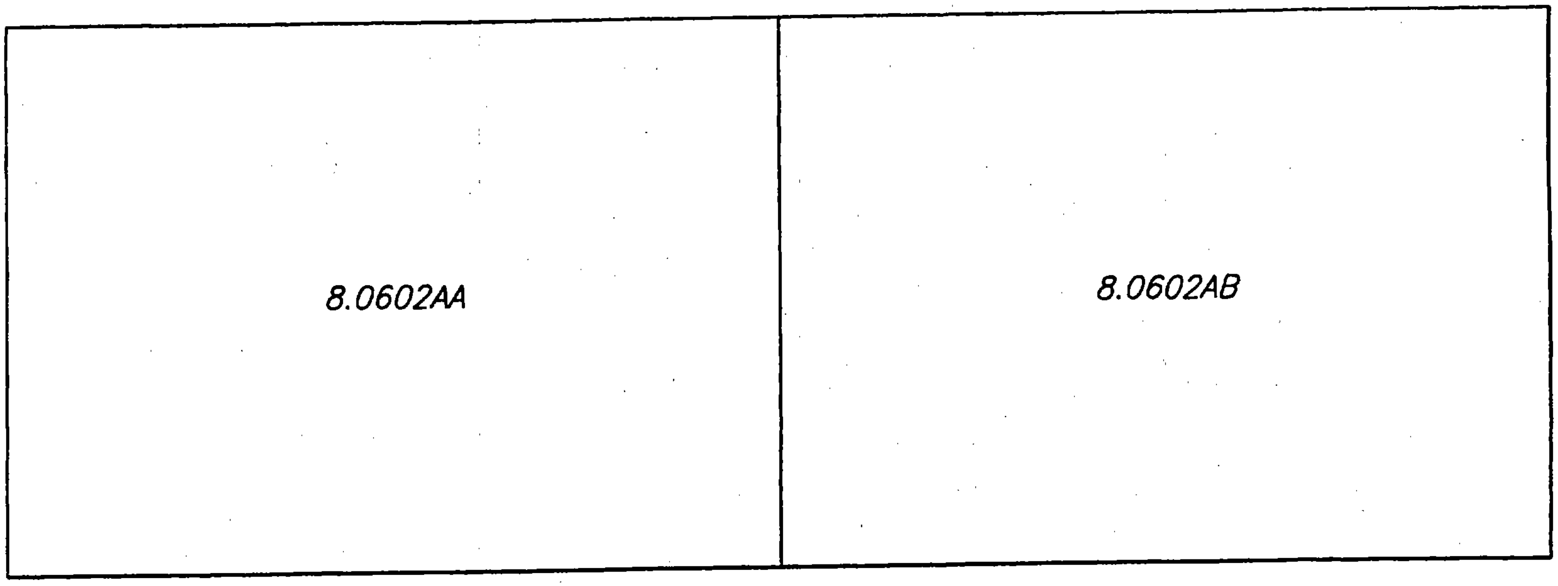
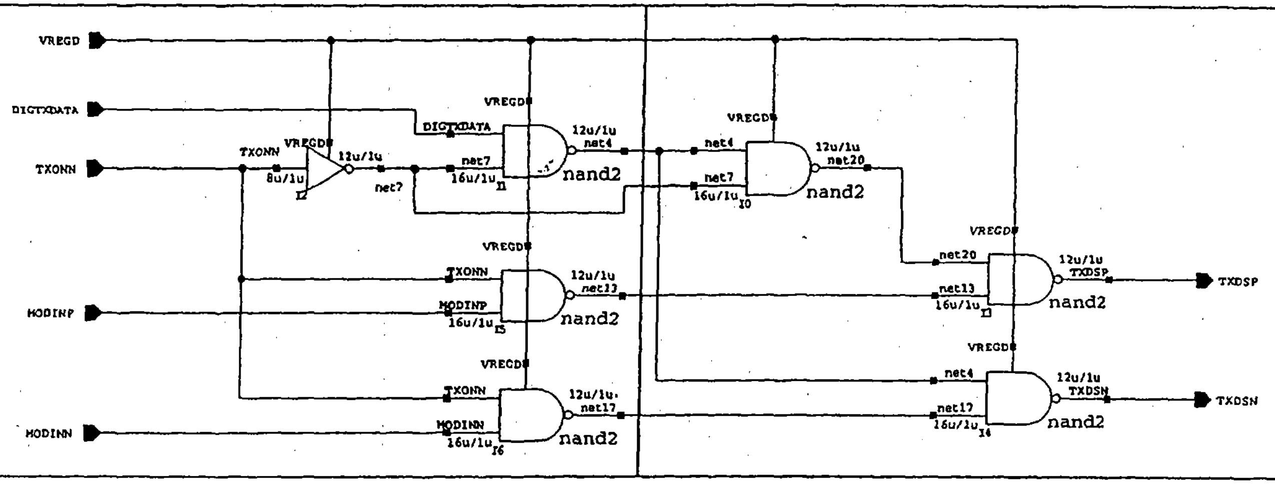


Fig 8.0602



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: Test Mode Data Selector
NAME: 103reva/txdatasel
REV: B1
SIZE: A
DATE: Apr 18 16:05:40 1995
SHEET:

FIG. 8.0602

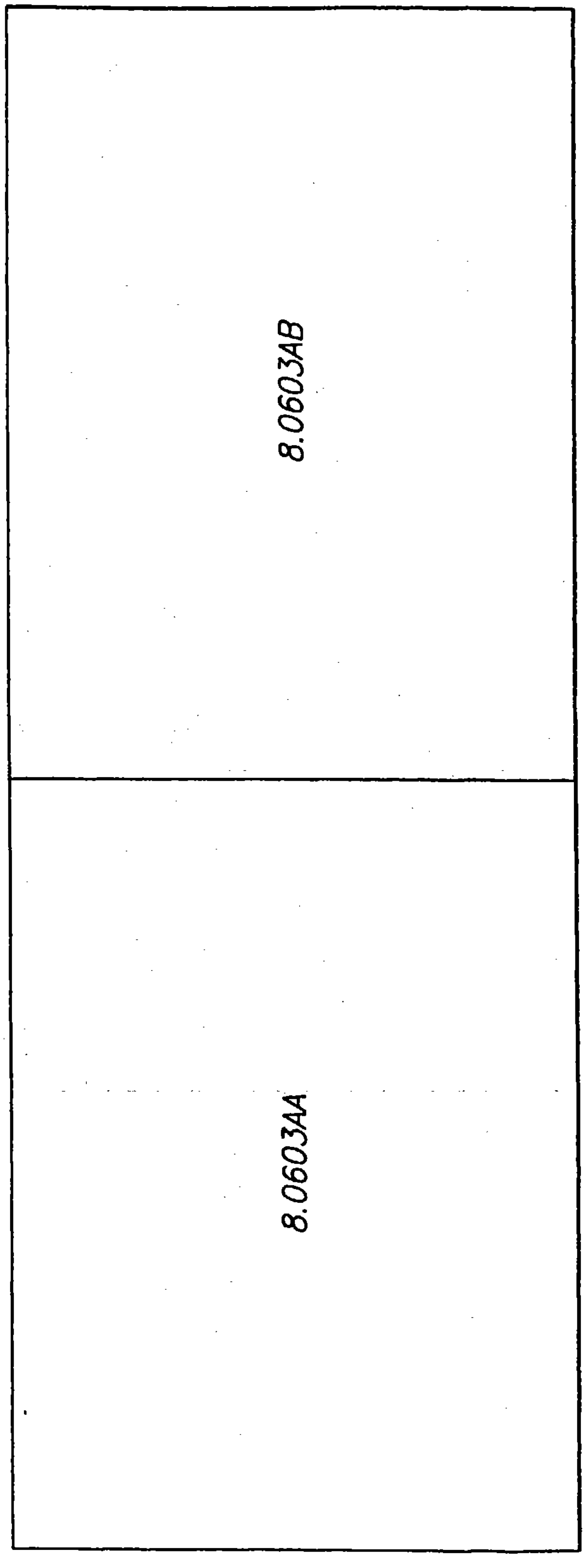


FIG. 8.0603

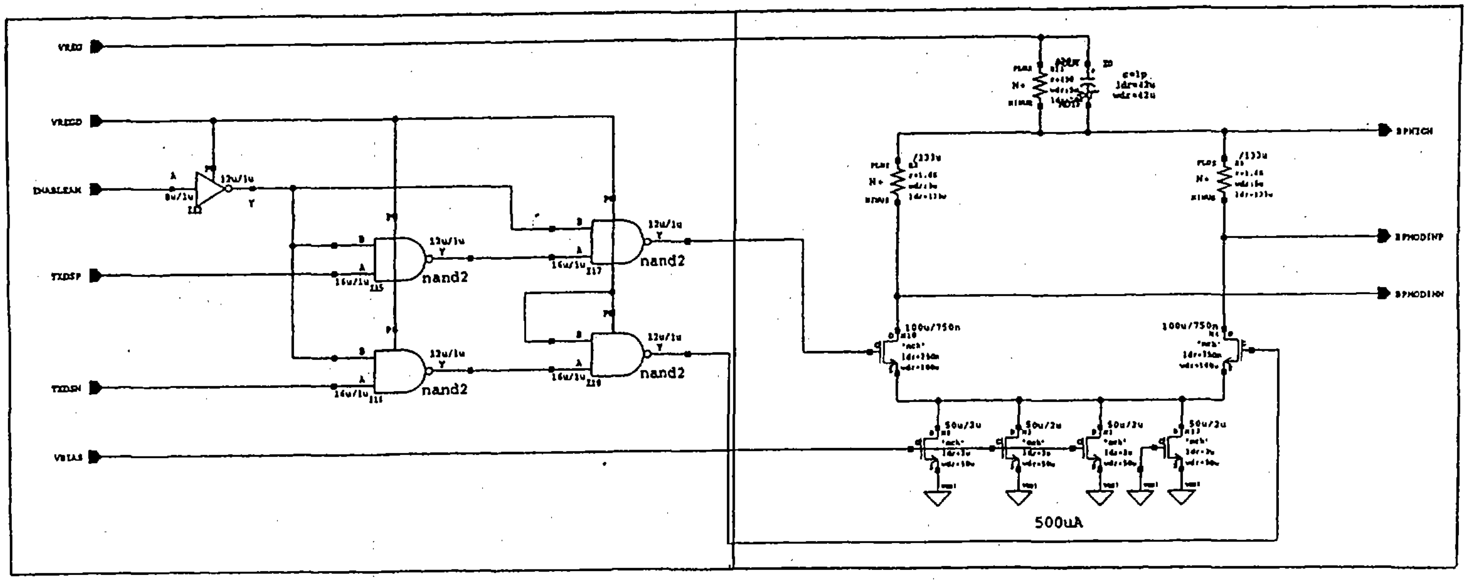


Fig. 8.0603

BB: modified current source

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: BPSK Modulation Driver			
IBIAS=500uA			
NAME: 103reva/txbpsk		REV: B8	FILE: nil
DATE: Jan 18 10:28:46 1996		SHEET:	

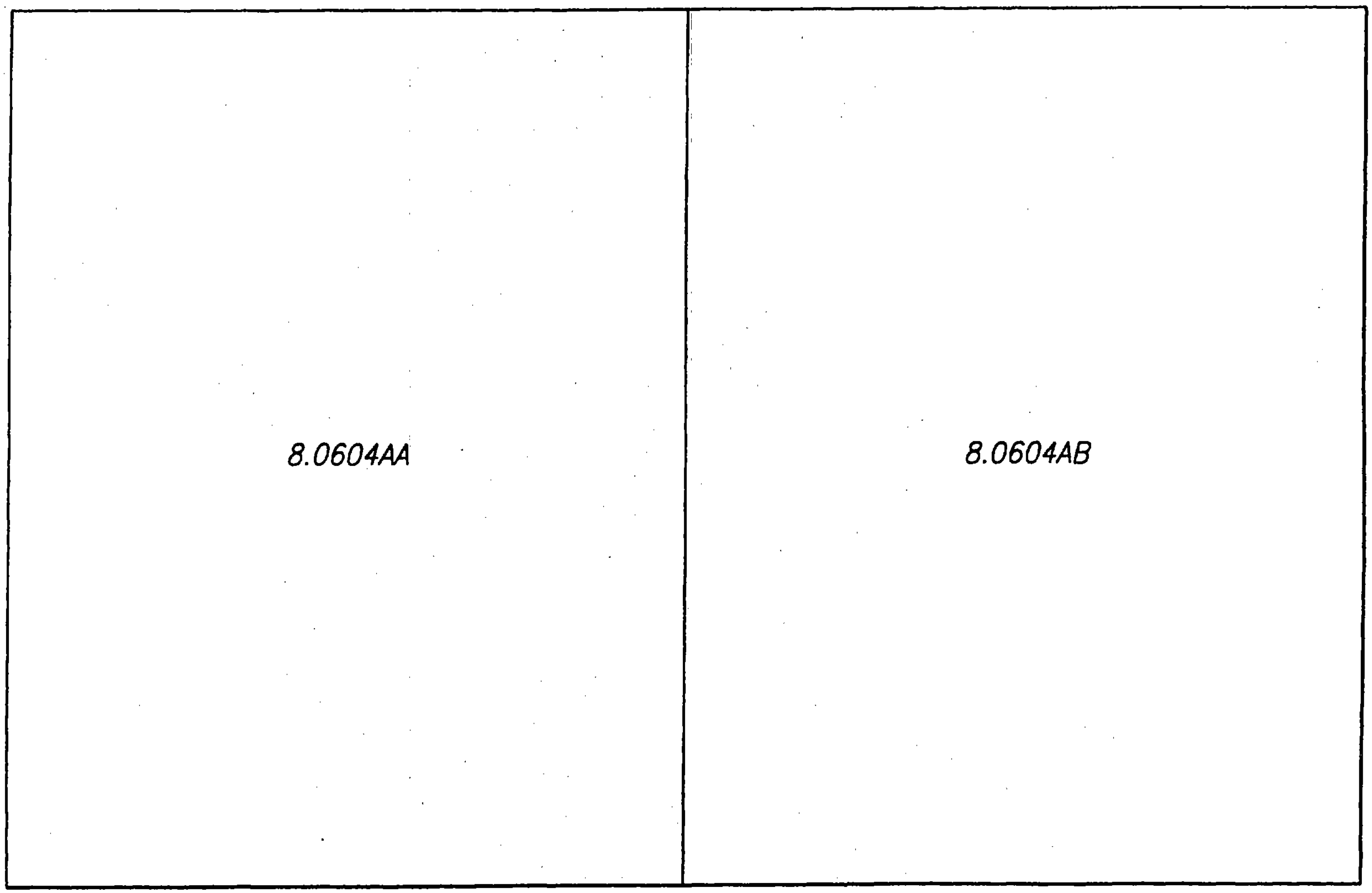


Fig 8.0604

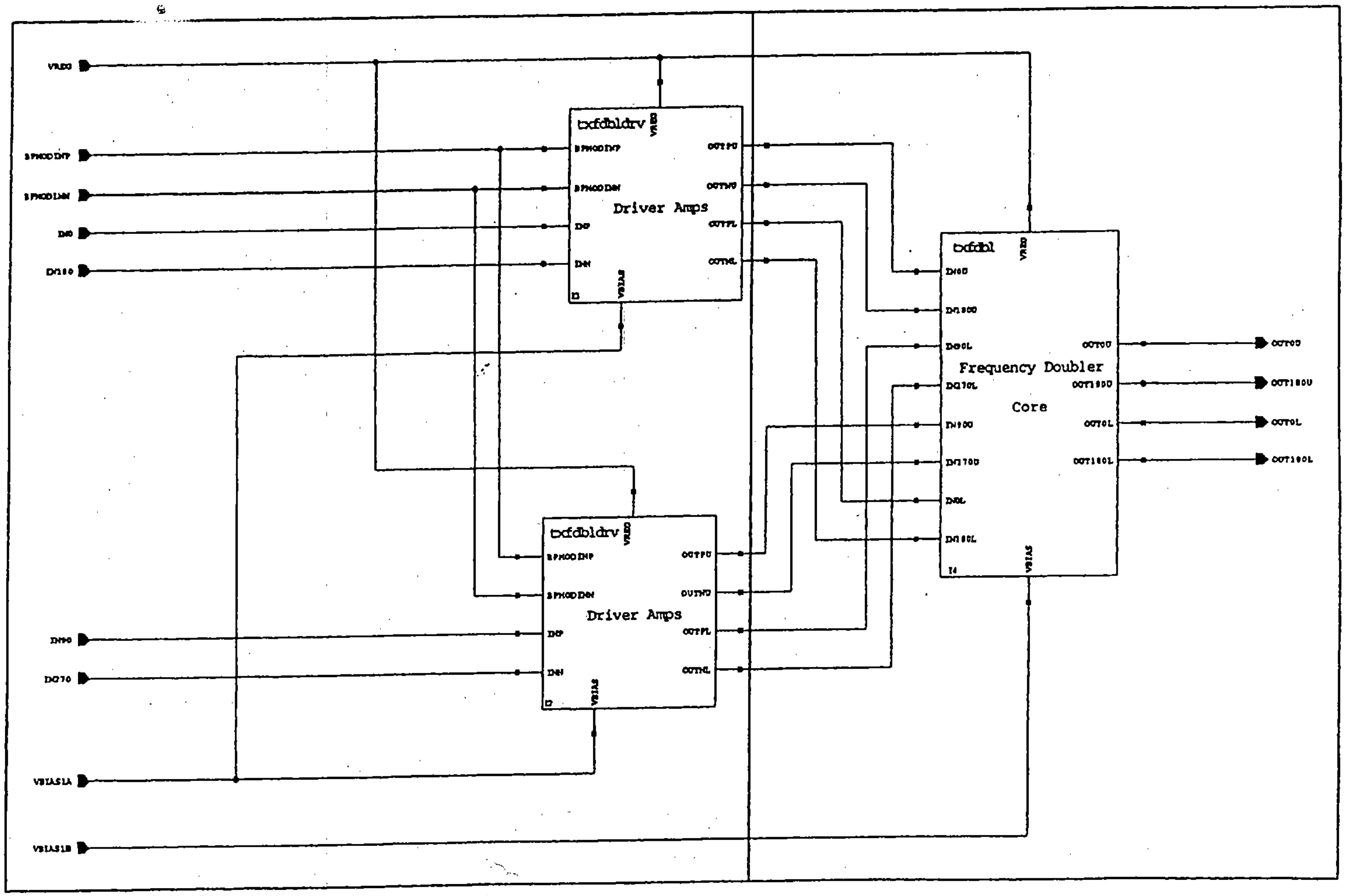


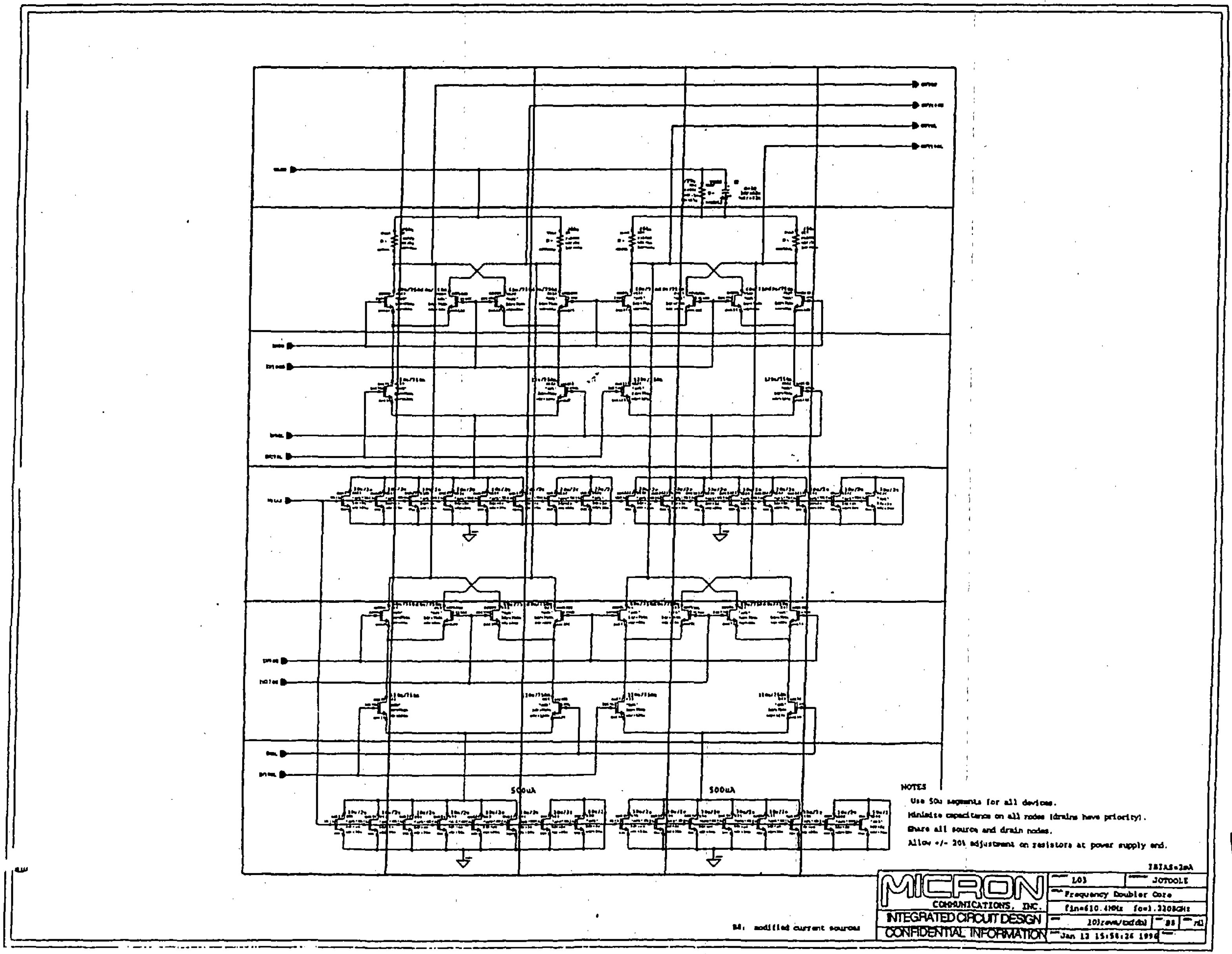
FIG. 8.0604

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: Frequency Doubler
IBIAS=4mA
NAME: 103reva/txdoubler
REV: B1
SIZE: mil
DATE: Apr 5 10:17:13 1995
SHEET:

8.060401AA	8.060401AB	8.060401AC	8.060401AD	8.060401AE
8.060401BA	8.060401BB	8.060401BC	8.060401BD	8.060401BE
8.060401CA	8.060401CB	8.060401CC	8.060401CD	8.060401CE
8.060401DA	8.060401DB	8.060401DC	8.060401DD	8.060401DE
8.060401EA	8.060401EB	8.060401EC	8.060401ED	8.060401EE
8.060401FA	8.060401FB	8.060401FC	8.060401FD	8.060401FE

Fig 8.060401



NOTES

Use 50u segments for all devices.

Minimize capacitance on all nodes (drains have priority).

Share all source and drain nodes.

Allow +/- 20% adjustment on resistors at power supply end.

FIG. 8.060901

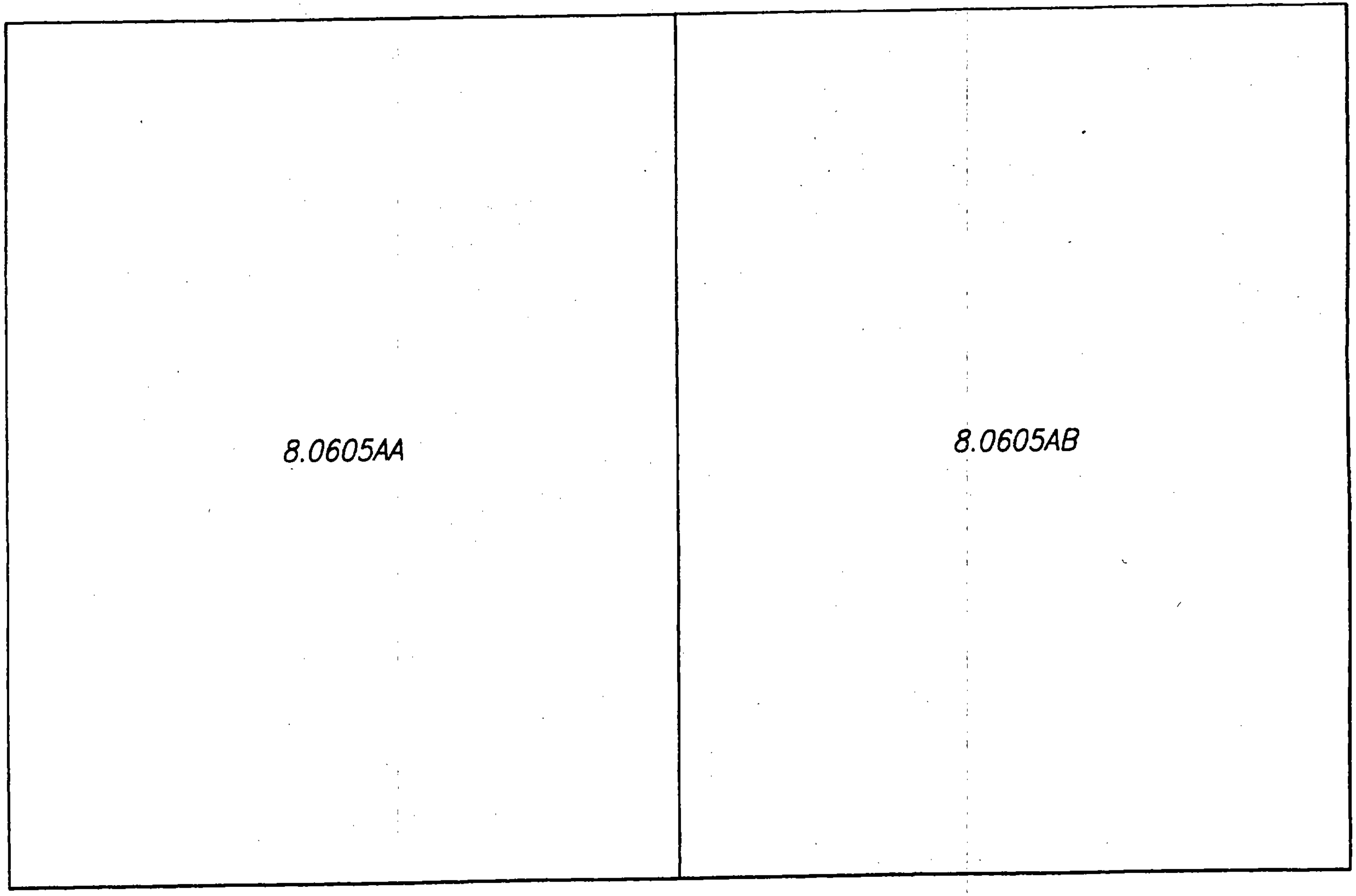


Fig 8.0605

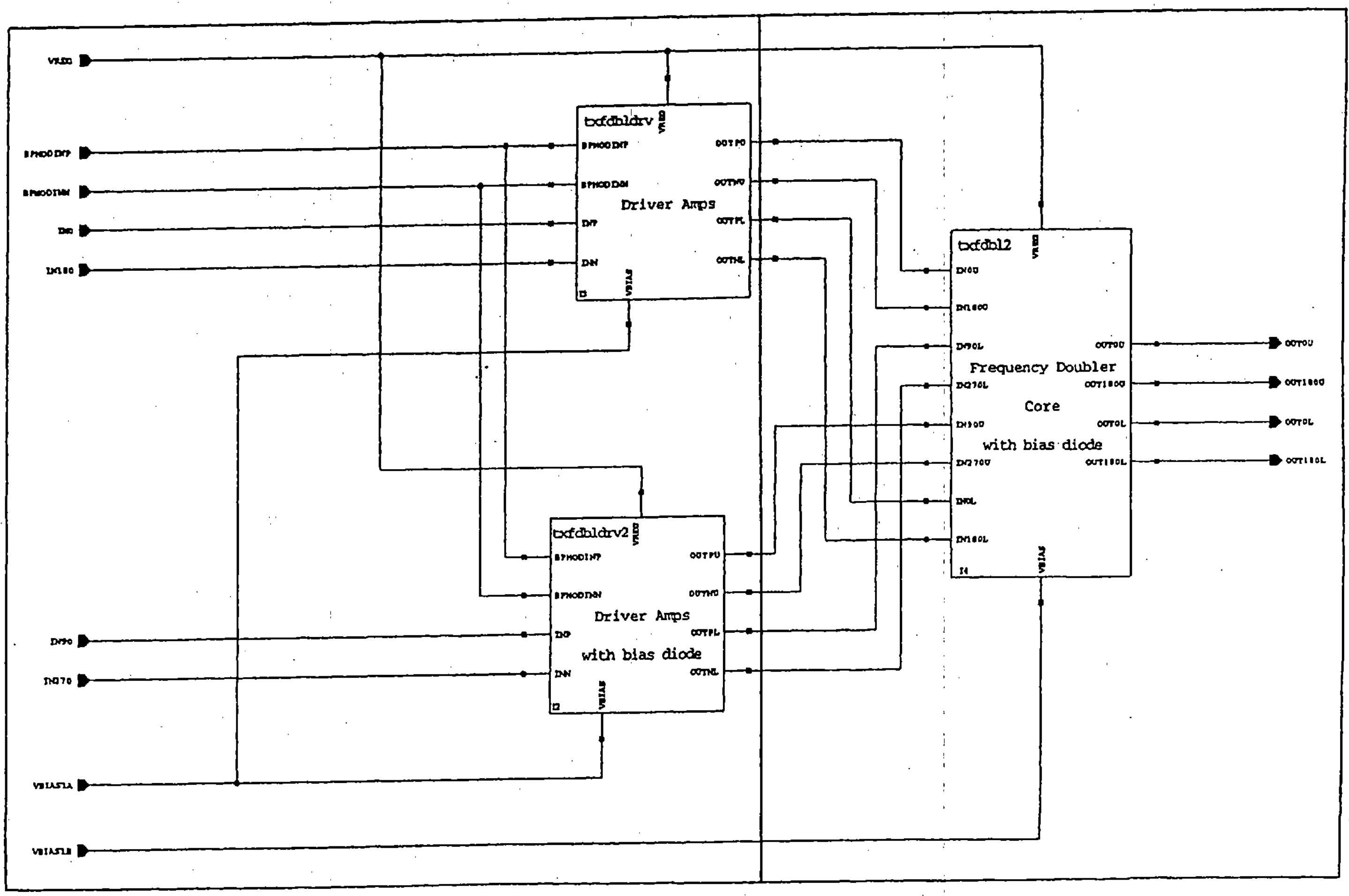


FIG. 8.0605

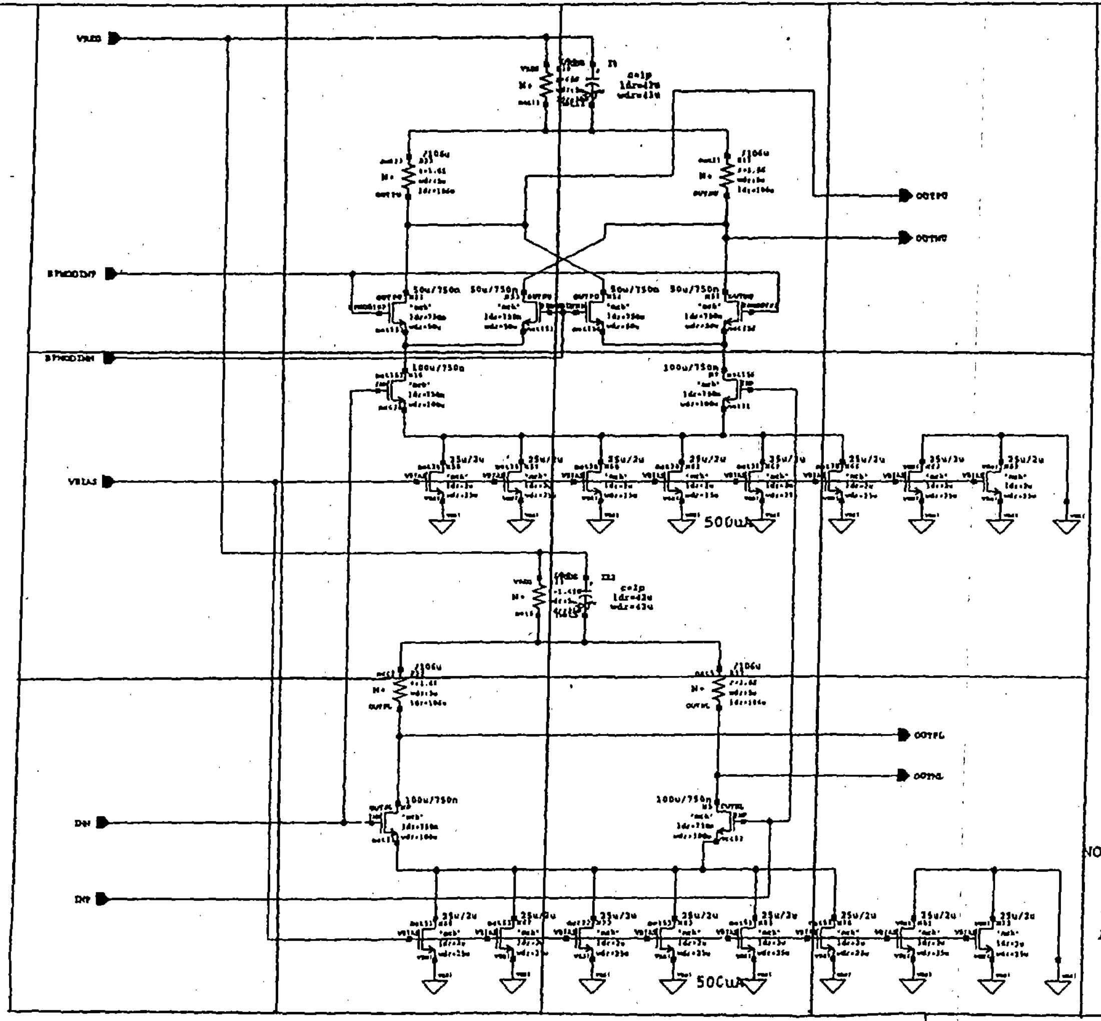
B8: current sources modified

MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Frequency Doubler IBIAS=4mA	
NAME: 103reva/txdoubler2	REV: B8 SIZE: mil
DATE: Jan 12 17:22:51 1996	SHEET:

8.060501AA	8.060501AB	8.060501AC	8.060501AD
8.060501BA	8.060501BB	8.060501BC	8.060501BD
8.060501CA	8.060501CB	8.060501CC	8.060501CD

Fig 8.060501



NOTES

Minimize capacitance on output nodes.

Share all source/drain nodes.

Allow +/- 20% adjustment on resistors
at supply end.

FIG. 8.060501

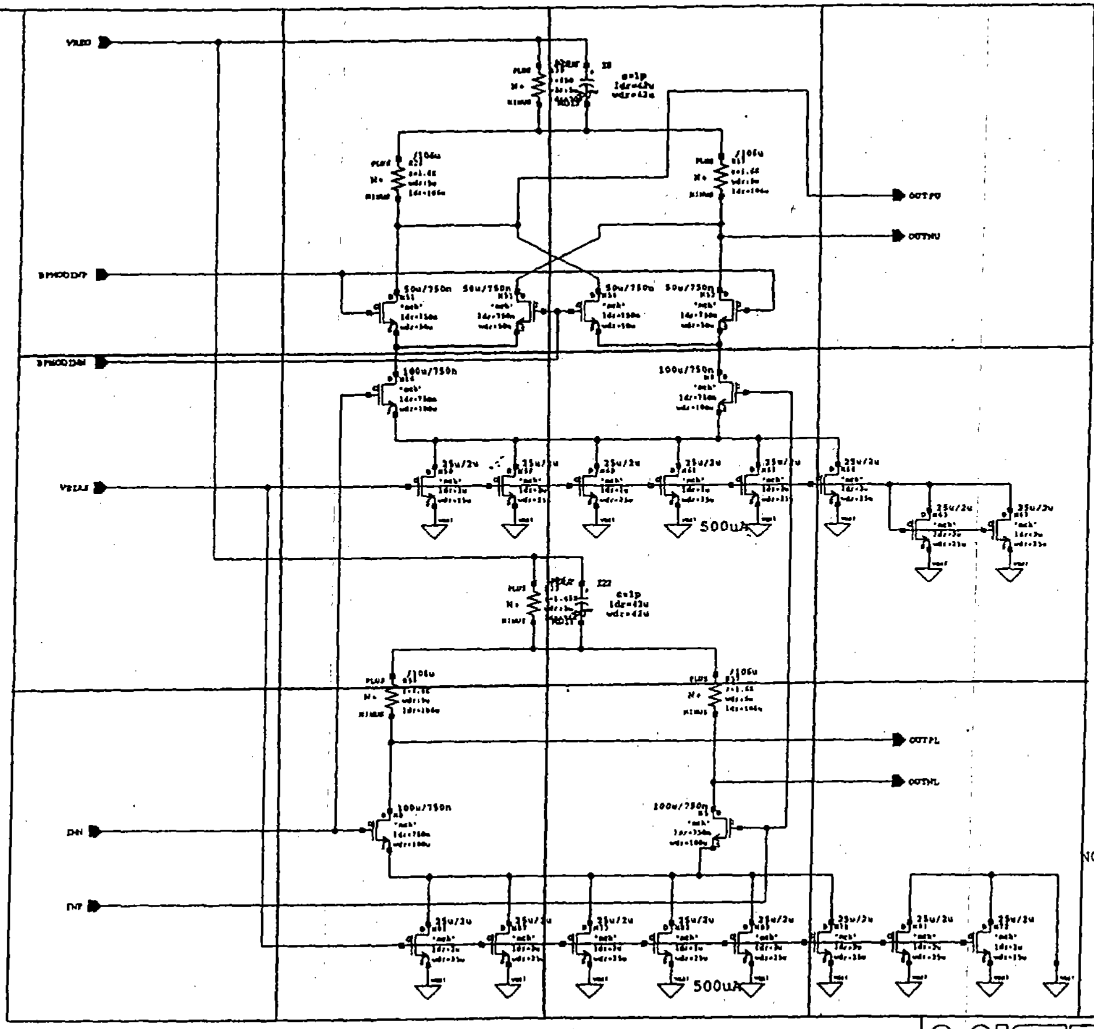
B8: modified current sources

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Doubler Driver Amps IBIAS=1mA	
NAME: 103reva/bdfdbldrv	REV: B8 SCALE: nil
DATE: Jan 12 15:37:26 1996	SHEET:

8.060502AA	8.060502AB	8.060502AC	8.060502AD
8.060502BA	8.060502BB	8.060502BC	8.060502BD
8.060502CA	8.060502CB	8.060502CC	8.060502CD

Fig 8.060502



NOTES

Minimize capacitance on output nodes.

Share all source/drain nodes.

Allow +/- 20% adjustment on resistors at supply end.

FIG. 8.060502

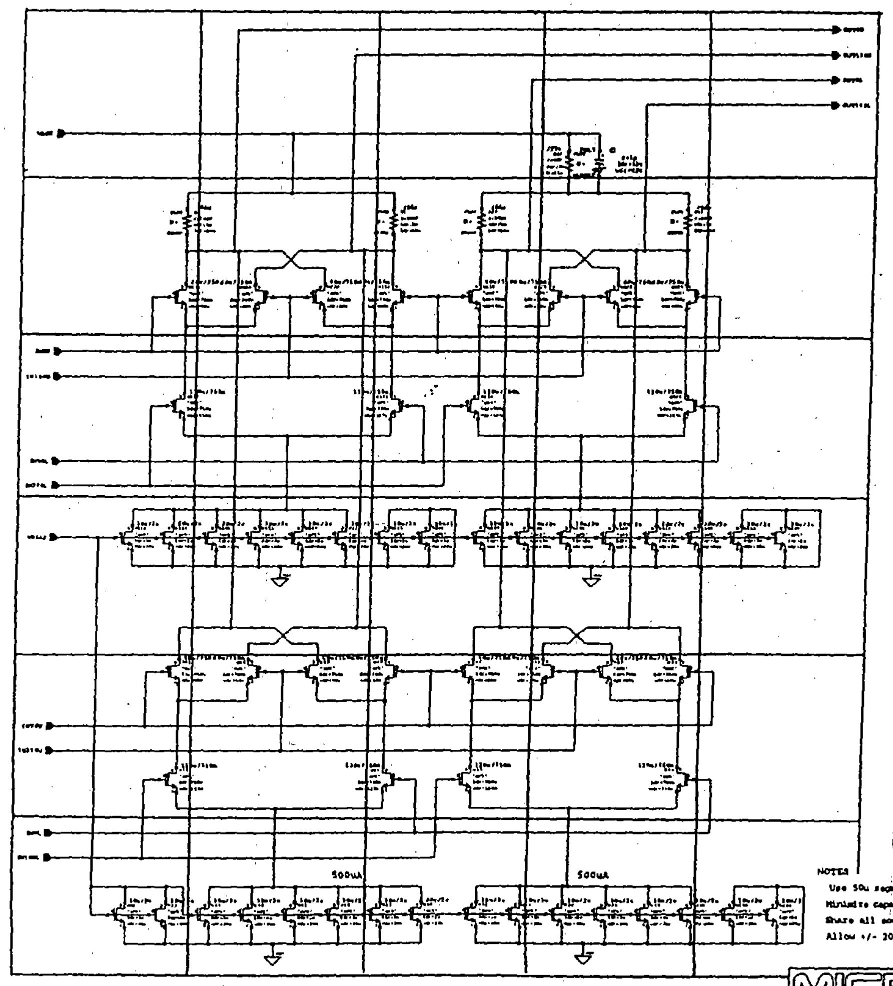
B8: modified current sources

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Doubler Driver Amps	
IBIAS=1mA	
NAME: 103reva/txfdbldrv2	REV: B8 SIZE: nil
DATE: Jan 18 08:22:12 1996	SHEET:

8.060503AA	8.060503AB	8.060503AC	8.060503AD	8.060503AE
8.060503BA	8.060503BB	8.060503BC	8.060503BD	8.060503BE
8.060503CA	8.060503CB	8.060503CC	8.060503CD	8.060503CE
8.060503DA	8.060503DB	8.060503DC	8.060503DD	8.060503DE
8.060503EA	8.060503EB	8.060503EC	8.060503ED	8.060503EE
8.060503FA	8.060503FB	8.060503FC	8.060503FD	8.060503FE

Fig 8.060503



NOTES
Use 50u segments for all devices.
Minimize capacitance on all nodes (drains have priority).
Share all source and drain nodes.
Allow +/- 20% adjustment on resistors at power supply end.

IBIAS=2mA

B4: modified current sources

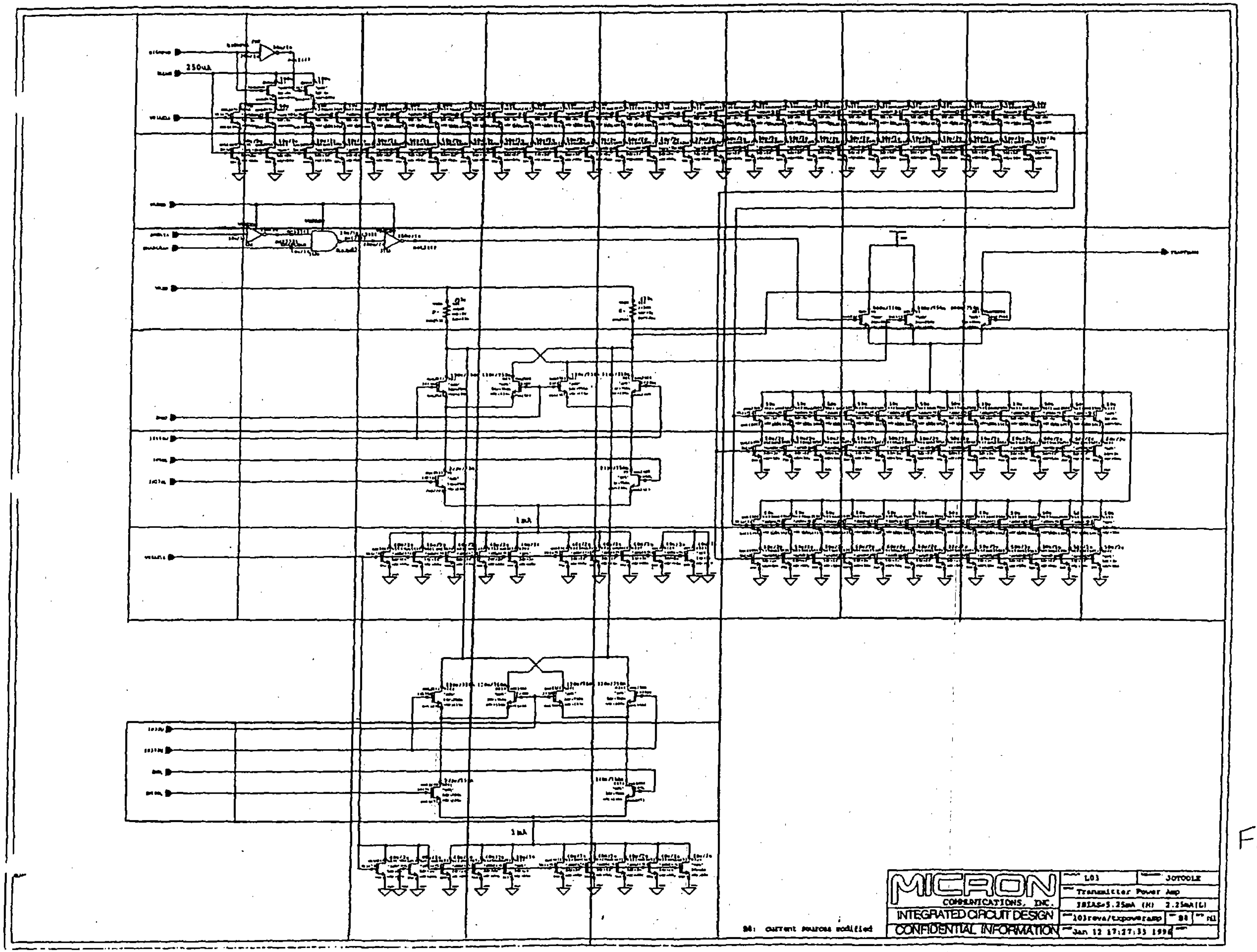
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L01
JOTOOLE
Frequency Doubler Core
fin=610.4MHz fo=1.2208GHz
10)rev4/txfdbl1
B8
r11
Jan 18 08:21:28 1996

FIG. 8.060503

8.0606AA	8.0606AB	8.0606AC	8.0606AD	8.0606AE	8.0606AF	8.0606AG	8.0606AH	
8.0606BA	8.0606BB	8.0606BC	8.0606BD	8.0606BE	8.0606BF	8.0606BG	8.0606BH	
8.0606CA	8.0606CB	8.0606CC	8.0606CD	8.0606CE	8.0606CF	8.0606CG	8.0606CH	8.0606CI
8.0606DA	8.0606DB	8.0606DC	8.0606DD	8.0606DE	8.0606DF	8.0606DG	8.0606DH	8.0606DI
8.0606EA	8.0606EB	8.0606EC	8.0606ED	8.0606EE	8.0606EF	8.0606EG	8.0606EH	8.0606EI
8.0606FA	8.0606FB	8.0606FC	8.0606FD	8.0606FE	8.0606FF	8.0606FG	8.0606FH	8.0606FI
		8.0606GC	8.0606GD	8.0606GE				
8.0606HA	8.0606HB	8.0606HC	8.0606HD	8.0606HE				
	8.0606IB	8.0606IC	8.0606ID	8.0606IE				

FIG 8.0606



08: current sources modified

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03	JOTOOLE
Transmitter Power Amp	
IBIAS=5.25mA (H) 2.25mA(L)	
103reva/txpoweramp	08
Jan 12 17:27:33 1996	

FIG. 8.0606

8.0607AA	8.0607AB	8.0607AC	8.0607AD	8.0607AE	8.0607AF	8.0607AG	8.0607AH	8.0607AI	8.0607AJ
8.0607BA	8.0607BB	8.0607BC	8.0607BD	8.0607BE	8.0607BF	8.0607BG	8.0607BH	8.0607BI	8.0607BJ
8.0607CA	8.0607CB	8.0607CC	8.0607CD	8.0607CE	8.0607CF	8.0607CG	8.0607CH	8.0607CI	8.0607CJ
8.0607DA	8.0607DB	8.0607DC	8.0607DD	8.0607DE	8.0607DF	8.0607DG	8.0607DH	8.0607DI	8.0607DJ
8.0607EA	8.0607EB	8.0607EC	8.0607ED	8.0607EE	8.0607EF	8.0607EG	8.0607EH	8.0607EI	8.0607EJ
8.0607FA	8.0607FB	8.0607FC	8.0607FD	8.0607FE	8.0607FF	8.0607FG	8.0607FH	8.0607FI	8.0607FJ
8.0607GA	8.0607GB	8.0607GC	8.0607GD	8.0607GE	8.0607GF	8.0607GG	8.0607GH	8.0607GI	8.0607GJ
8.0607HA	8.0607HB	8.0607HC	8.0607HD	8.0607HE	8.0607HF	8.0607HG	8.0607HH	8.0607HI	8.0607HJ
8.0607IA	8.0607IB	8.0607IC	8.0607ID	8.0607IE	8.0607IF	8.0607IG	8.0607IH	8.0607II	8.0607IJ
8.0607JA	8.0607JB	8.0607JC	8.0607JD	8.0607JE	8.0607JF	8.0607JG	8.0607JH	8.0607JI	8.0607JJ

Fig 8.0607

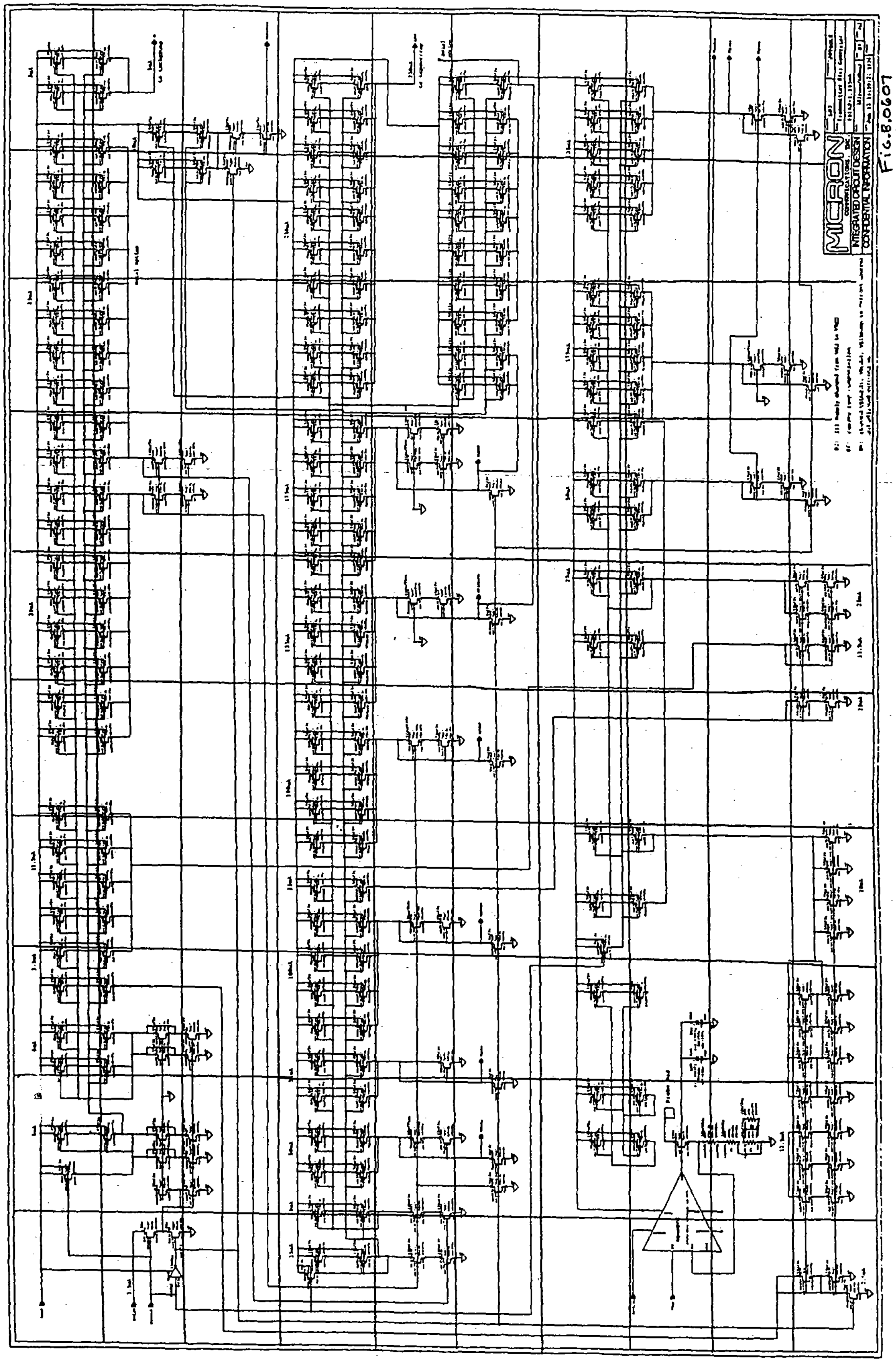

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

FIG.8.0607

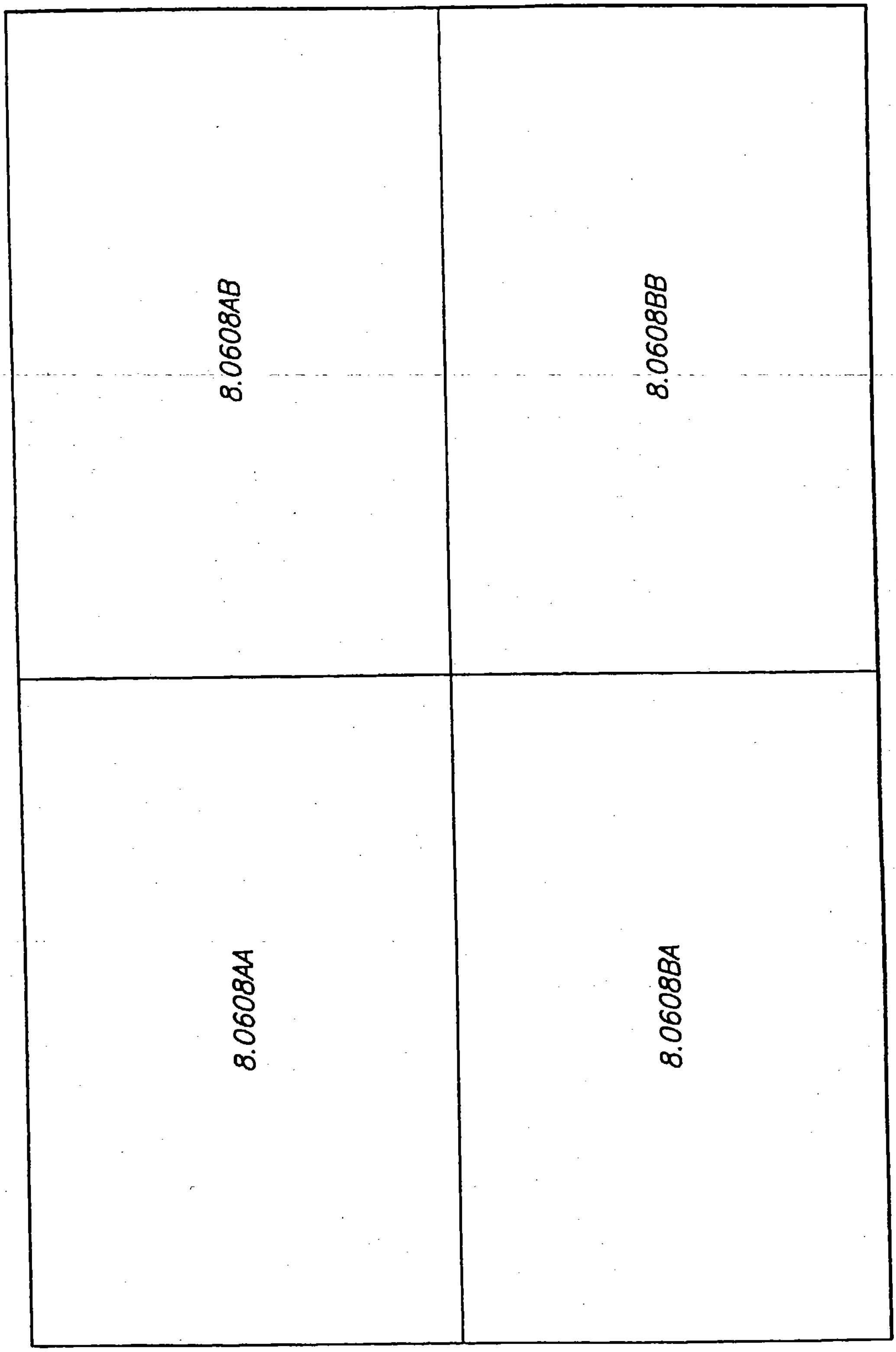
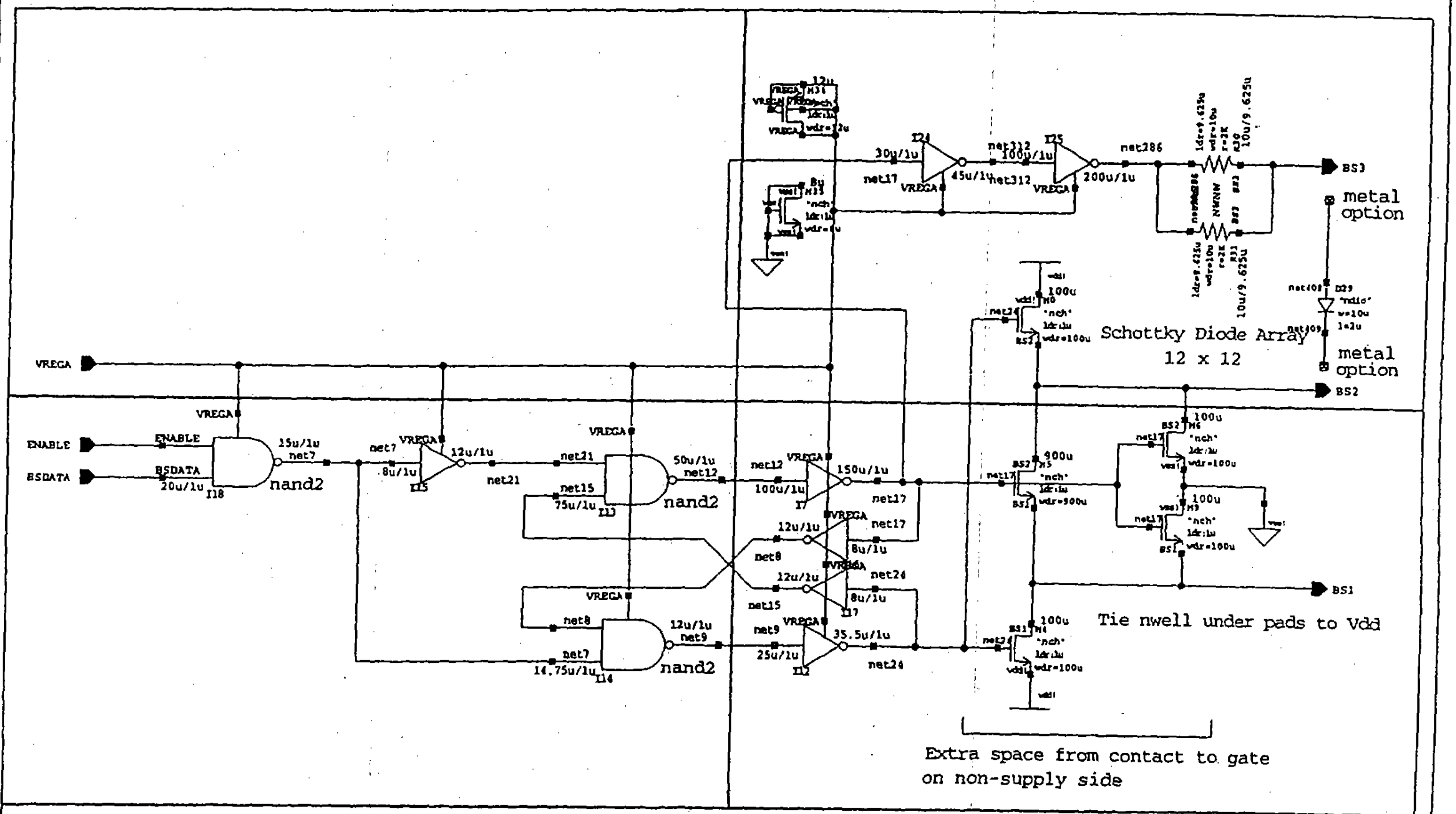


Fig. 8.0608



B8: initial release of this design

B10: disconnected inverter

MICRON

COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Modulated Backscatter Transmitter	
NAME: 103reva/txmbs	REV: B10 SIZE: A
DATE: Mar 26 11:07:42 1996	SHEET:

FIG. 8.0608

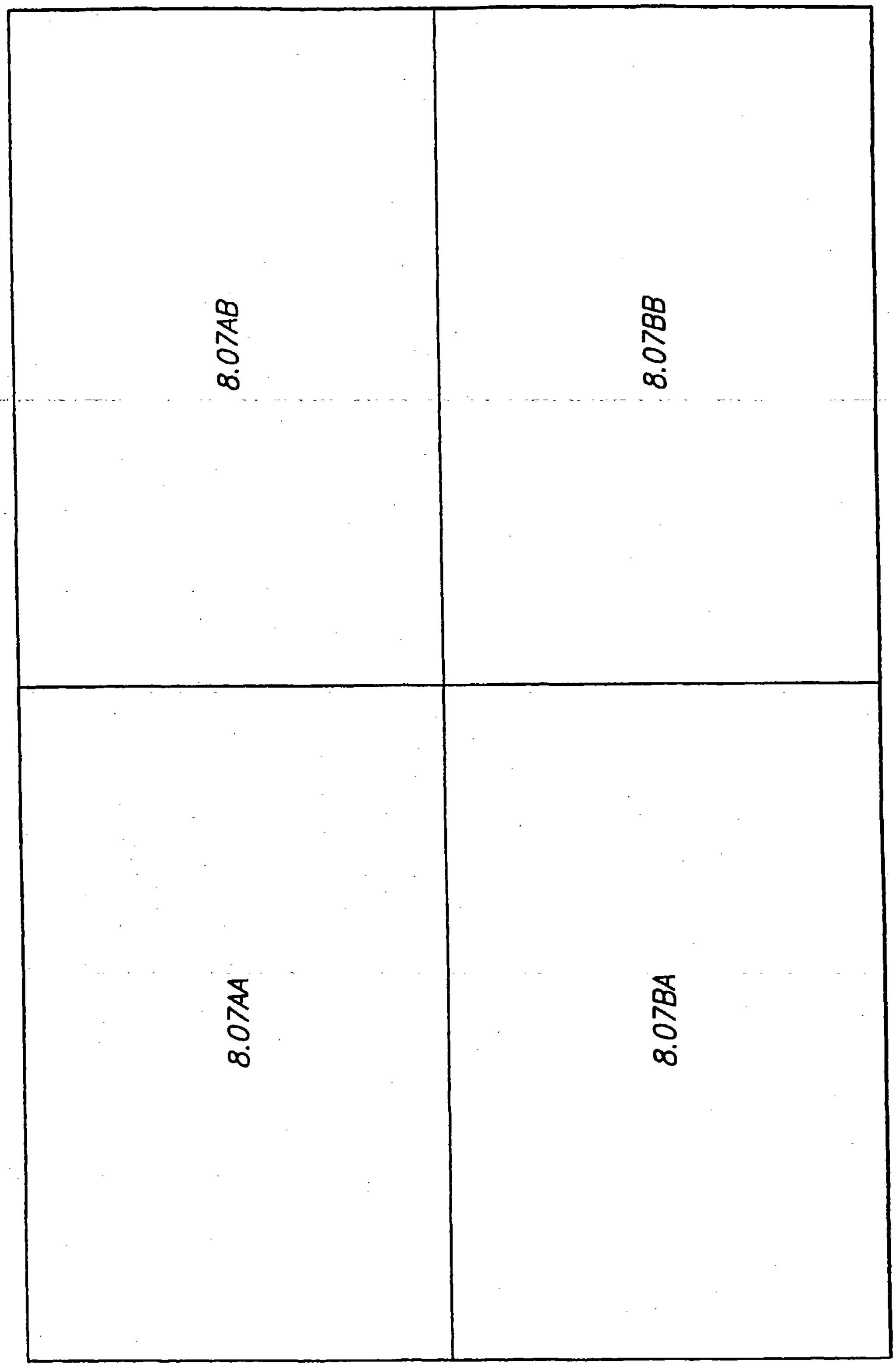


Fig. 8.07

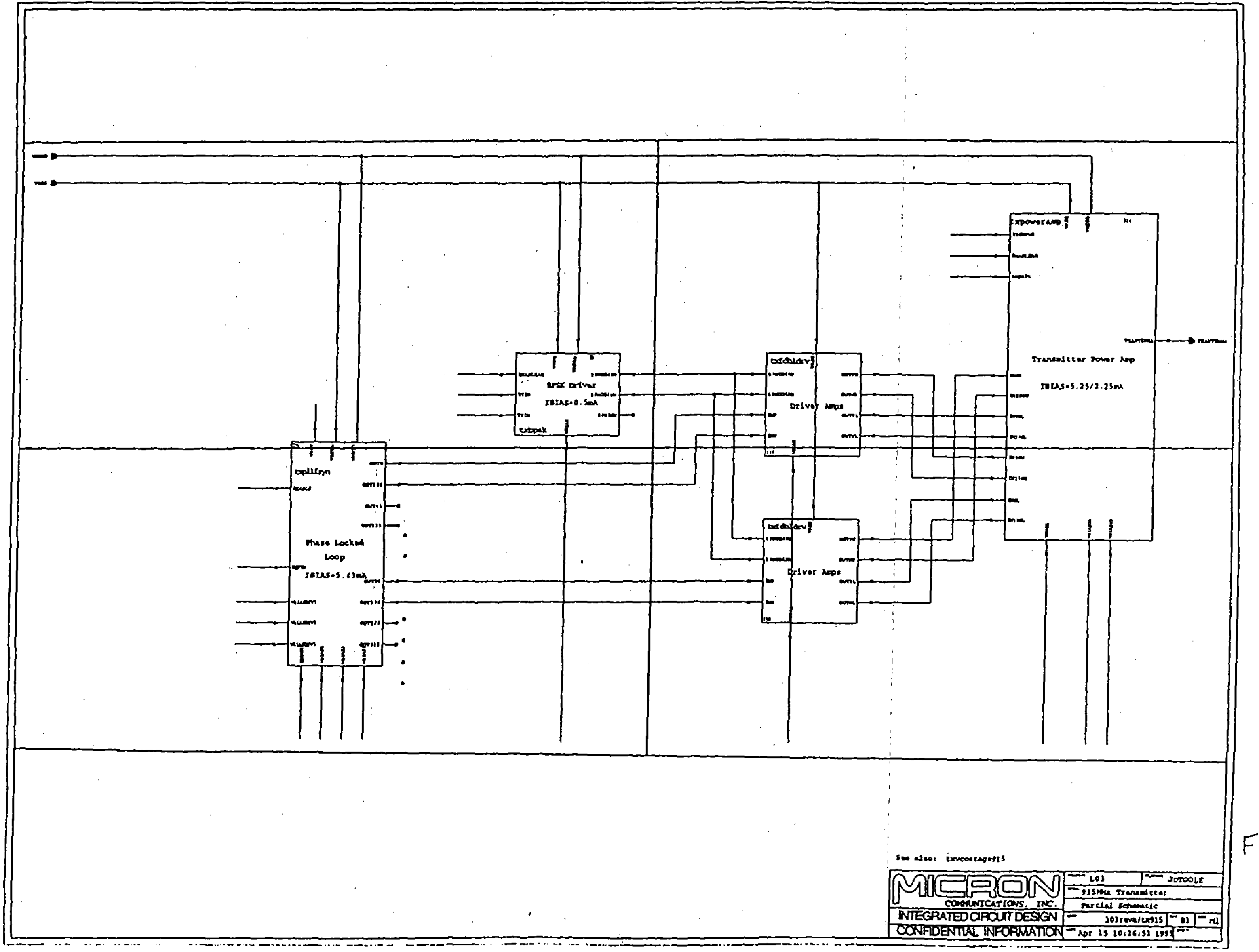
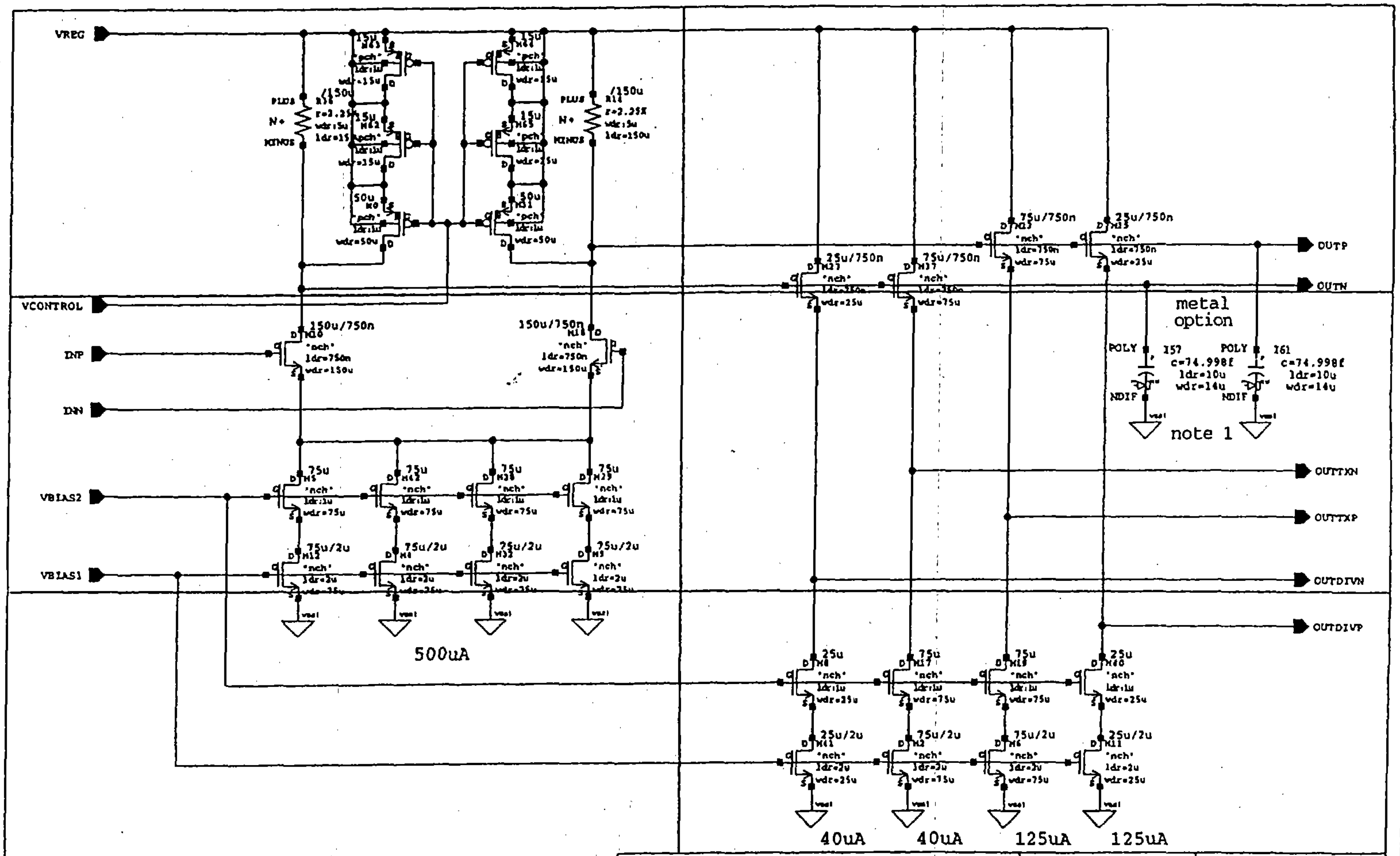

txpllfsyn
Phase Locked
Loop
IBIAS=5.43mA
BPSK Driver
IBIAS=0.5mA
txbpsk
txdbldrv
Driver Amps
txdbldrv
Driver Amps
txpoweramp
Transmitter Power Amp
IBIAS=5.25/2.25mA
See also: txvcostage915
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
JOTOOLE
915MHz Transmitter
Partial Schematic
303reva/tx915
B1
rd1
Apr 15 10:26:53 1995

FIG. 8.07

8.0701AA	8.0701AB
8.0701BA	8.0701BB
8.0701CA	8.0701CB

Fig. 8.0701



Notes: 1. Caps are used for 915MHz metal option.
Allow L adjustment up to 14um.
Tie each to an isolated n+ region.

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: TX VCO Stage for 915MHz
IBIAS=833uA
NAME: 103reva/txvcostage915
REV: B1
SIZE: A
DATE: Apr 15 10:23:19 1995
SHEET:

FIG. 8.0701

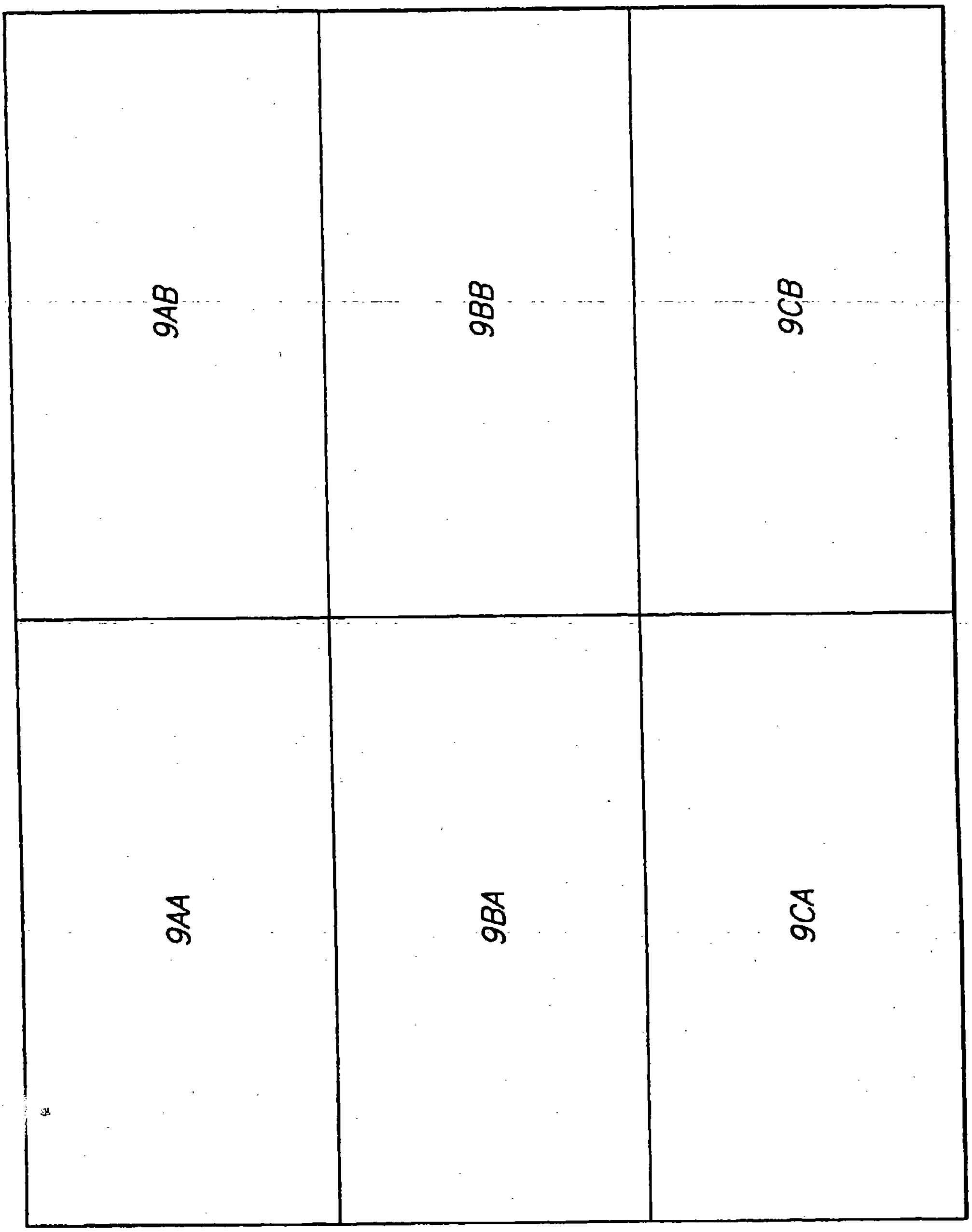
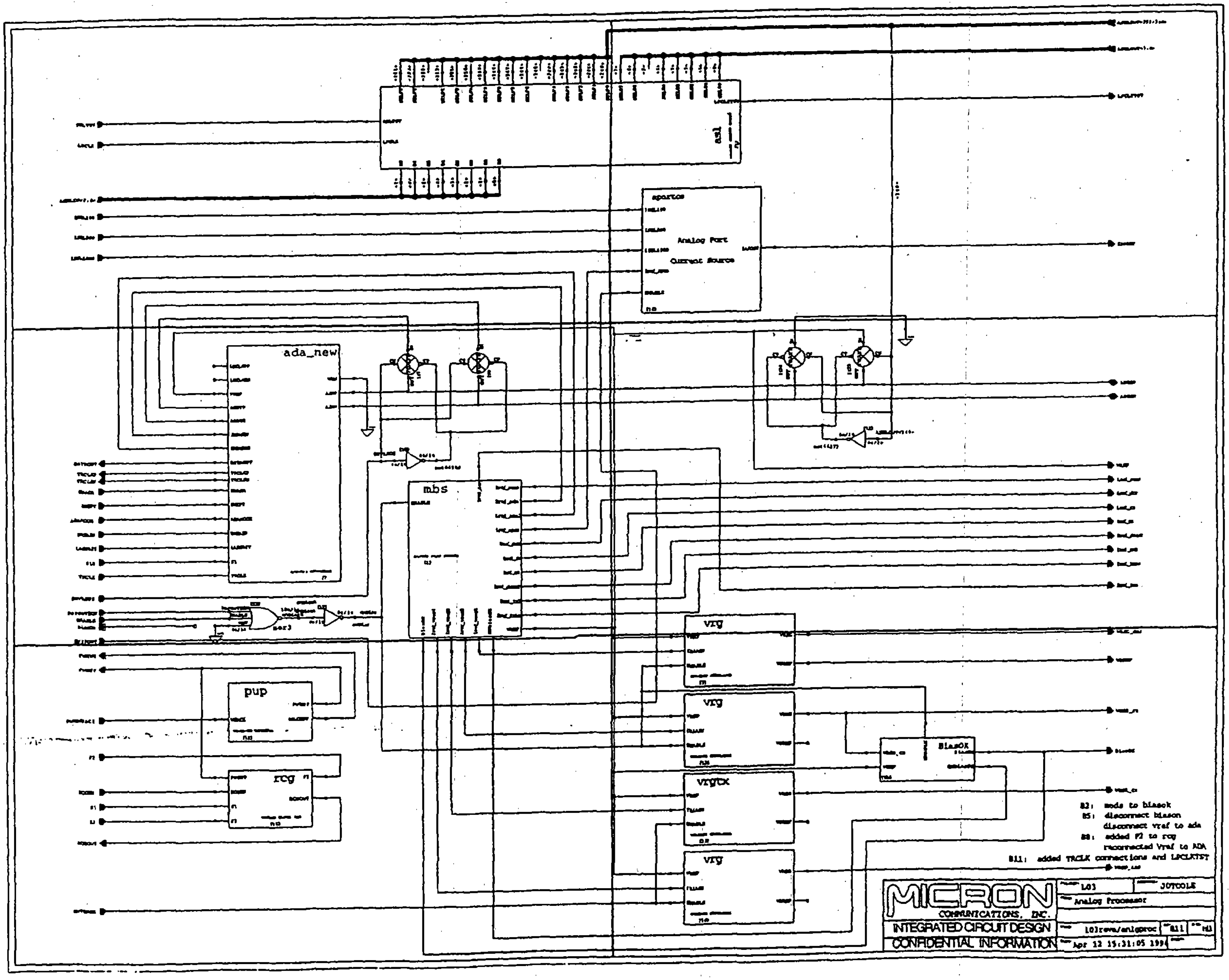


FIG. 9


asl
aportcs
Analog Port
Current Source
ada_new
mbs
vrg
vrg
vrgtx
vrg
BiasOK
pup
rcg
B2: mode to biasok
B5: disconnect biason
disconnect vref to ada
B8: added F2 to rcg
reconnected Vref to ADA
B11: added TRCLK connections and LPCLKTST
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
JOTCOLE
Analog Processor
l03reva/anlgproc
B11
H1
Apr 12 15:31:05 199

F16. 9

9.01AA	9.01AB	9.01AC	9.01AD	9.01AE	9.01AF	9.01AG	9.01AH
9.01BA	9.01BB	9.01BC	9.01BD	9.01BE	9.01BF	9.01BG	9.01BH
9.01CA	9.01CB	9.01CC	9.01CD	9.01CE	9.01CF	9.01CG	9.01CH
9.01DA	9.01DB	9.01DC	9.01DD	9.01DE	9.01DF	9.01DG	9.01DH

Fig. 9.01

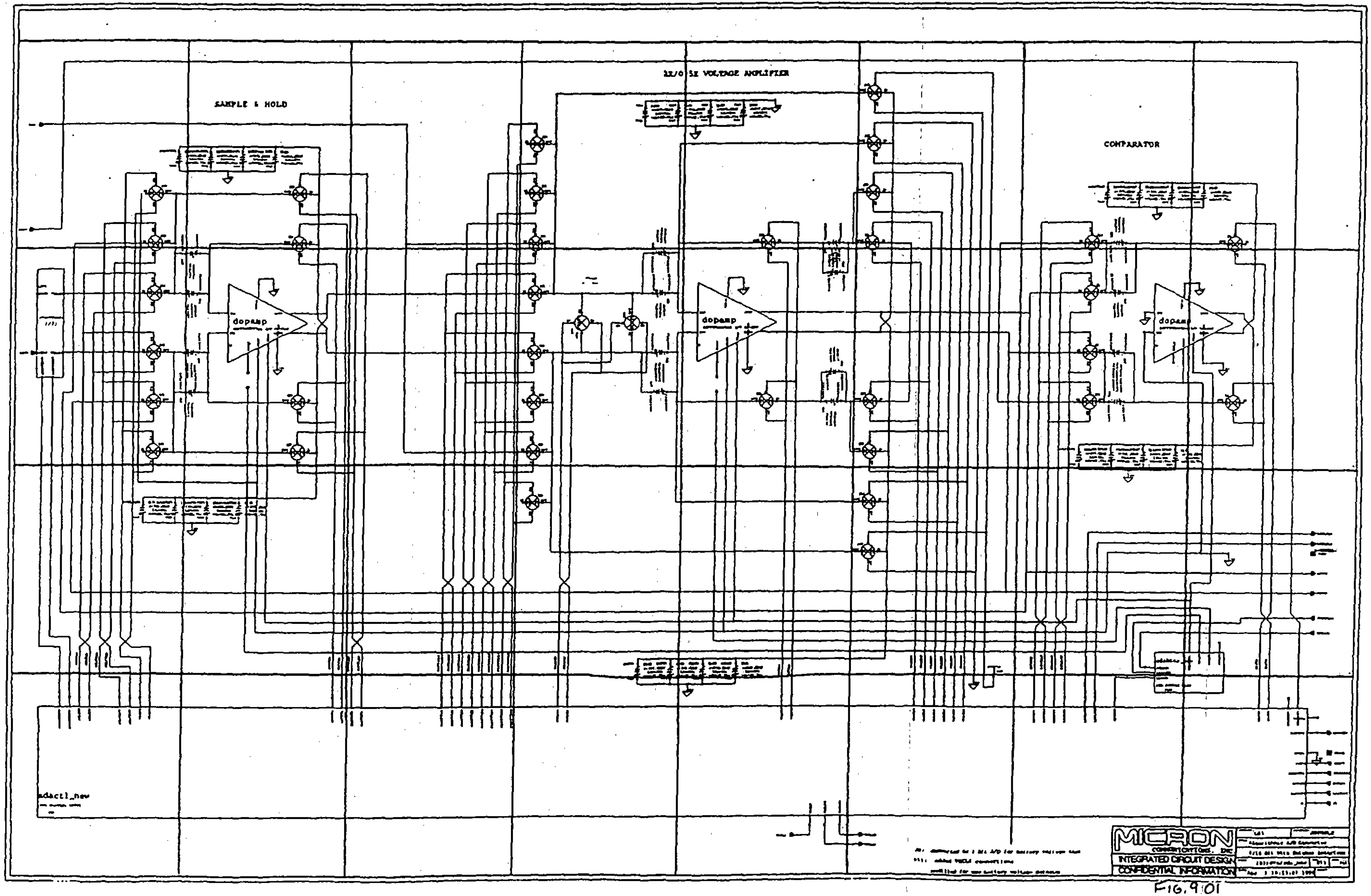

SAMPLE & HOLD
1X/0.5X VOLTAGE AMPLIFIER
COMPARATOR
dopamp
dopamp
dopamp
adactl_new
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

FIG. 9.01

9.0101AA	9.0101AB	9.0101AC	9.0101AD	9.0101AE	9.0101AF	9.0101AG	9.0101AH	9.0101AI	9.0101AJ	9.0101AK
9.0101BA	9.0101BB	9.0101BC	9.0101BD	9.0101BE	9.0101BF	9.0101BG	9.0101BH	9.0101BI	9.0101BJ	9.0101BK
9.0101CA	9.0101CB	9.0101CC	9.0101CD	9.0101CE	9.0101CF	9.0101CG	9.0101CH	9.0101CI	9.0101CJ	9.0101CK

Fig 9.0101

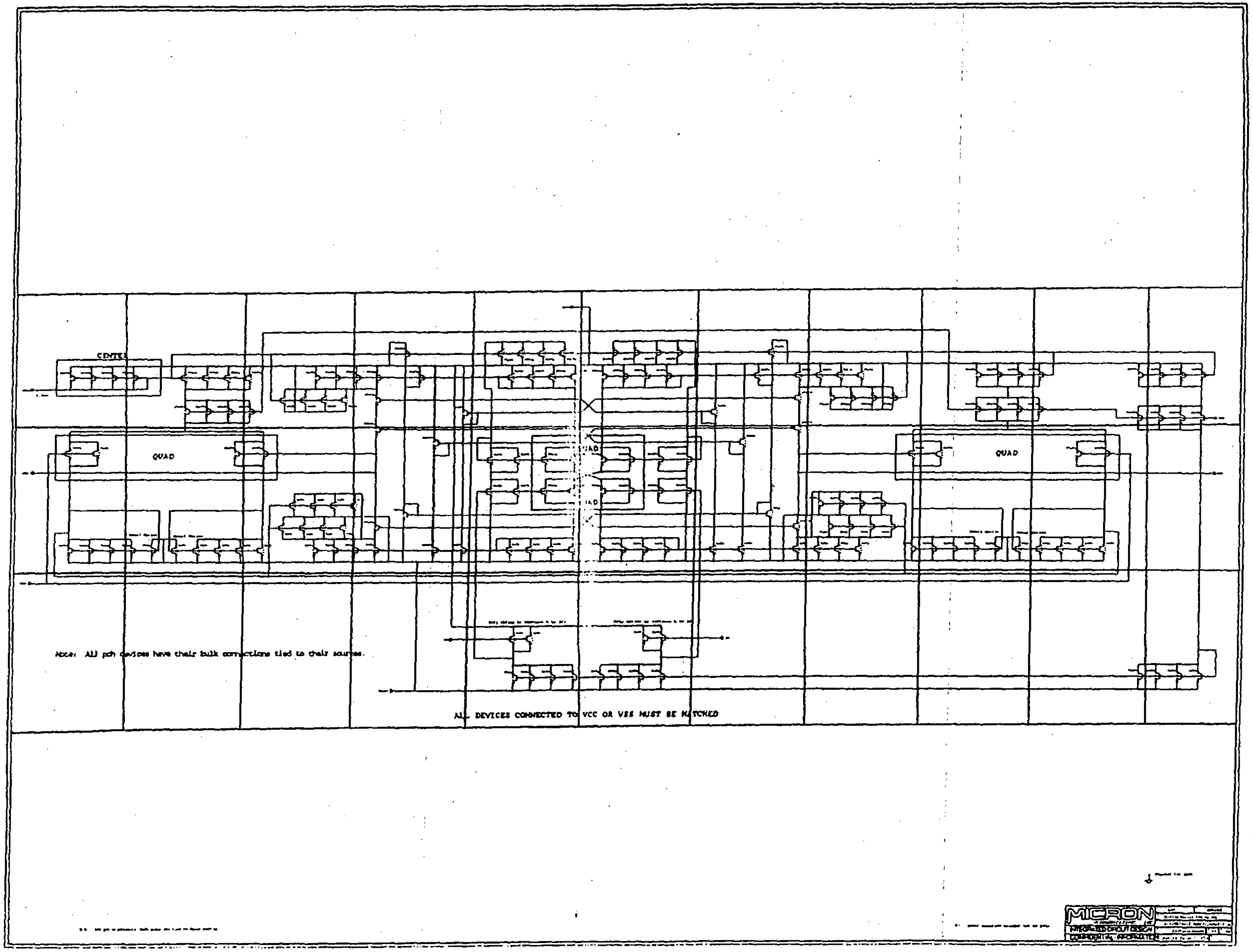
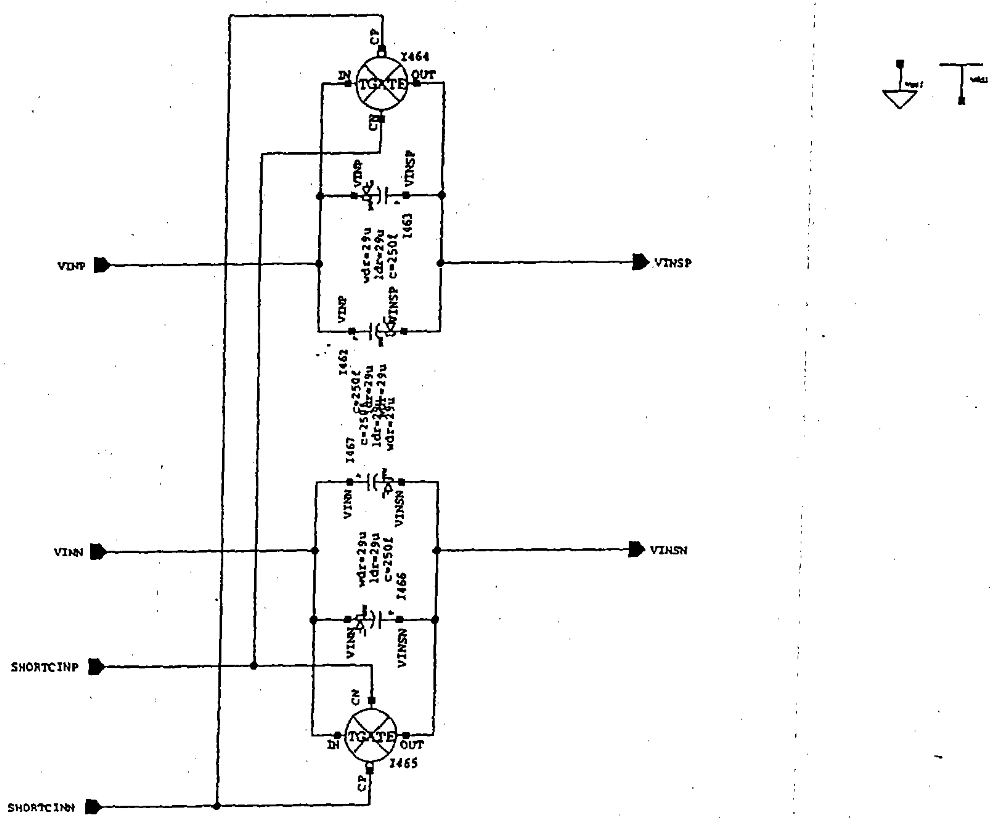

CENTER
QUAD
QUAD
QUAD
QUAD
Note: All pch devices have their bulk connections tied to their sources.
ALL DEVICES CONNECTED TO VCC OR VSS MUST BE MATCHED
MICRON
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

FIG. 9.0101



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: Analog Divide by 2
NAME: 103reva/adaprescale
REV: B1
SIZE: A
DATE: May 19 16:34:53 1995
SHEET:

FIG. 9.0102

									9.0103AJ	9.0103AK	9.0103AL	9.0103AM	9.0103AN	9.0103AO	9.0103AP
9.0103BA	9.0103BB	9.0103BC	9.0103BD	9.0103BE	9.0103BF	9.0103BG	9.0103BH		9.0103BJ	9.0103BK	9.0103BL	9.0103BM	9.0103BN	9.0103BO	9.0103BP
9.0103CA	9.0103CB	9.0103CC	9.0103CD	9.0103CE	9.0103CF	9.0103CG	9.0103CH	9.0103CI	9.0103CJ	9.0103CK	9.0103CL	9.0103CM	9.0103CN	9.0103CO	9.0103CP
9.0103DA	9.0103DB	9.0103DC	9.0103DD	9.0103DE	9.0103DF	9.0103DG	9.0103DH	9.0103DI	9.0103DJ	9.0103DK	9.0103DL	9.0103DM	9.0103DN	9.0103DO	9.0103DP
9.0103EA	9.0103EB	9.0103EC	9.0103ED	9.0103EE	9.0103EF	9.0103EG	9.0103EH	9.0103EI	9.0103EJ	9.0103EK	9.0103EL	9.0103EM	9.0103EN	9.0103EO	9.0103EP
9.0103FA	9.0103FB	9.0103FC	9.0103FD	9.0103FE	9.0103FF	9.0103FG	9.0103FH	9.0103FI	9.0103FJ	9.0103FK	9.0103FL	9.0103FM	9.0103FN	9.0103FO	9.0103FP

FIG 9.0103

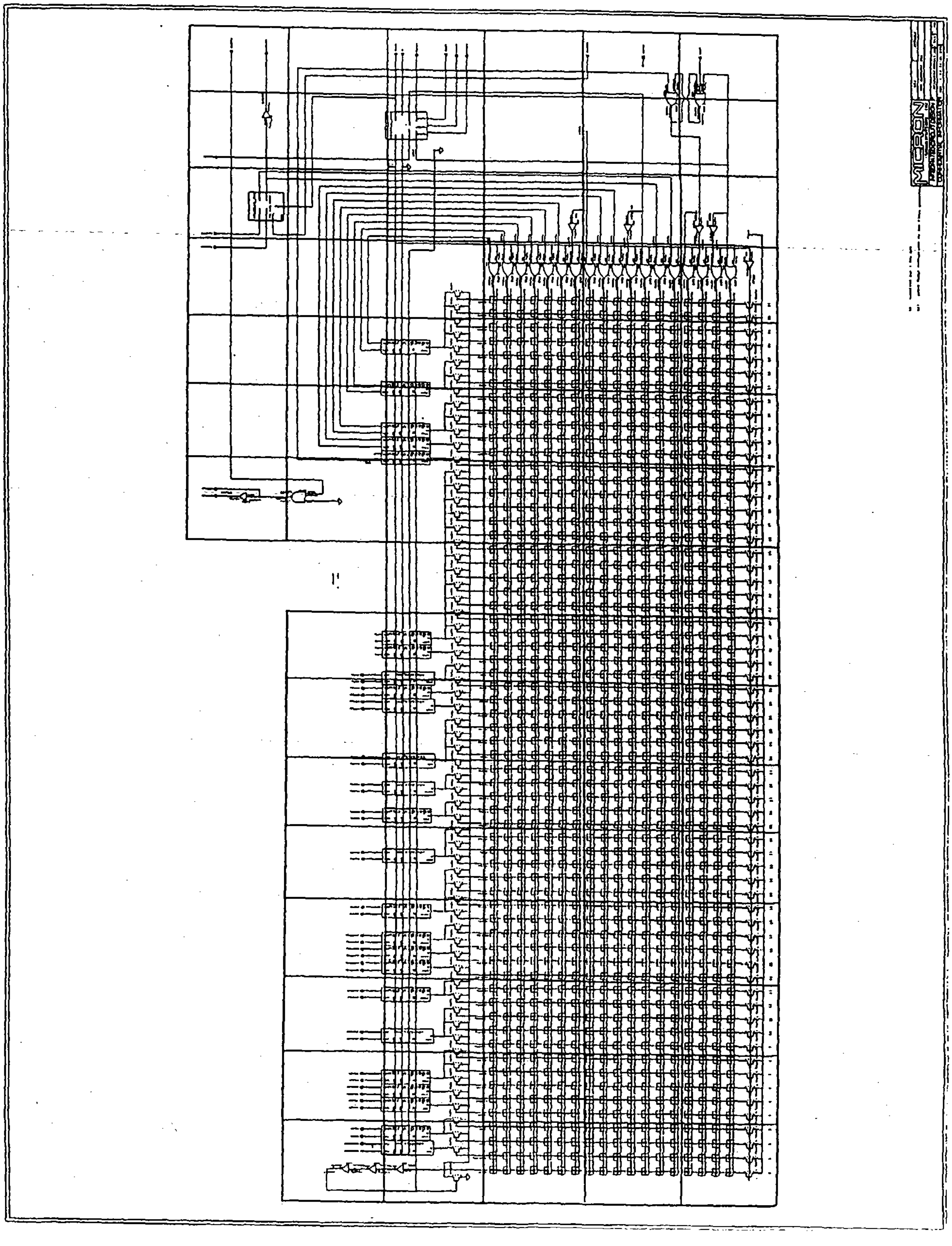
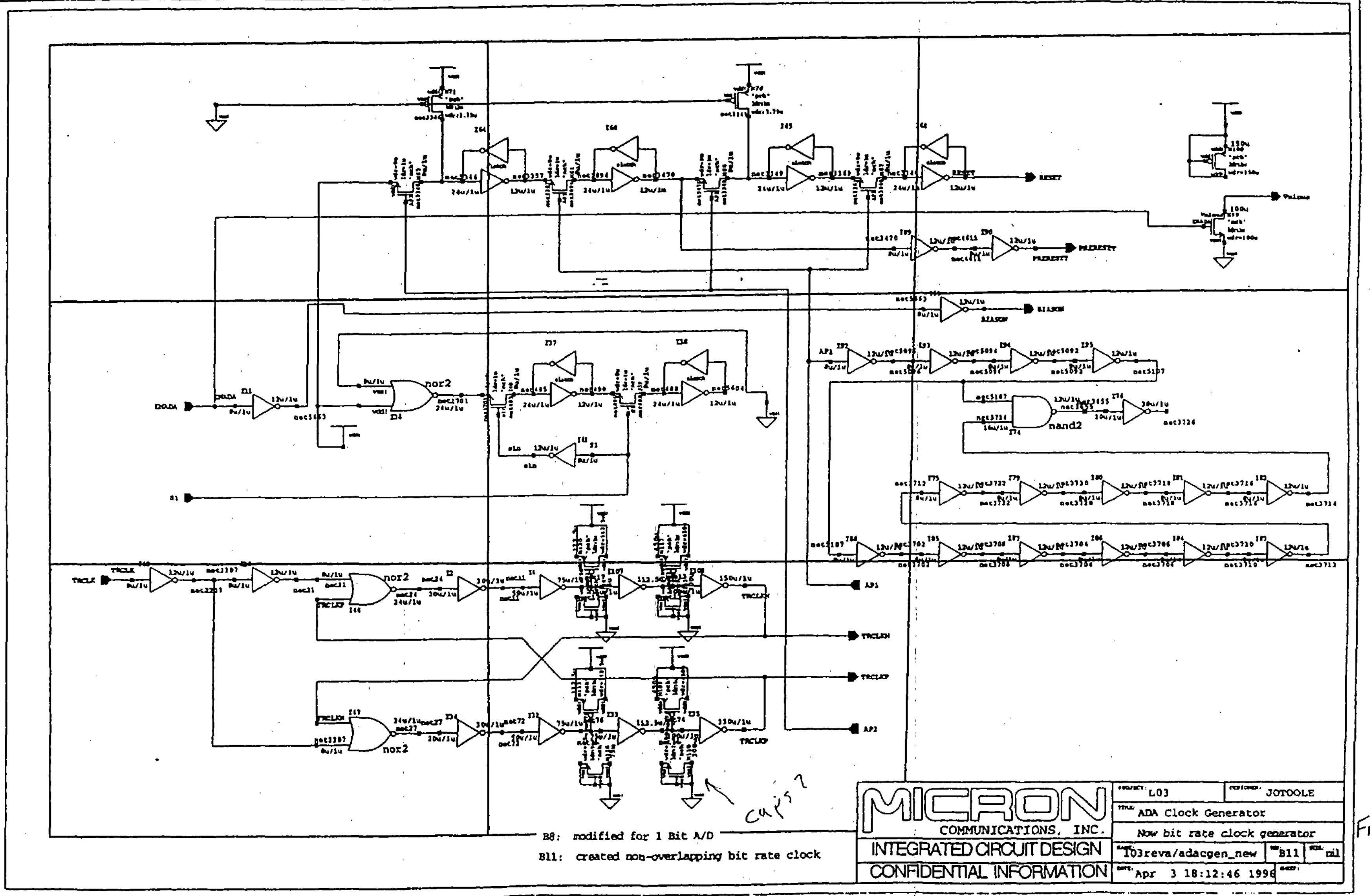


Fig. 9.0103

9.010301AA	9.010301AB	9.010301AC
9.010301BA	9.010301BB	9.010301BC
9.010301CA	9.010301CB	9.010301CC

FIG 9.010301



caps?

B8: modified for 1 Bit A/D
B11: created non-overlapping bit rate clock

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
ENGINEER: JOTOOLE
TITLE: ADA Clock Generator
Now bit rate clock generator
NAME: T03reva/adacgen_new
REV: B11
SIZE: mil
DATE: Apr 3 18:12:46 1996
SHEET:

FIG. 9.010301

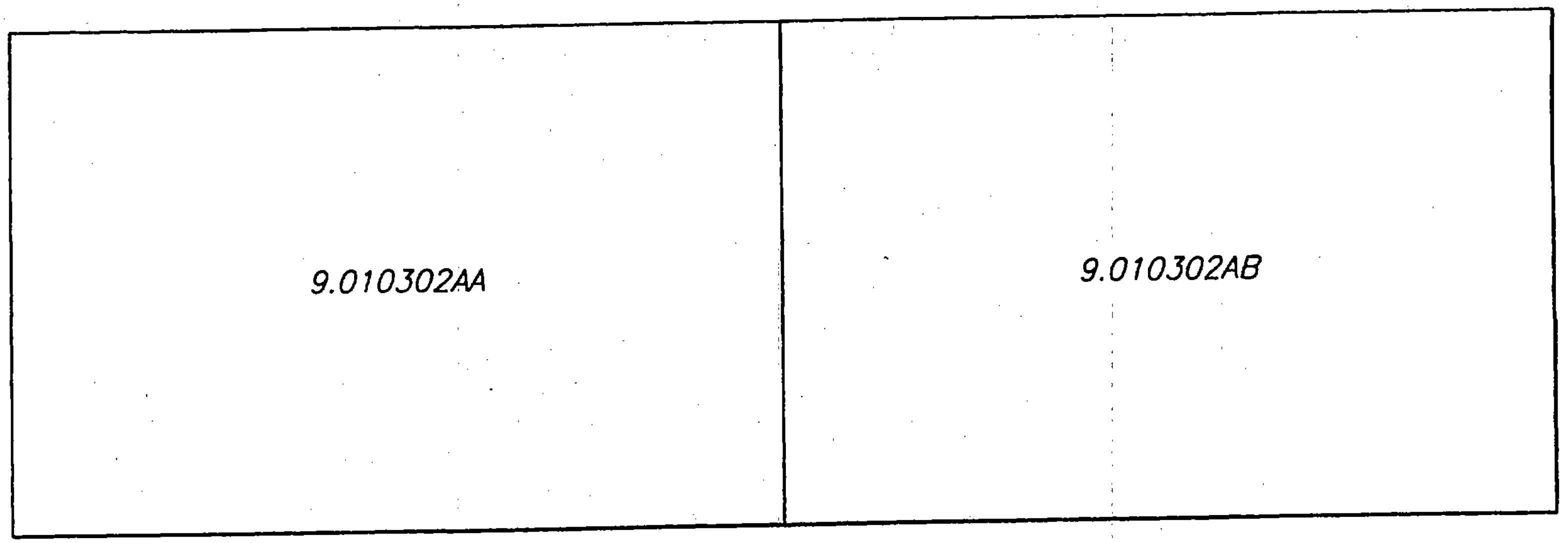
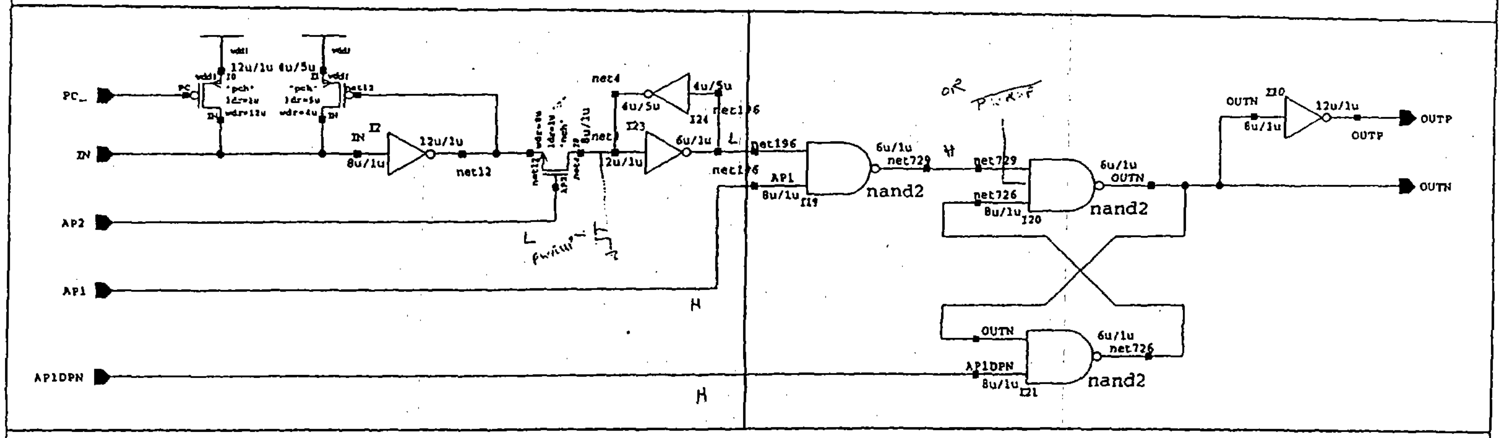


FIG 9.010302



MICRON COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: ADA CONTROL OUTPUT DRIVER	
NAME: l03reva/adacdrv_new	REV: B1 SIZE: A
DATE: May 18 18:02:41 1995	SHEET:

FIG. 9.010302

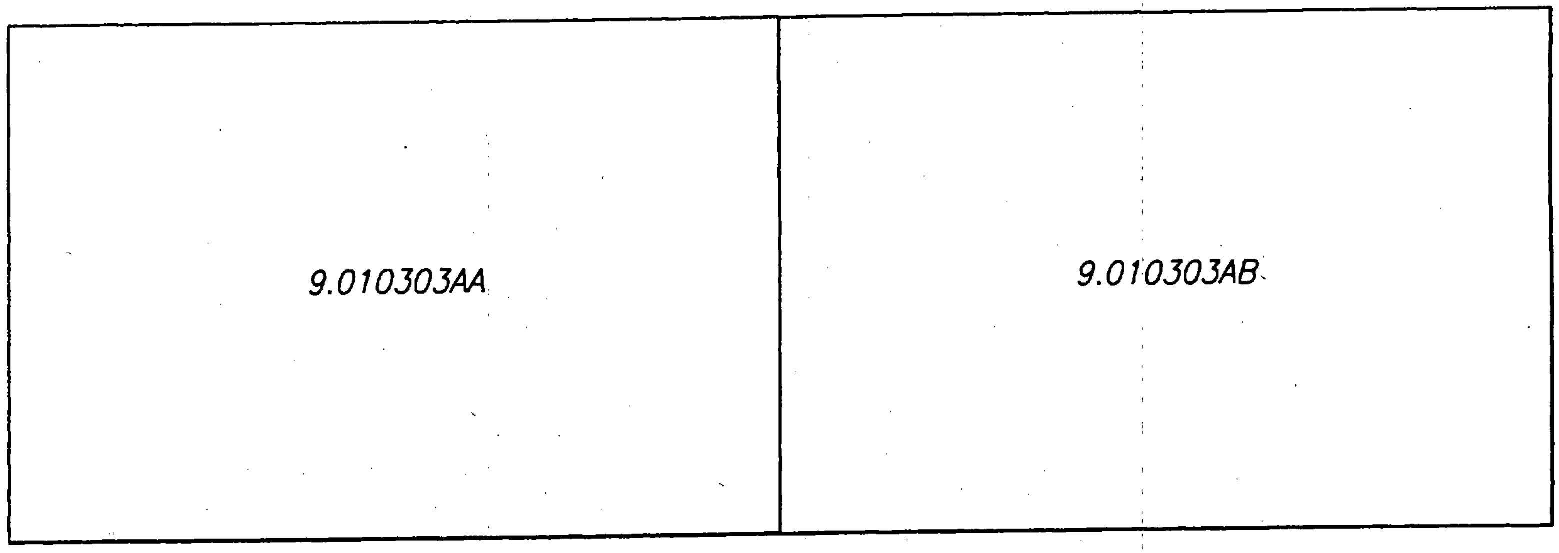
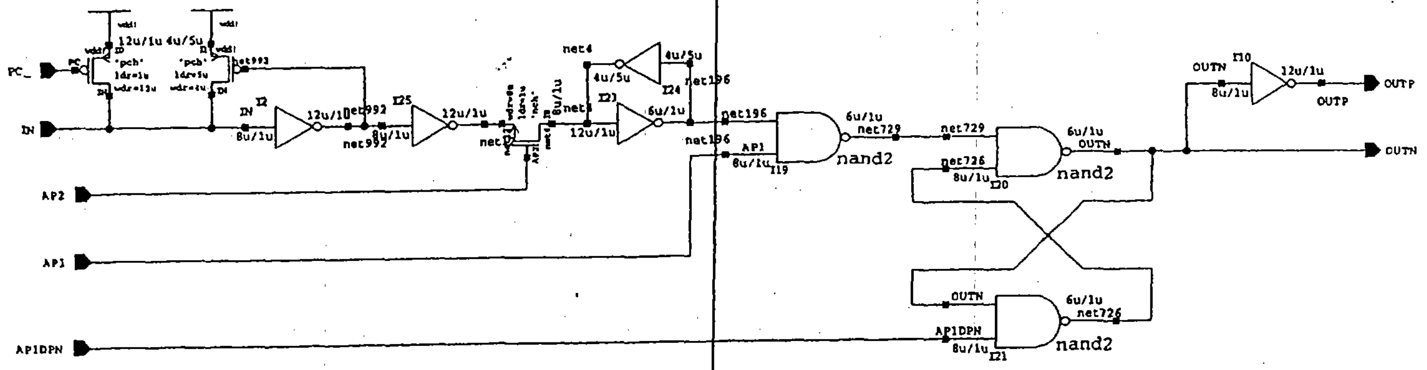


FIG. 9.010303



MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: ADA CONTROL OUTPUT DRIVER	
NAME: l03reva/adacdrvn_new	REV: B1 SIZE: A
DATE: May 19 15:33:27 1995	SHEET:

FIG. 9.010303

MI40-030

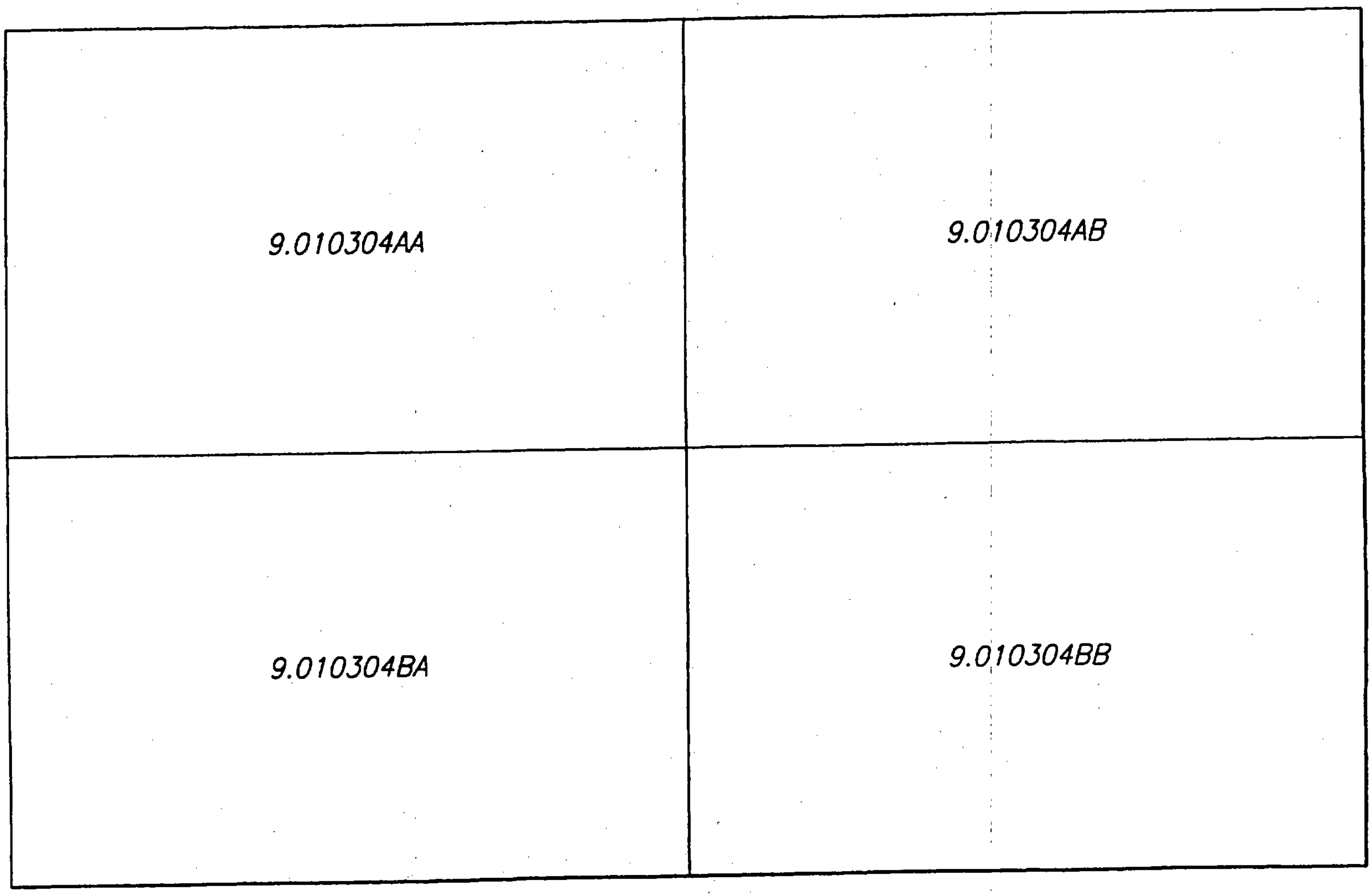
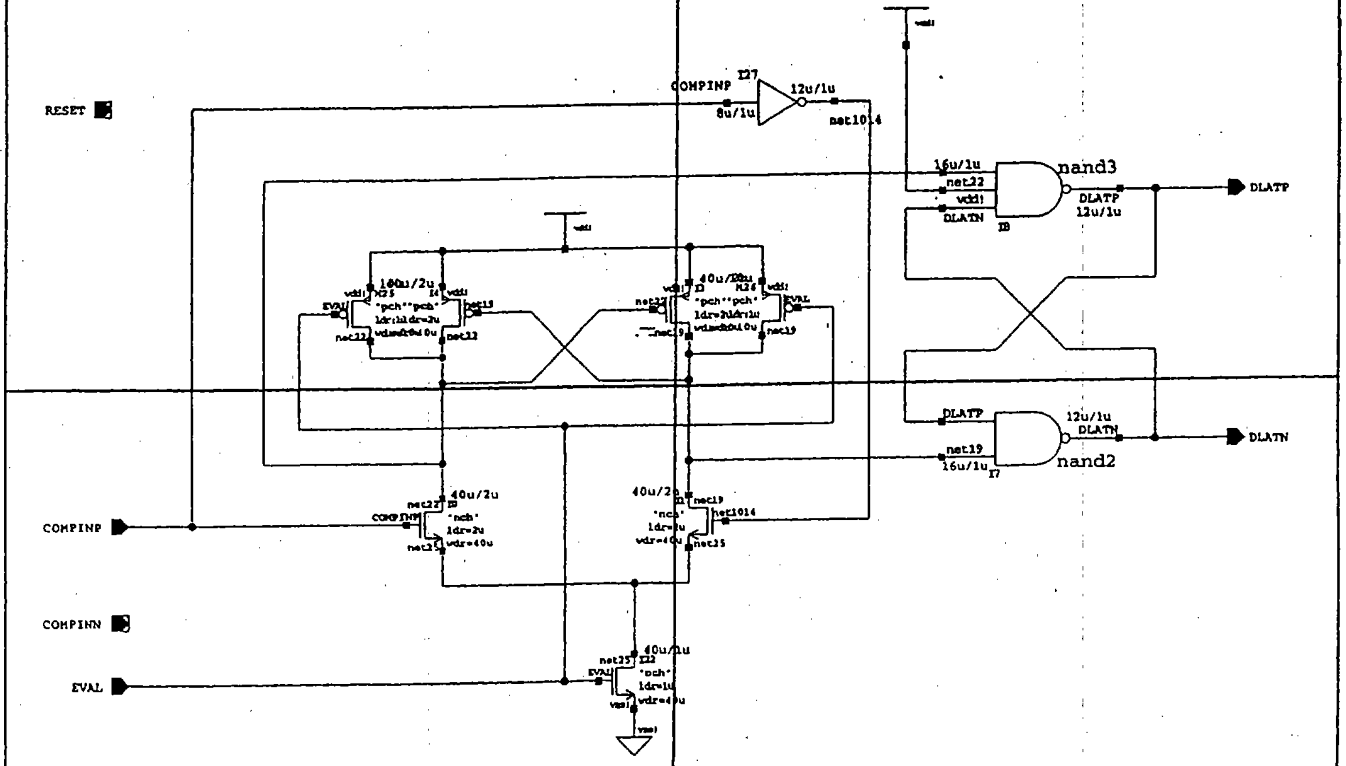


Fig 9.010304



B5: disconnect eval input; connect to vss

B8: reconnect eval and change reset polarity

B11: modified for use in battery voltage sensor

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: ADA Data Latch
NAME: 103reva/adadlat_new
REV: B11
SIZE: A
DATE: Apr 8 10:39:12 1996
SHEET:

FIG. 9.010304

9.0104AA	9.0104AB	9.0104AC	9.0104AD	9.0104AE
9.0104BA	9.0104BB	9.0104BC	9.0104BD	9.0104BE
9.0104CA	9.0104CB	9.0104CC	9.0104CD	
9.0104DA	9.0104DB	9.0104DC	9.0104DD	

FIG 9.0104

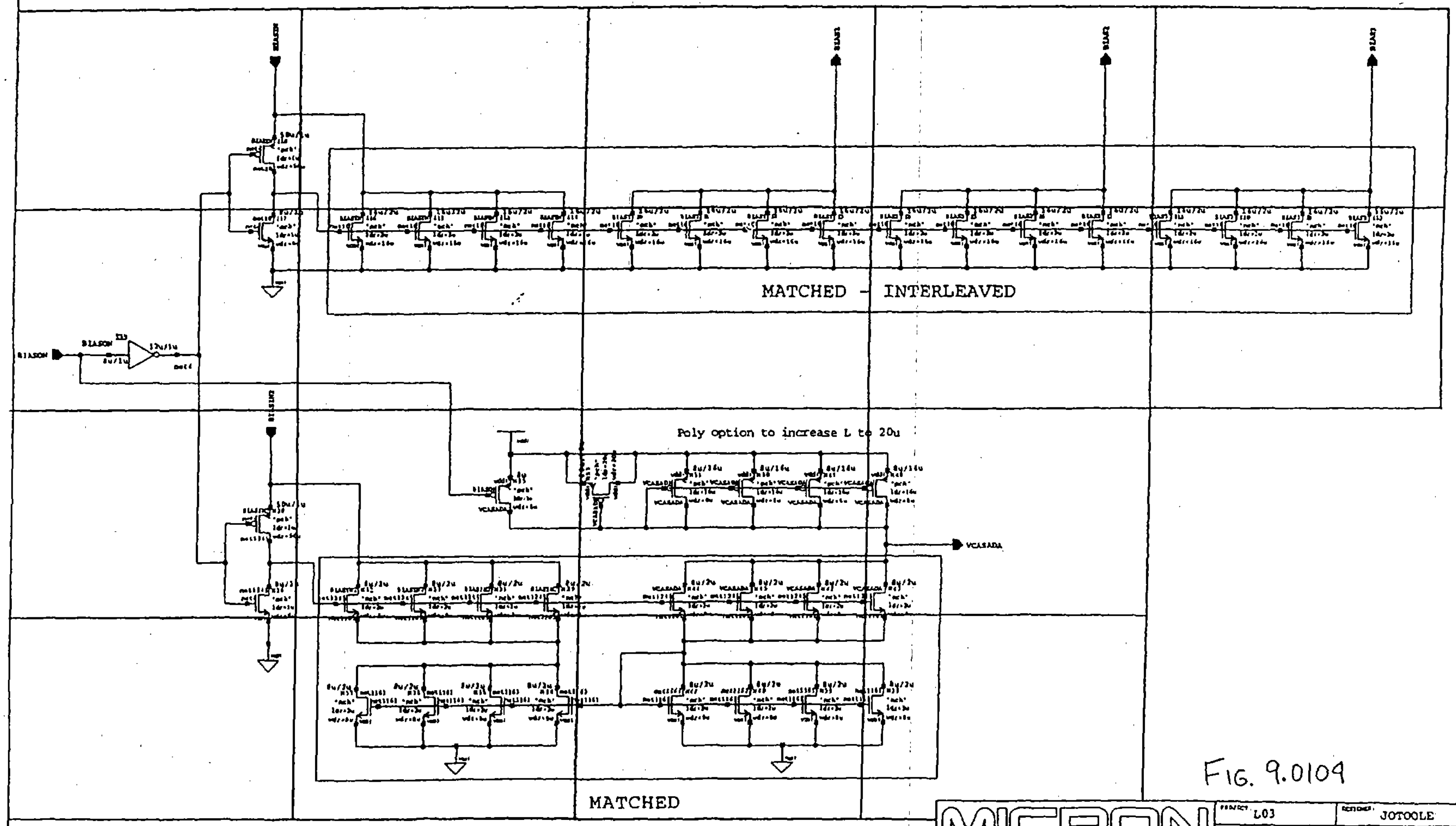


FIG. 9.0109

MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: ADA Analog Bias			
NAME: 103reva/adabias_new	REV: B1	FILE: rdl	
DATE: May 18 17:28:39 1995		SHEET:	

9.02AA	9.02AB	9.02AC	9.02AD	9.02AE	9.02AF	9.02AG	9.02AH	9.02AI	9.02AJ	9.02AK
9.02BA	9.02BB	9.02BC	9.02BD	9.02BE	9.02BF	9.02BG	9.02BH	9.02BI	9.02BJ	9.02BK
9.02CA		9.02CC	9.02CD	9.02CE	9.02CF	9.02CG	9.02CH	9.02CI	9.02CJ	9.02CK
9.02DA	9.02DB	9.02DC	9.02DD		9.02DF	9.02DG	9.02DH	9.02DI	9.02DJ	9.02DK

Fig 9.02

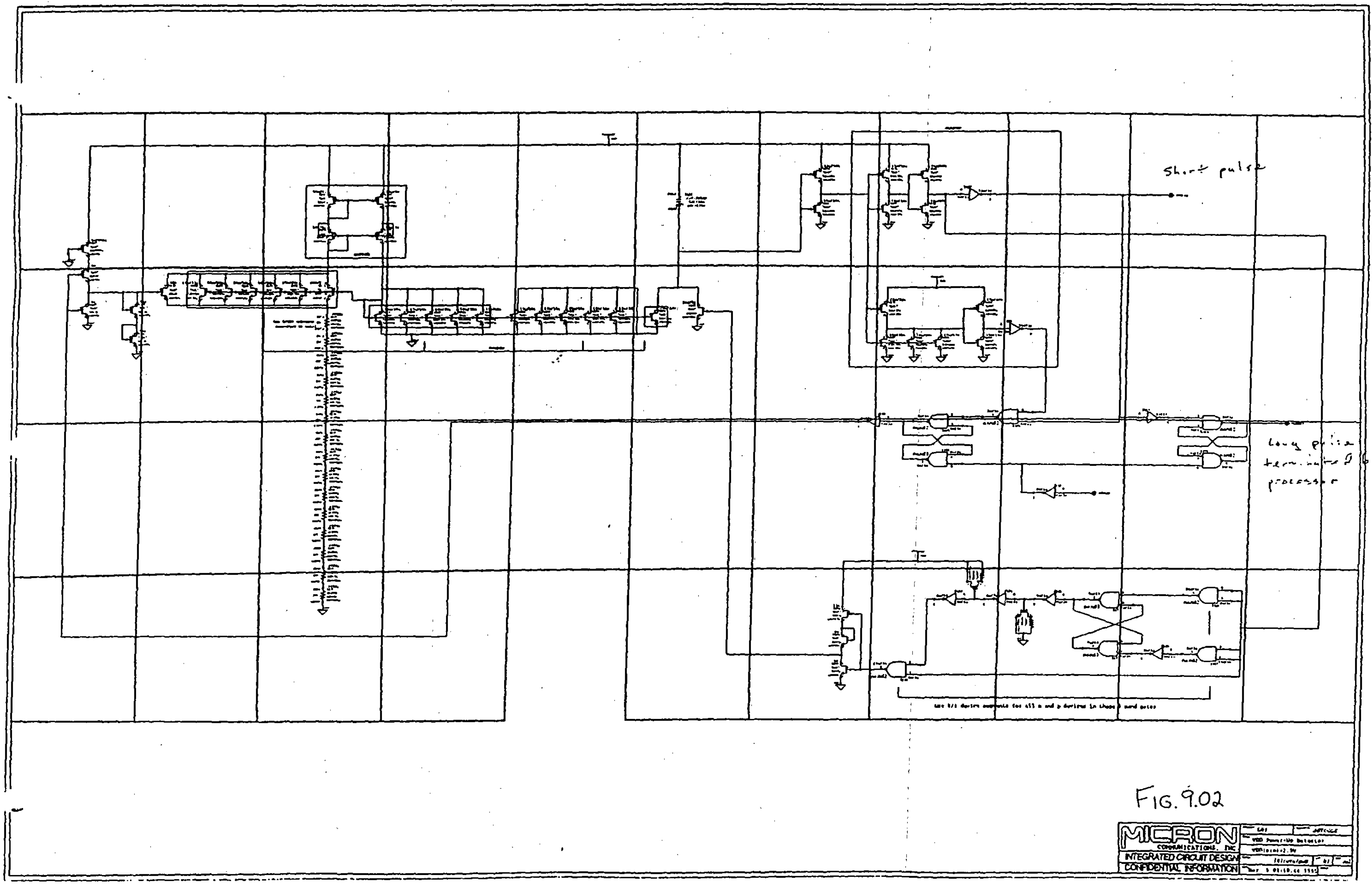

short pulse
Long pulse terminated by processor
use 1/1 device currents for all n and p devices in these 3 nand gates
MICRON COMMUNICATIONS, INC
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
VDD Power-Up Detector

FIG. 9.02

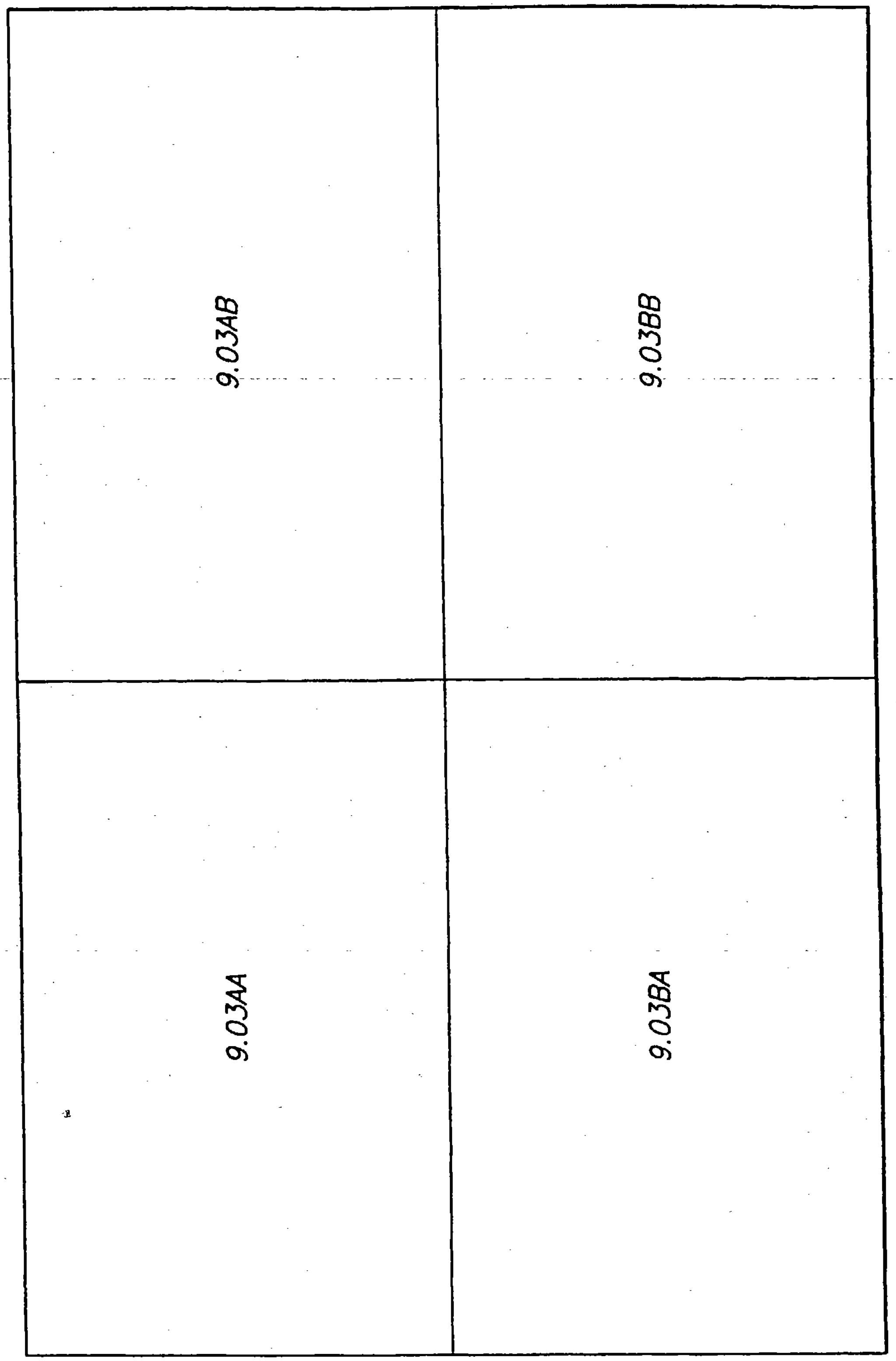


FIG. 9.03

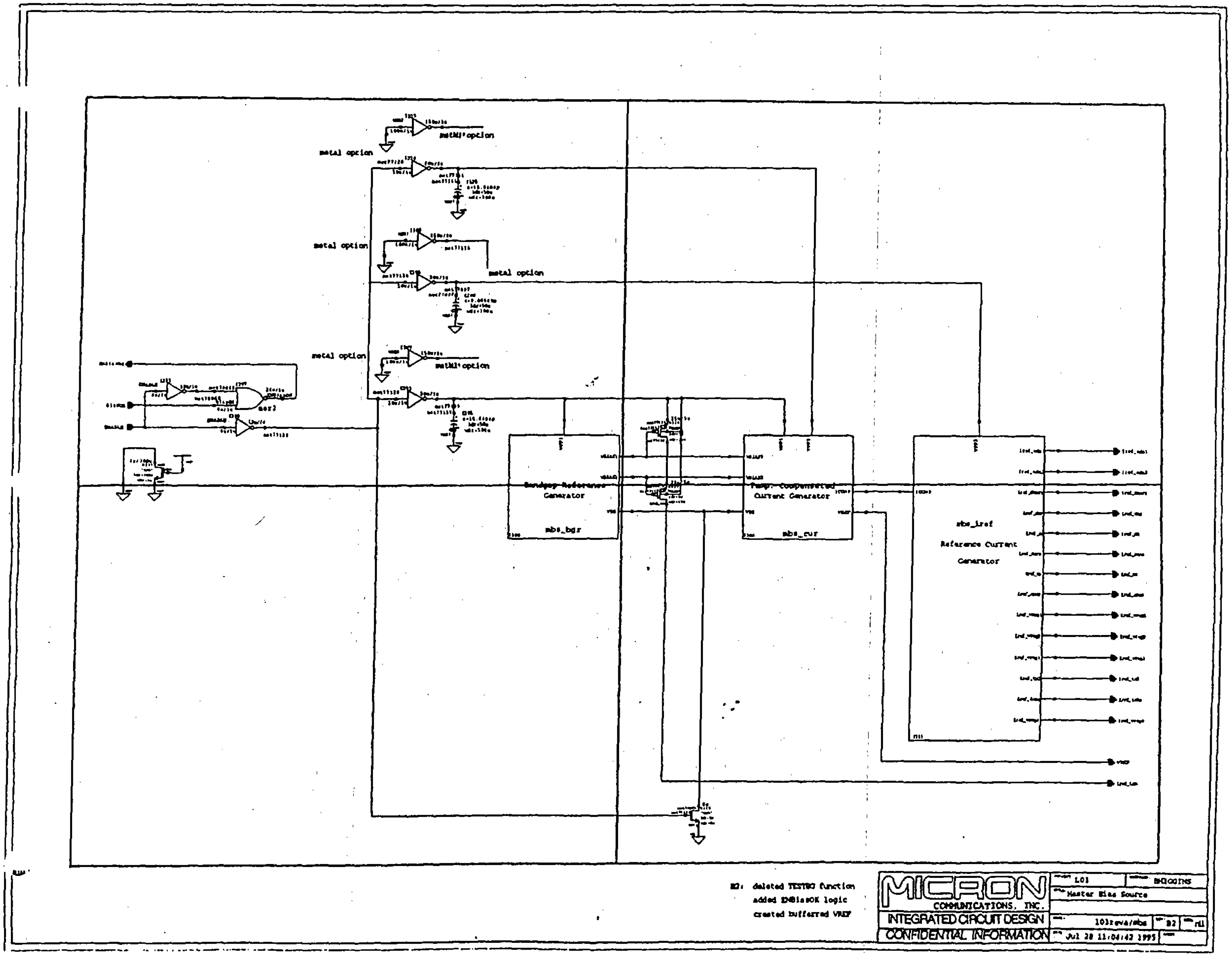

metal option
metal option
metal option
metal option
Bandgap Reference Generator
mbs_bgr
Temp. Compensated Current Generator
mbs_cur
mbs_iref
Reference Current Generator
VREF
B2: deleted TESTBG function
added ENBiasOK logic
created buffered VREF
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L01
BHIGGINS
Master Bias Source
103reva/mbs
B2
Jul 28 11:04:42 1995

FIG. 9.03

9.0301AA	9.0301AB	9.0301AC	9.0301AD	9.0301AE	9.0301AF	9.0301AG	9.0301AH	9.0301AI	9.0301AJ
9.0301BA	9.0301BB	9.0301BC	9.0301BD	9.0301BE	9.0301BF	9.0301BG	9.0301BH	9.0301BI	9.0301BJ
	9.0301CB	9.0301CC	9.0301CD	9.0301CE	9.0301CF	9.0301CG	9.0301CH	9.0301CI	9.0301CJ
	9.0301DB	9.0301DC	9.0301DD	9.0301DE	9.0301DF	9.0301DG	9.0301DH	9.0301DI	9.0301DJ

FIG 9.0301

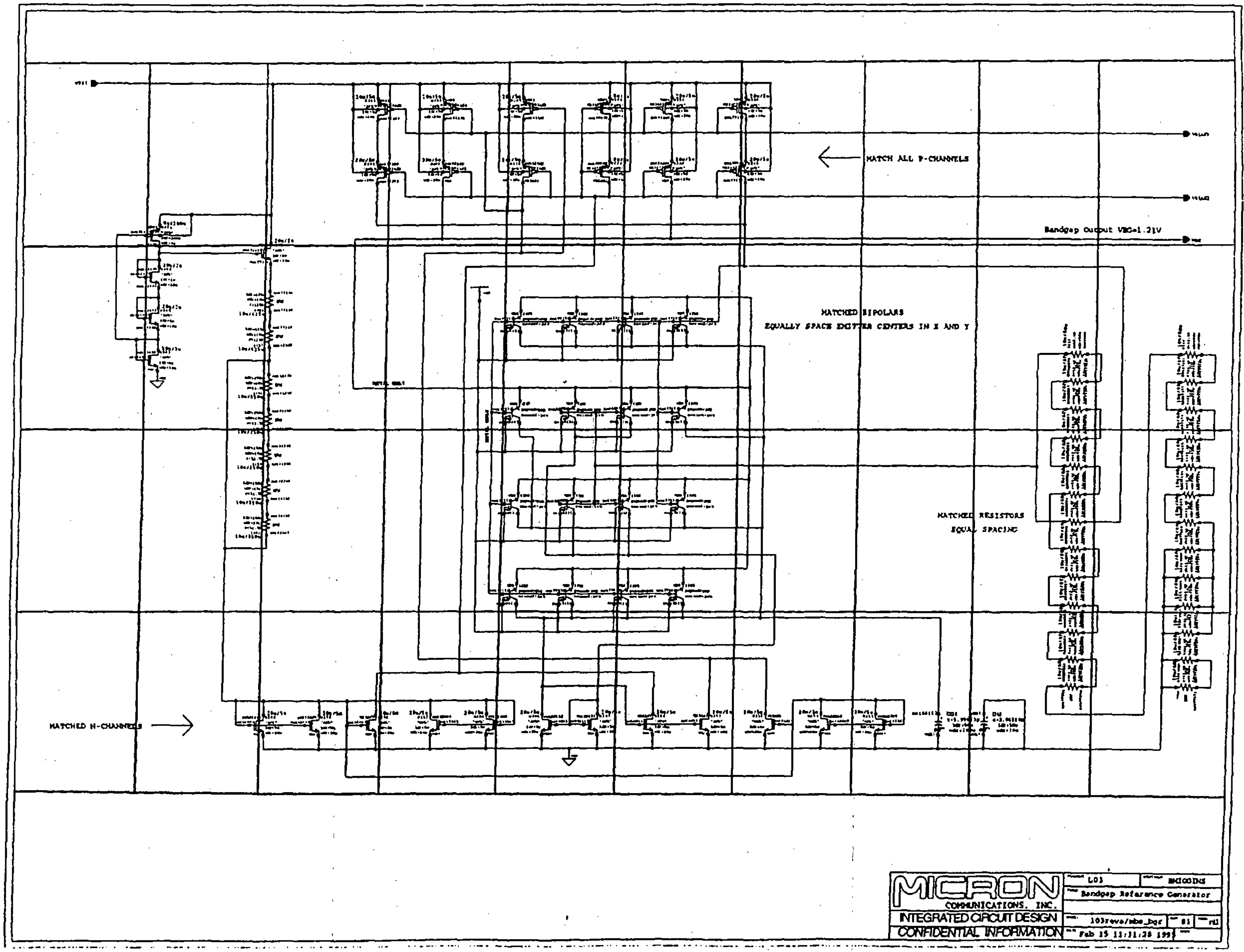

MATCH ALL P-CHANNELS
Bandgap Output VBG=1.21V
MATCHED BIPOLARS
EQUALLY SPACE EMITTER CENTERS IN X AND Y
MATCHED RESISTORS
EQUAL SPACING
MATCHED N-CHANNELS
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
BHIGGINS
Bandgap Reference Generator
103reva/mbe_bgr
01
Feb 15 11:11:28 1995

FIG. 9.0301

9.0302AJ	9.0302BJ	9.0302CJ	
9.0302AI	9.0302BI	9.0302CI	9.0302DI
9.0302AH	9.0302BH	9.0302CH	9.0302DH
9.0302AG	9.0302BG	9.0302CG	9.0302DG
9.0302AF	9.0302BF	9.0302CF	
9.0302AE	9.0302BE	9.0302CE	
9.0302AD	9.0302BD	9.0302CD	
9.0302AC	9.0302BC	9.0302CC	
9.0302AB	9.0302BB		
9.0302AA	9.0302BA		

Fig. 9.0302

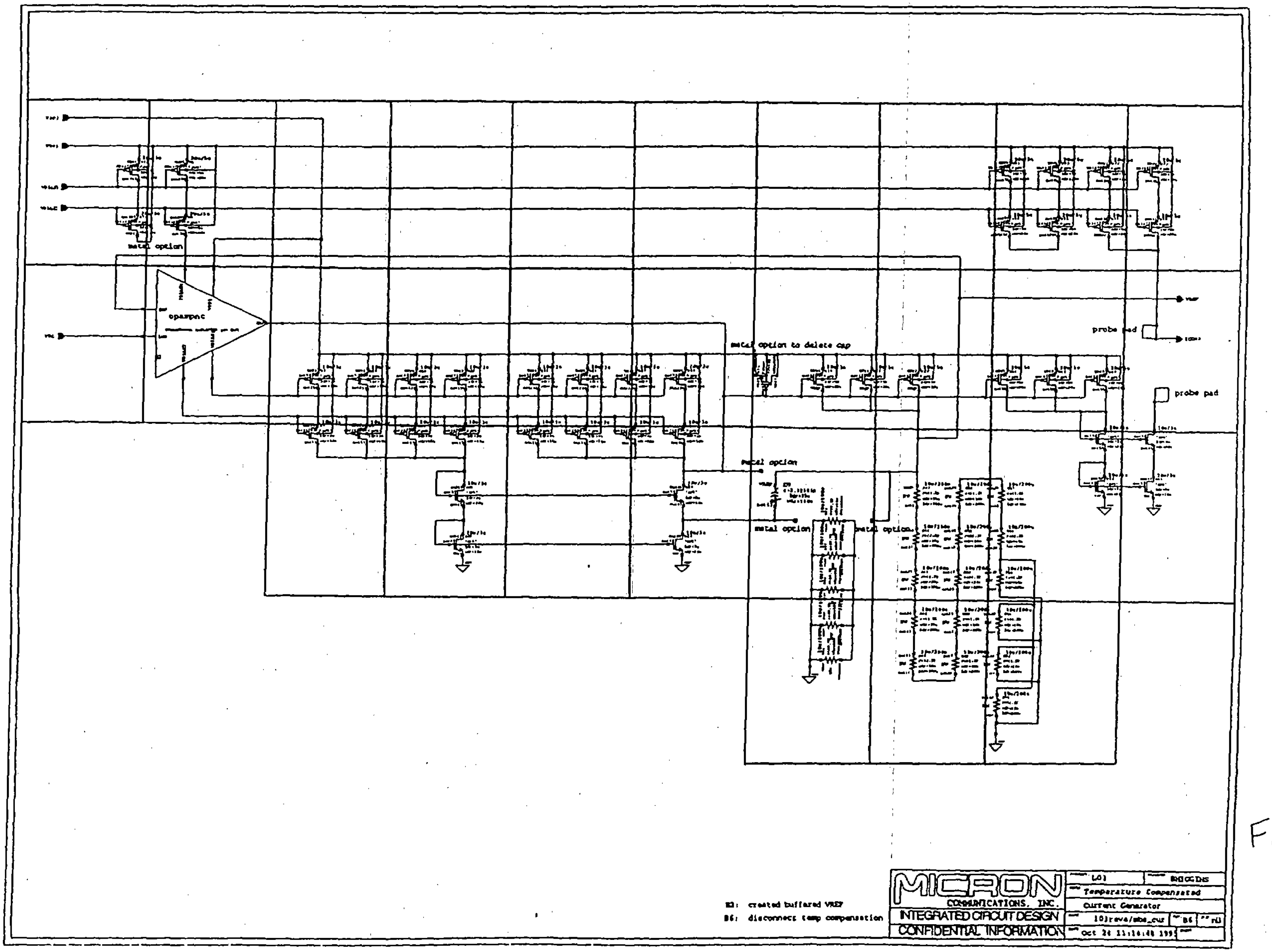

metal option
opampnc
metal option to delete cap
probe pad
probe pad
metal option
metal option
metal option
B3: created buffered VREF
B6: disconnect temp compensation
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L01
Temperature Compensated
Current Generator
10]reva/mbe_cur
B6
Oct 24 11:16:48 1995

FIG. 9.0302

9.0303AA	9.0303AB	9.0303AC	9.0303AD	9.0303AE	9.0303AF
9.0303BA	9.0303BB	9.0303BC	9.0303BD	9.0303BE	9.0303BF
	9.0303CB	9.0303CC	9.0303CD	9.0303CE	9.0303CF

FIG 9.0303

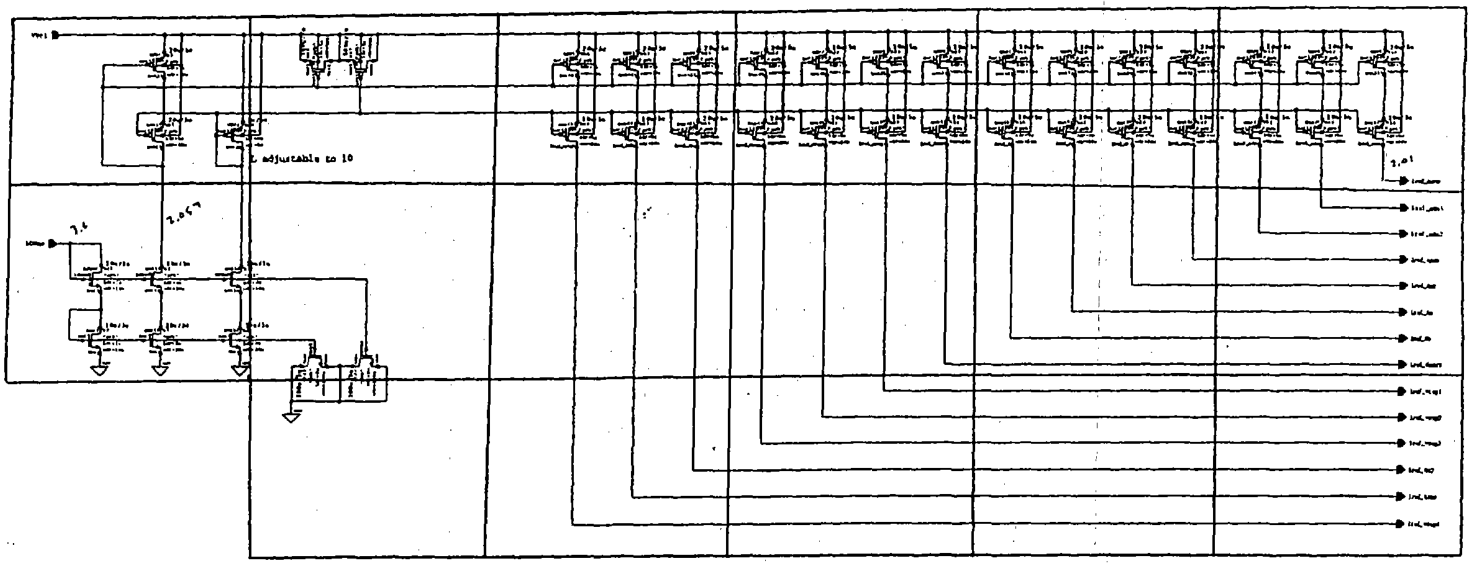


FIG. 9.0303

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03 | BUCODS
Reference Current
Generator
101revo/abs_iref | B1 | rd)
Apr 21 11:15:21 1995

9.04AA	9.04AB	9.04AC	9.04AD	9.04AE
9.04BA	9.04BB	9.04BC	9.04BD	9.04BE
9.04CA	9.04CB	9.04CC	9.04CD	9.04CE

FIG. 9.04

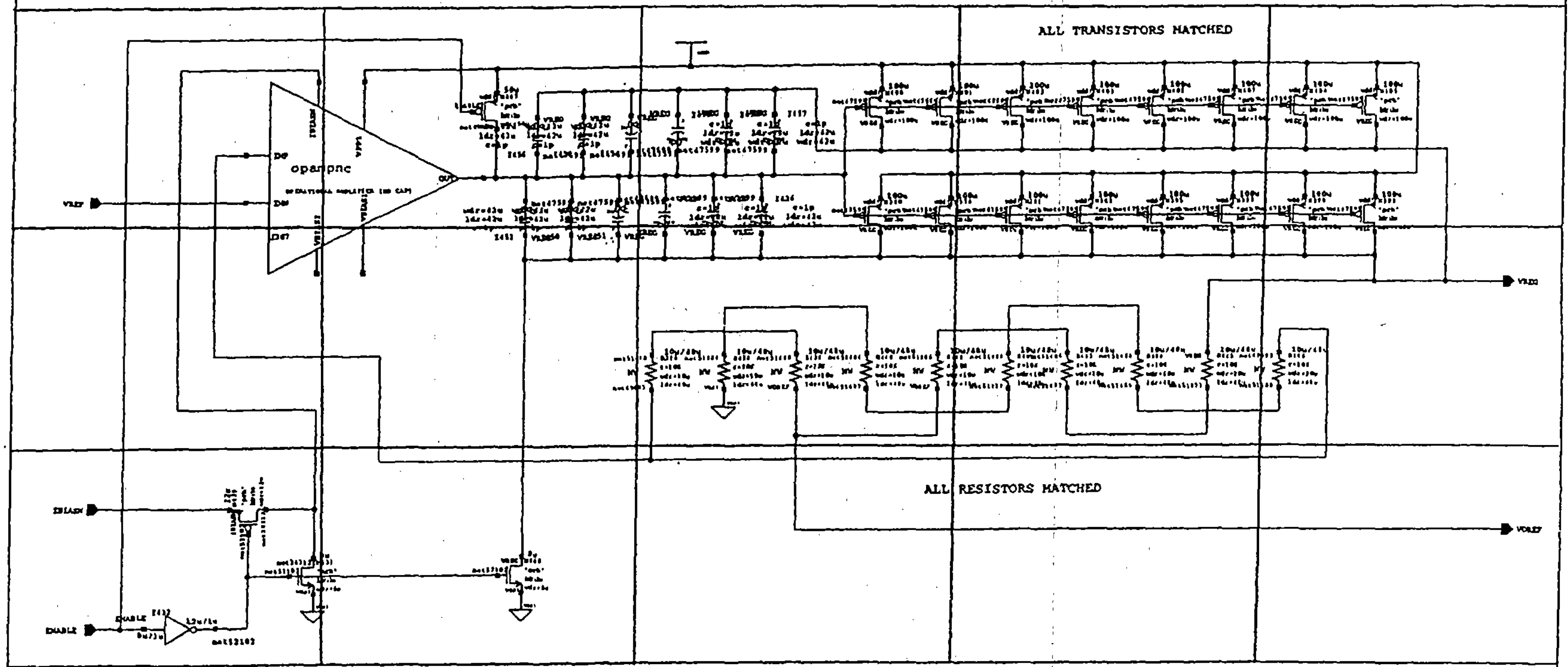
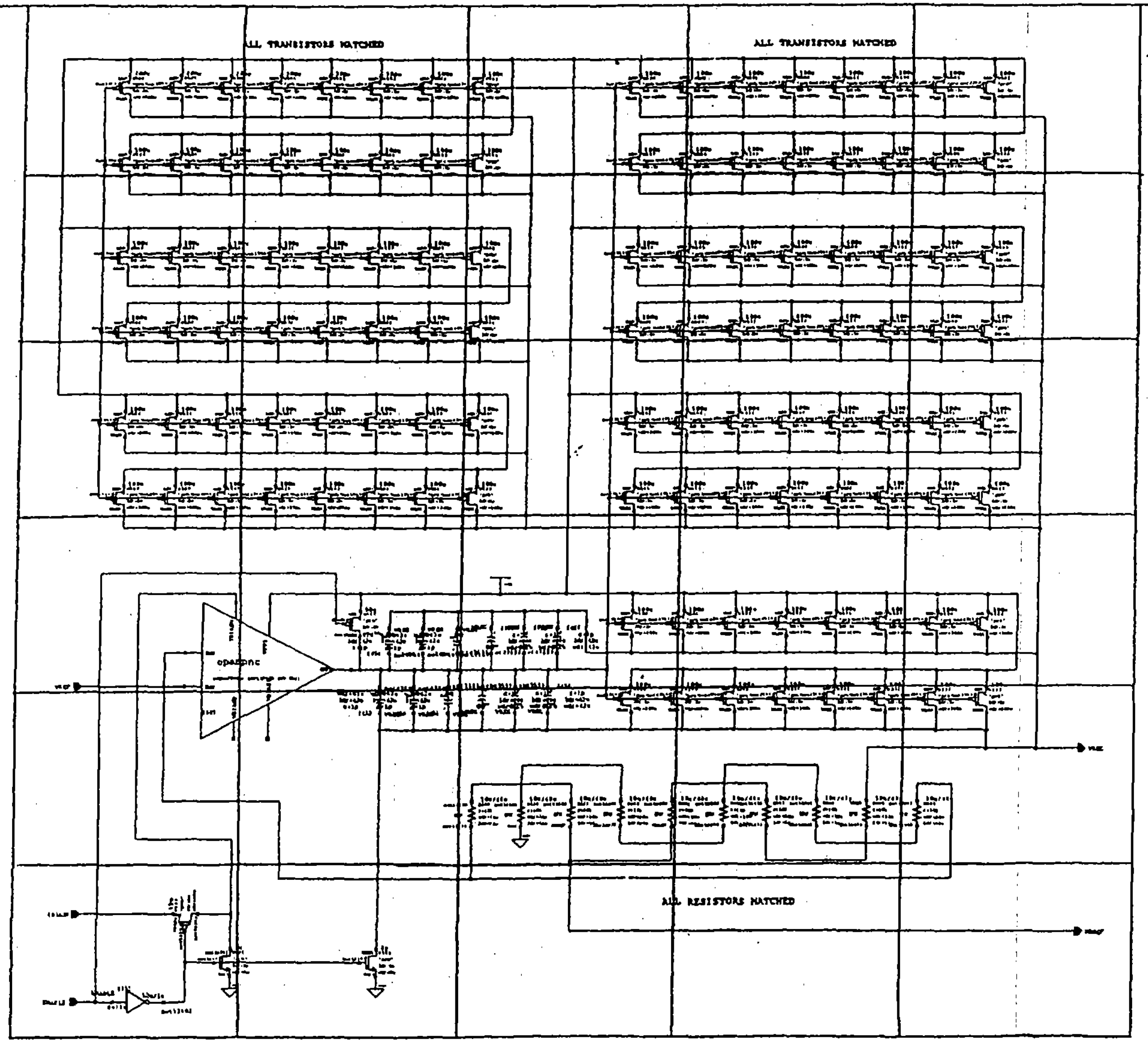


FIG. 9.04

MICRON COMMUNICATIONS, INC.	PROJECT: L03 — DESIGNER: BHIGGINS
INTEGRATED CIRCUIT DESIGN	TITLE: Voltage Regulator Vo=2.4/Vin(min)=2.5
CONFIDENTIAL INFORMATION	NAME: 103reva/vrg — REV: B1 — SCL: nil DATE: Apr 29 13:22:24 1995 — CKLT:

9.05AA	9.05AB	9.05AC	9.05AD	9.05AE
9.05BA	9.05BB	9.05BC	9.05BD	9.05BE
9.05CA	9.05CB	9.05CC	9.05CD	9.05CE
9.05DA	9.05DB	9.05DC	9.05DD	9.05DE
9.05EA	9.05EB	9.05EC	9.05ED	9.05EE
9.05FA	9.05FB	9.05FC	9.05FD	9.05FE

Fig 9.05



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
BHIGGINS
Voltage Regulator
Vo=2.4/Vin(min)=2.5
10)reva/vrgcx
B1
nil
Apr 29 11:23:47 1995

FIG. 9.05

9.0501AA	9.0501AB	9.0501AC	9.0501AD
9.0501BA	9.0501BB	9.0501BC	9.0501BD
9.0501CA	9.0501CB	9.0501CC	9.0501CD

Fig 9.0501

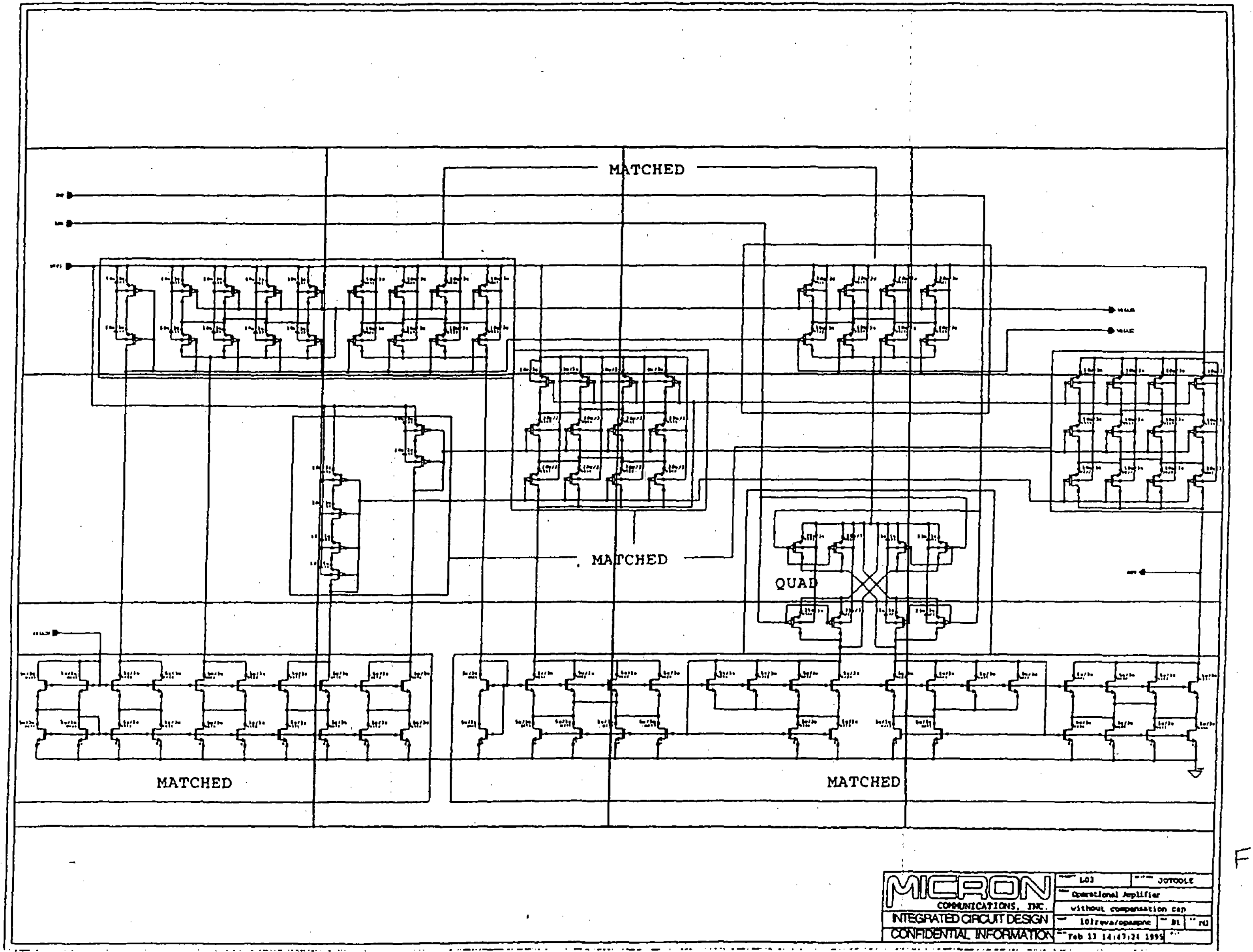
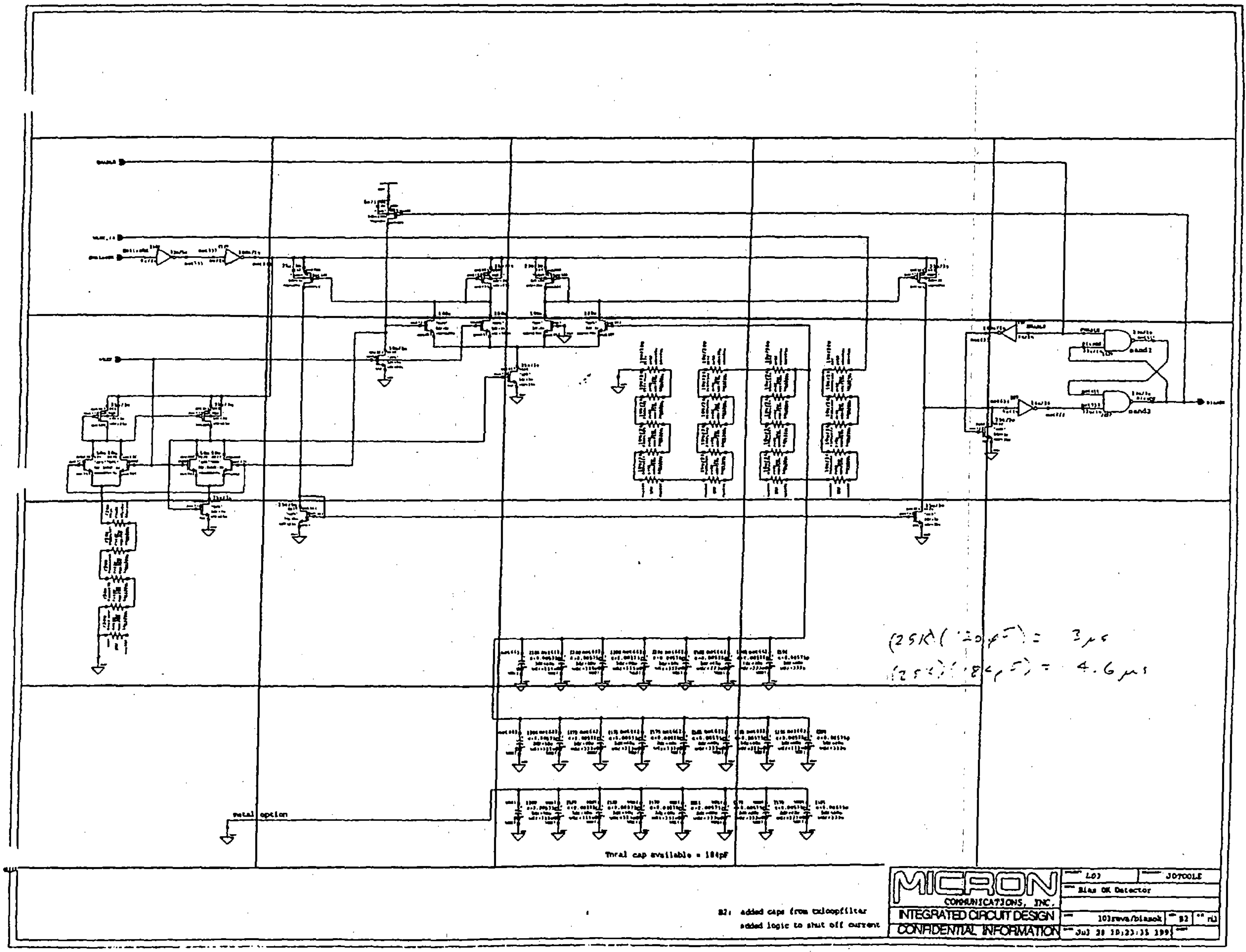

MATCHED
MATCHED
QUAD
MATCHED
MATCHED
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
JOTOOLE
Operational Amplifier
without compensation cap
101reva/opampnc
B1
Feb 13 14:47:24 1995

FIG. 9.0501

9.06AA	9.06AB	9.06AC	9.06AD	9.06AE
9.06BA	9.06BB	9.06BC	9.06BD	9.06BE
9.06CA	9.06CB	9.06CC	9.06CD	
9.06DA	9.06DB	9.06DC	9.06DD	

Fig 9.06



(25K)(120pF) = 3μs
(25K)(184pF) = 4.6μs

B2: added caps from txloopfilter
added logic to shut off current

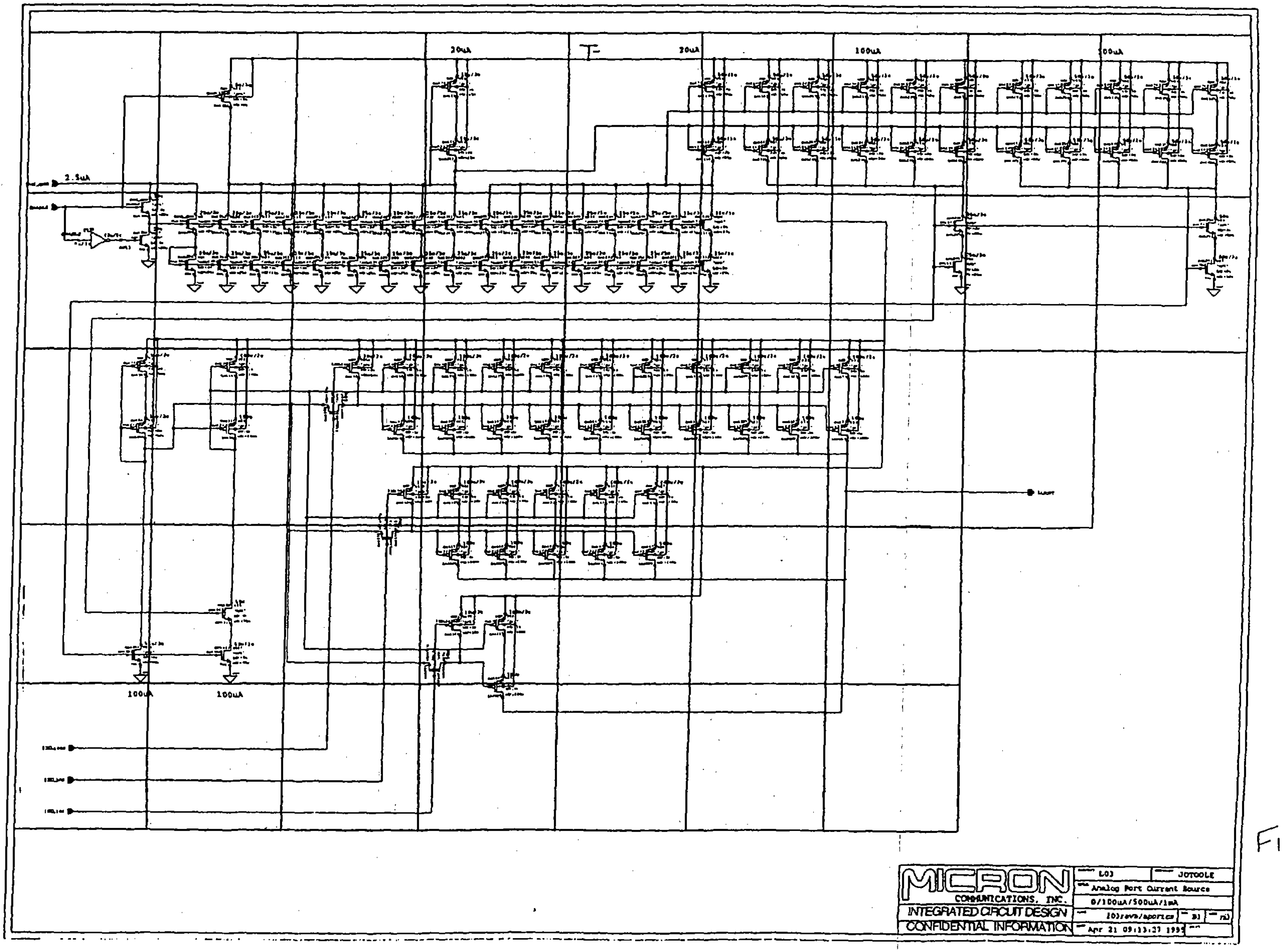
MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03 | JOTOOLE
Bias OK Detector
103reva/biasok | B2 | n1
Jul 28 10:23:35 199

FIG. 9.06

9.07AA	9.07AB	9.07AC	9.07AD	9.07AE	9.07AF	9.07AG	9.07AH	9.07AI
9.07BA	9.07BB	9.07BC	9.07BD	9.07BE	9.07BF	9.07BG	9.07BH	9.07BI
9.07CA	9.07CB	9.07CC	9.07CD	9.07CE	9.07CF	9.07CG	9.07CH	
9.07DA	9.07DB	9.07DC	9.07DD	9.07DE	9.07DF	9.07DG		
9.07EA	9.07EB	9.07EC	9.07ED	9.07EE	9.07EF	9.07EG		

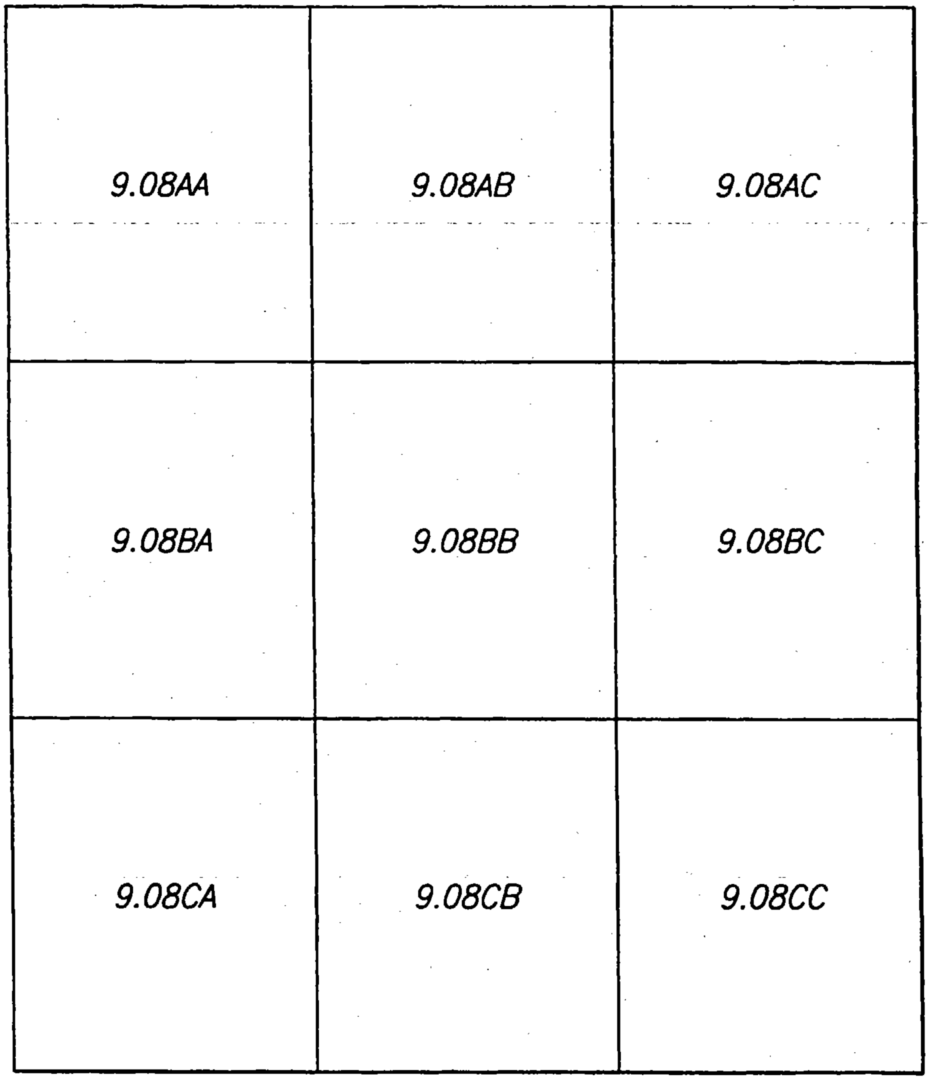
FIG 9.07



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

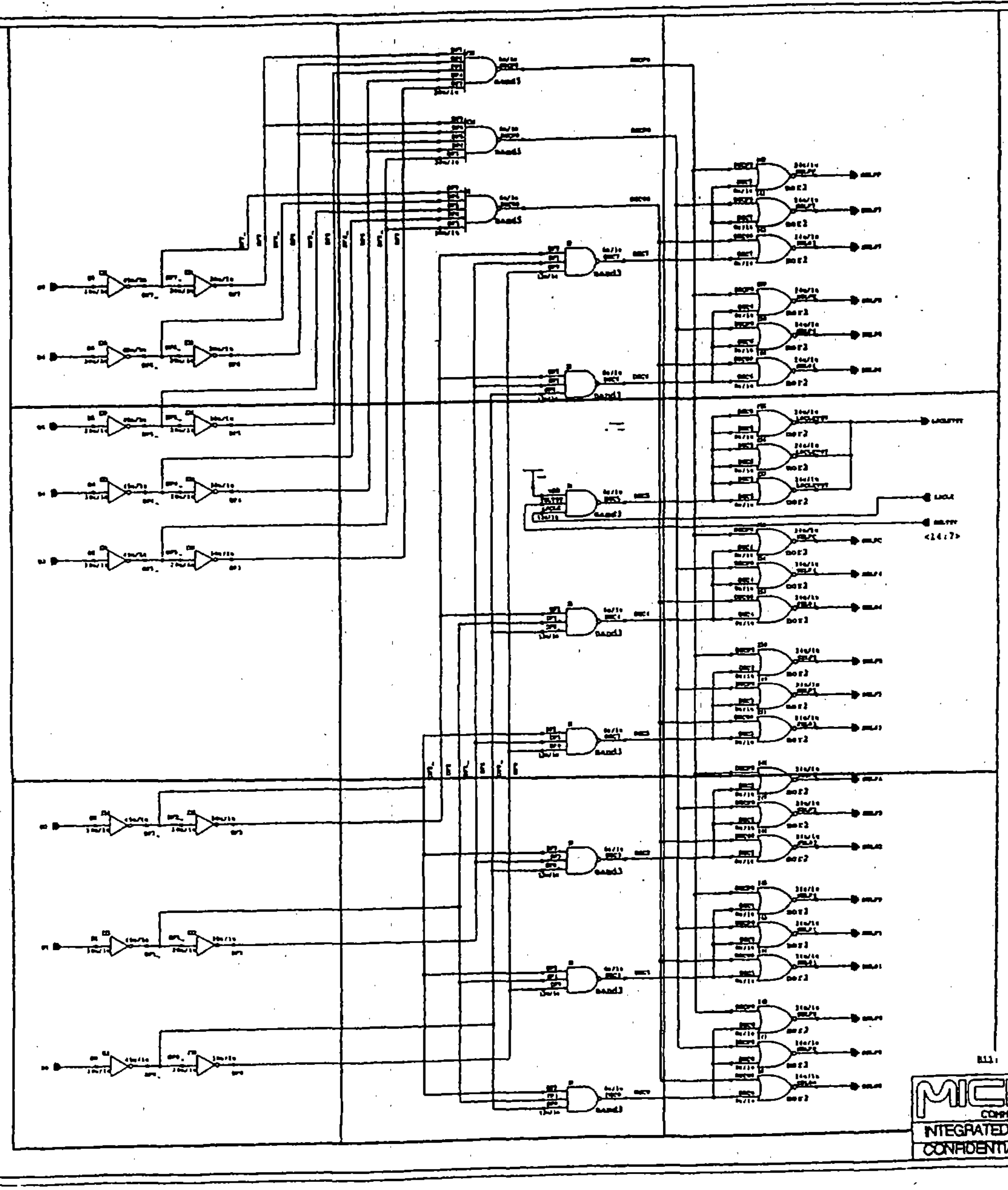
L03
JOTOOLE
Analog Port Current Source
0/100uA/500uA/1mA
I0)revb/aportcs
B1
n)
Apr 21 09:13:27 1995

FIG. 9.07



9.08AA	9.08AB	9.08AC
9.08BA	9.08BB	9.08BC
9.08CA	9.08CB	9.08CC

Fig 9.08



B11: added LPCLK test logic

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

(A3) JOTOOLE
Analog Multiplexer Decoder
and LPCLK test logic
103revs/ *** B11 r1l
Apr 12 14:56:23 1996

FIG. 9.08

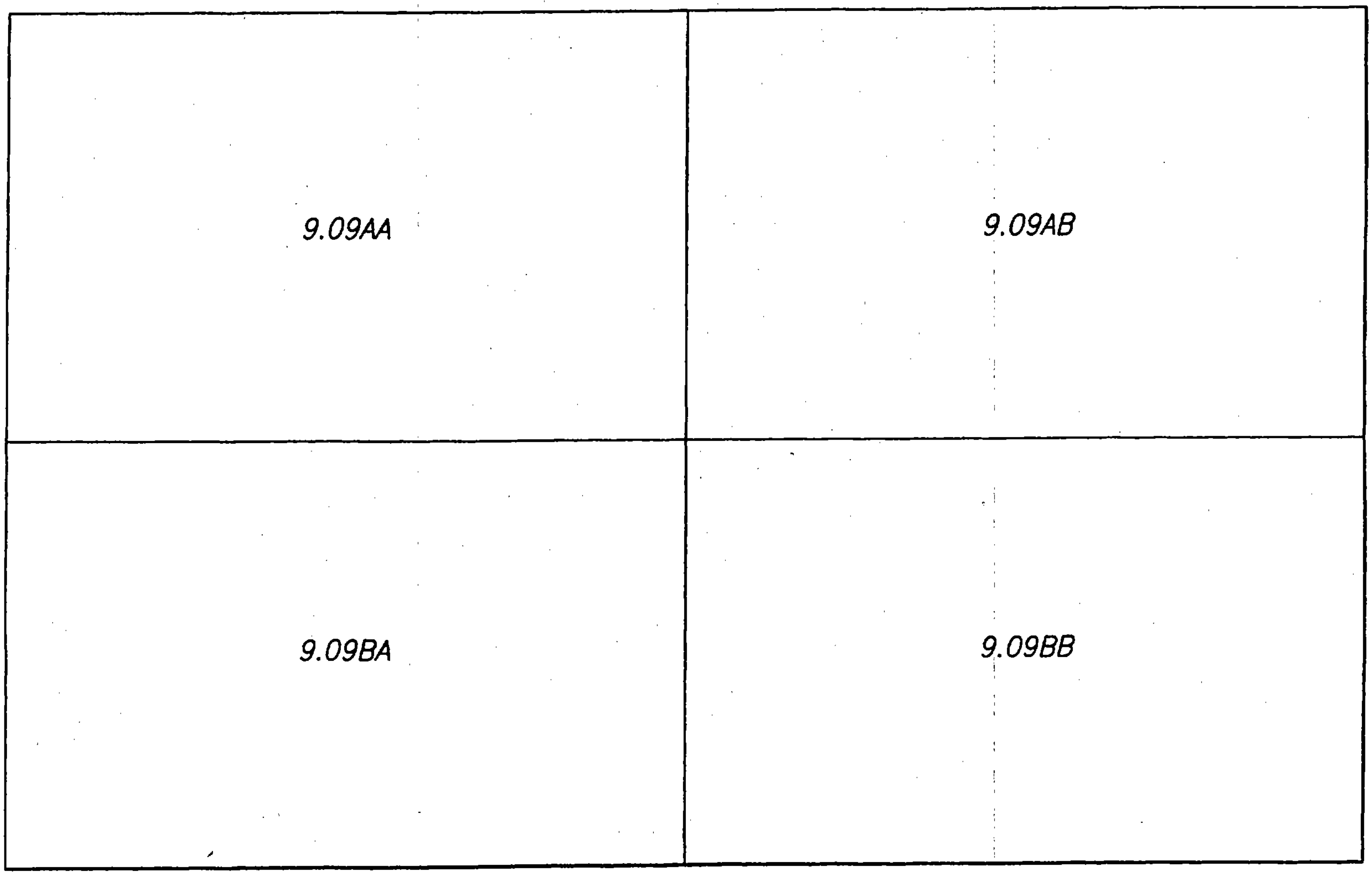


Fig 9.09

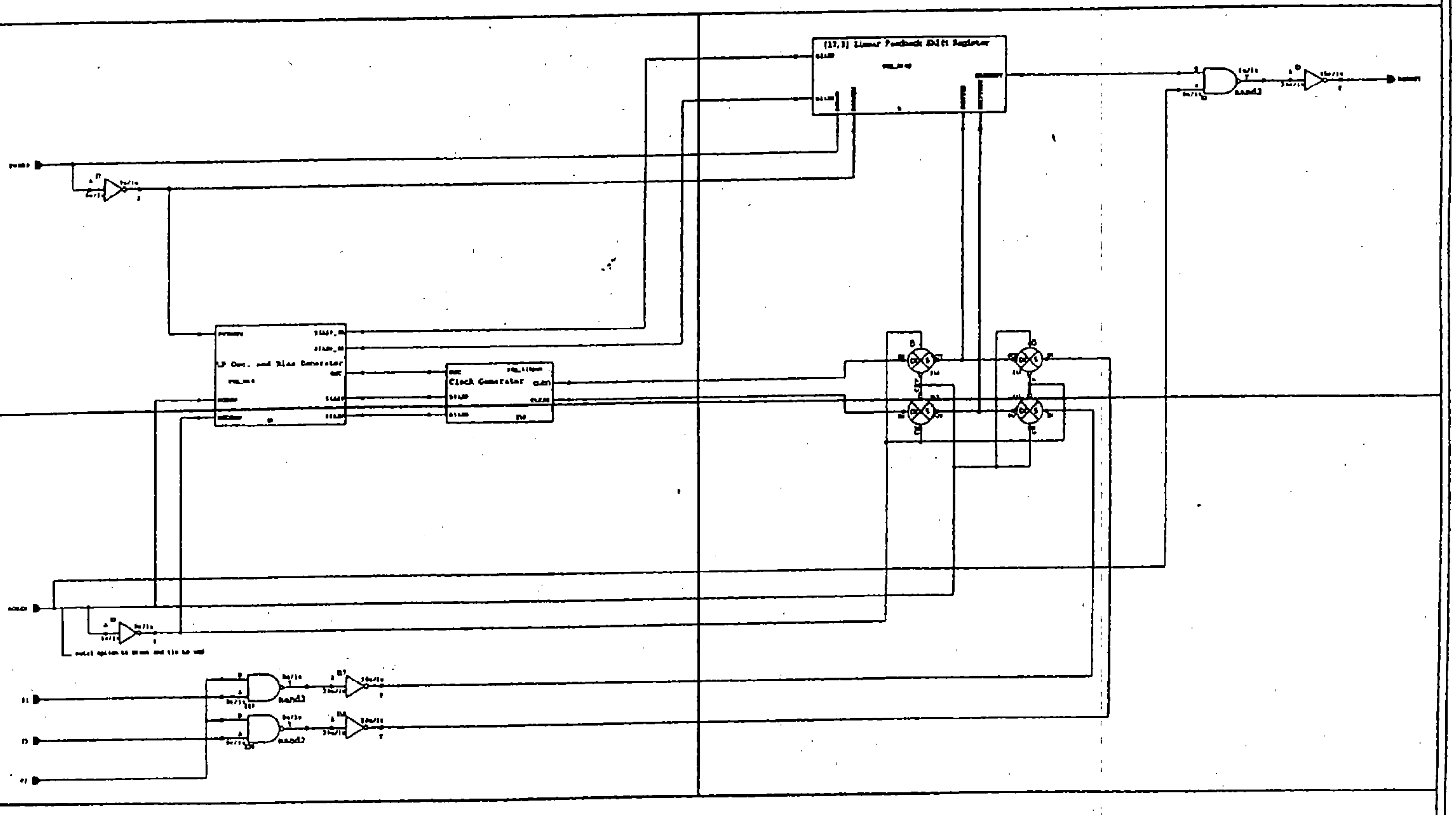

(17,3) Linear Feedback Shift Register
LF Osc. and Bias Generator
Clock Generator
nand2
nand2
nand2

FIG. 9.09

B8: added P2 input

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
JOTOOLE
Random Clock Generator
103reva/rcg
B8
Jan 24 09:37:38 1996

9.0901AA	9.0901AB	9.0901AC	9.0901AD	9.0901AE	9.0901AF	9.0901AG	9.0901AH
9.0901BA	9.0901BB	9.0901BC	9.0901BD	9.0901BE	9.0901BF	9.0901BG	9.0901BH
9.0901CA	9.0901CB	9.0901CC	9.0901CD	9.0901CE	9.0901CF	9.0901CG	9.0901CH

Fig 9.0901

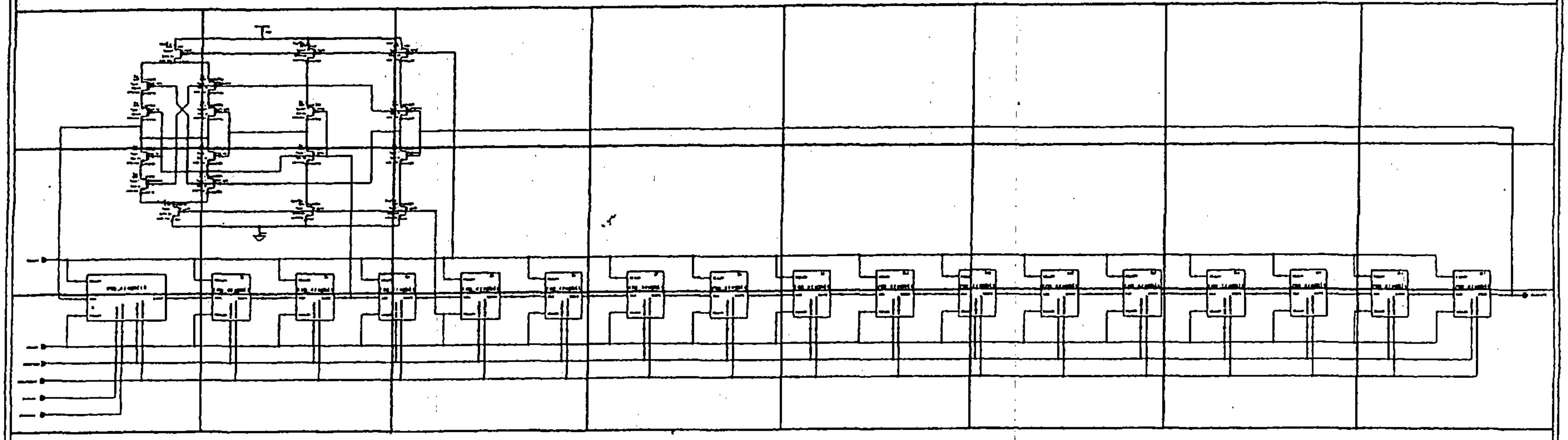
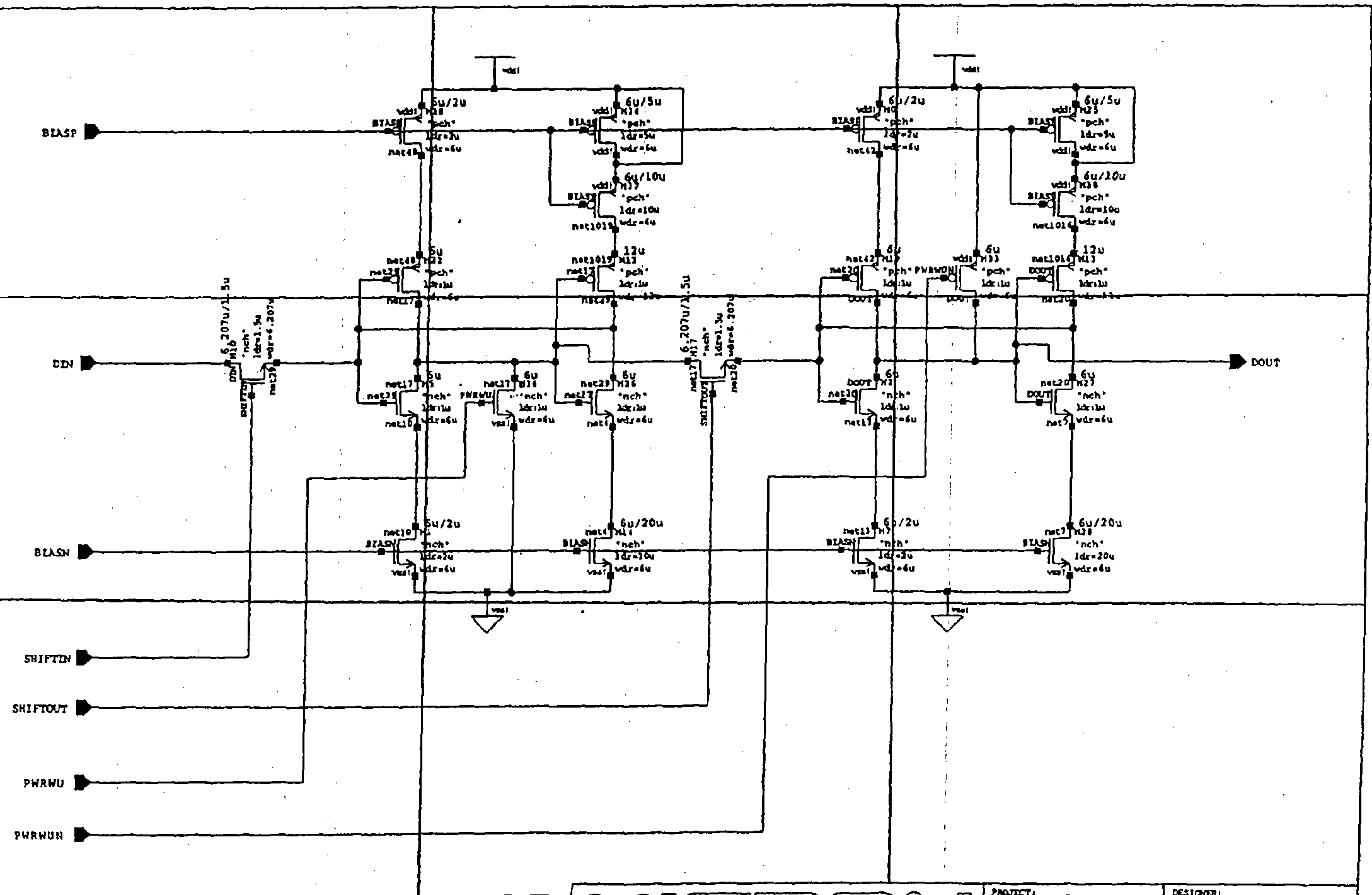


FIG. 9.0901

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

9.090101AA	9.090101AB	9.090101AC
9.090101BA	9.090101BB	9.090101BC
9.090101CA	9.090101CB	9.090101CC

Fig 9.090101



B8: increased L of passgates
decreased L of pch keepers

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: RCG Shift Register Bit0			
NAME: 103reva/rcg_sregbit0	REV: B8	SIZE: A	
DATE: Jan 25 13:22:35 1996	SHEET:		

FIG. 9.090101

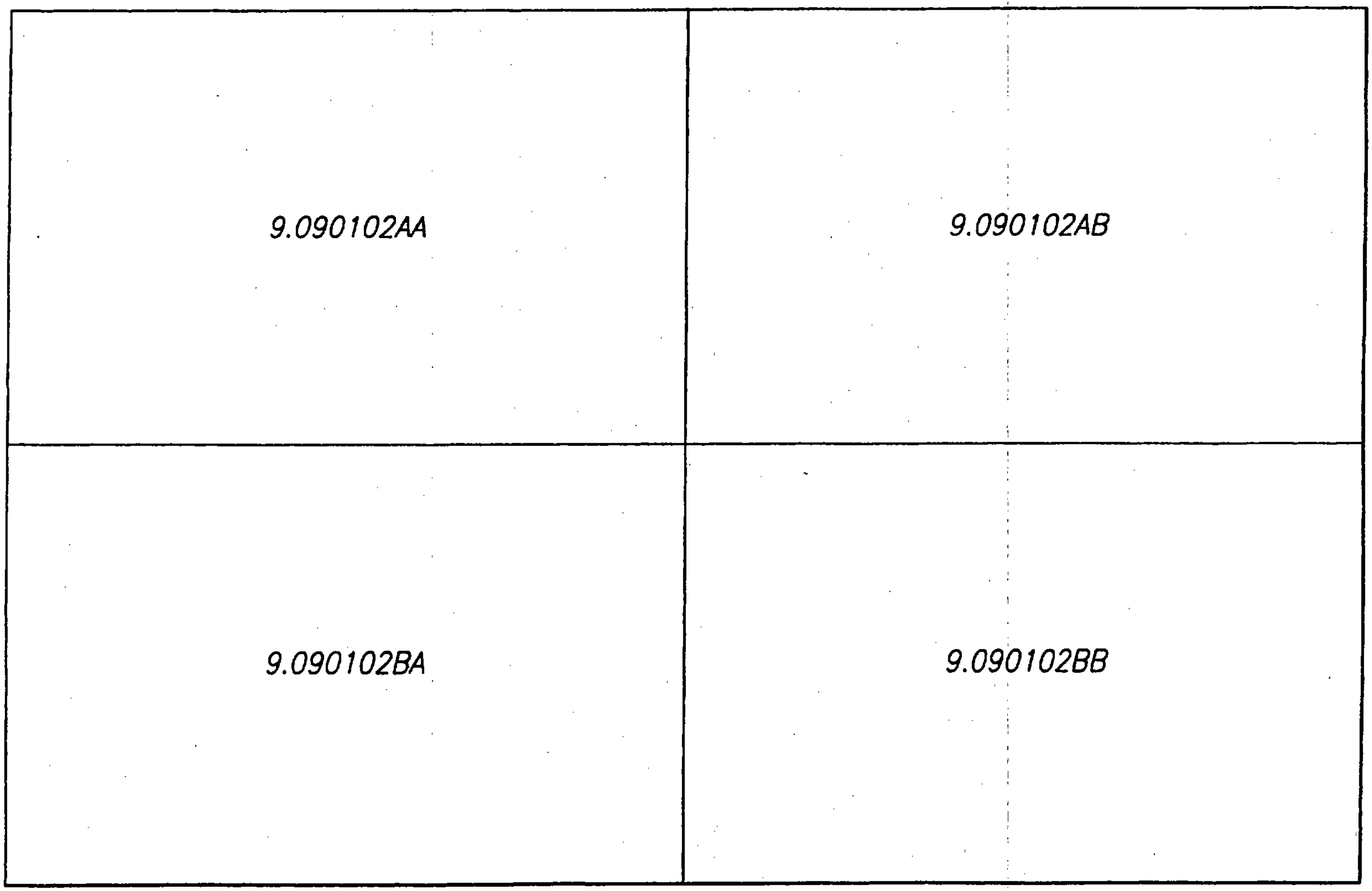
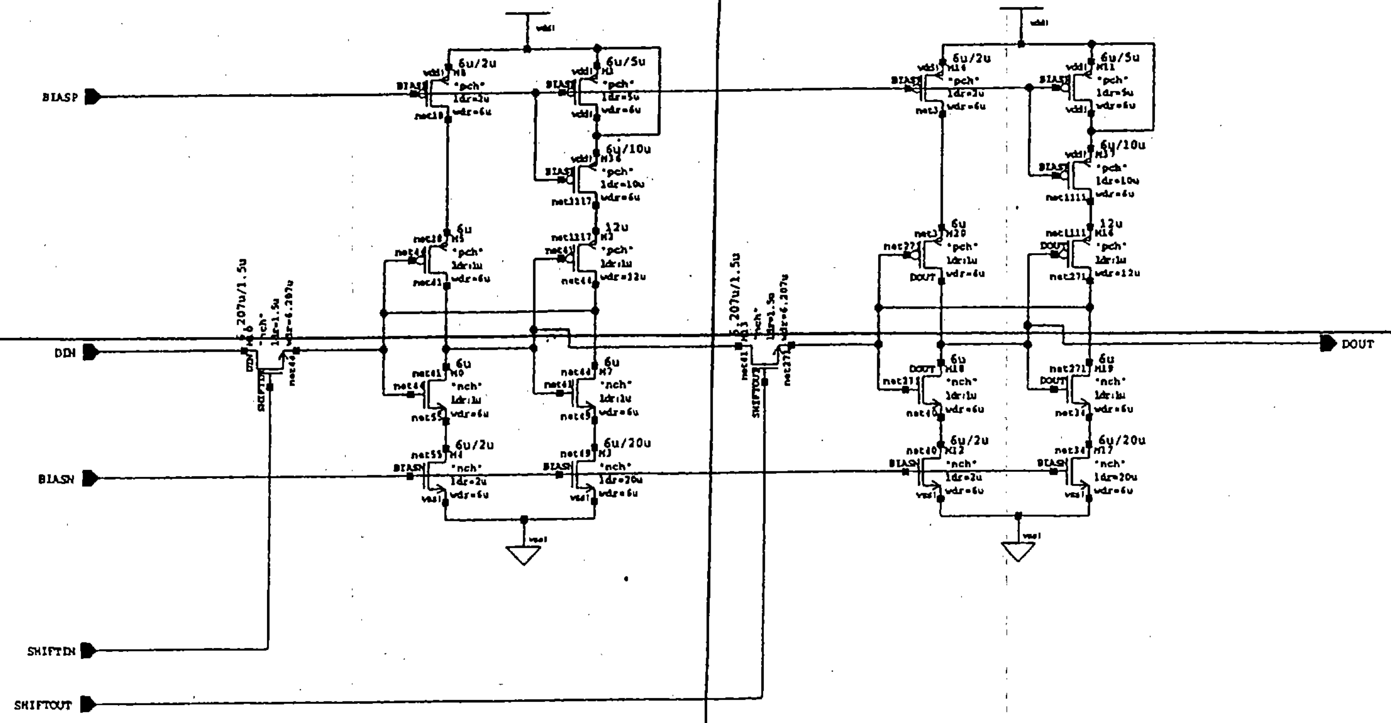


Fig 9.090102



B8: increased L of passgates
decreased L of pch keepers

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: RCG Shift Register Bit	
NAME: 103reva/rcg_sregbit	REV: B8 SIZE: A
DATE: Jan 25 13:25:16 1996	SHEET:

Fig. 9.090102

9.0902AA	9.0902AB	9.0902AC	9.0902AD	9.0902AE	9.0902F	9.0902AG	9.0902AH	9.0902AI	9.0902AJ	9.0902AK	9.0902AL
9.0902BA	9.0902BB	9.0902BC	9.0902BD	9.0902BE	9.0902F	9.0902BG	9.0902BH	9.0902BI	9.0902BJ	9.0902BK	9.0902BL
		9.0902CC	9.0902CD	9.0902CE	9.0902F	9.0902CG	9.0902CH	9.0902CI	9.0902CJ	9.0902CK	9.0902CL
		9.0902DC	9.0902DD	9.0902DE	9.0902F						9.0902DL
9.0902EA	9.0902EB	9.0902EC	9.0902ED	9.0902EE	9.0902F	9.0902EG	9.0902EH	9.0902EI	9.0902EJ	9.0902EK	9.0902EL
			9.0902FD	9.0902FE	9.0902F	9.0902FG	9.0902FH	9.0902FI	9.0902FJ	9.0902FK	9.0902FL

Fig 9.0902

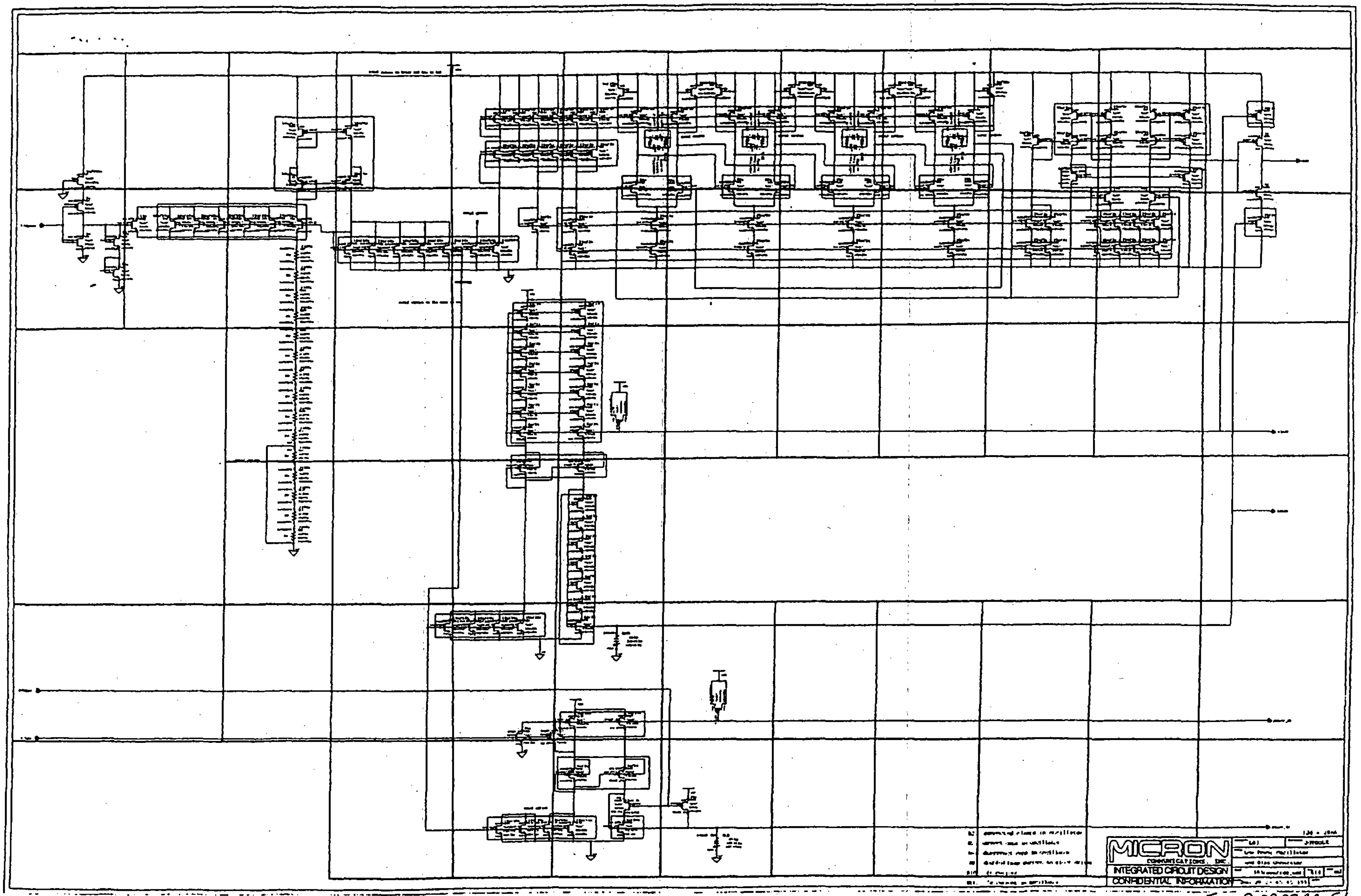


FIG. 9.0902AA-FL

9.0903AA	9.0903AB	9.0903AC
9.0903BA	9.0903BB	9.0903BC
9.0903CA	9.0903CB	9.0903CC

FIG 9.0903

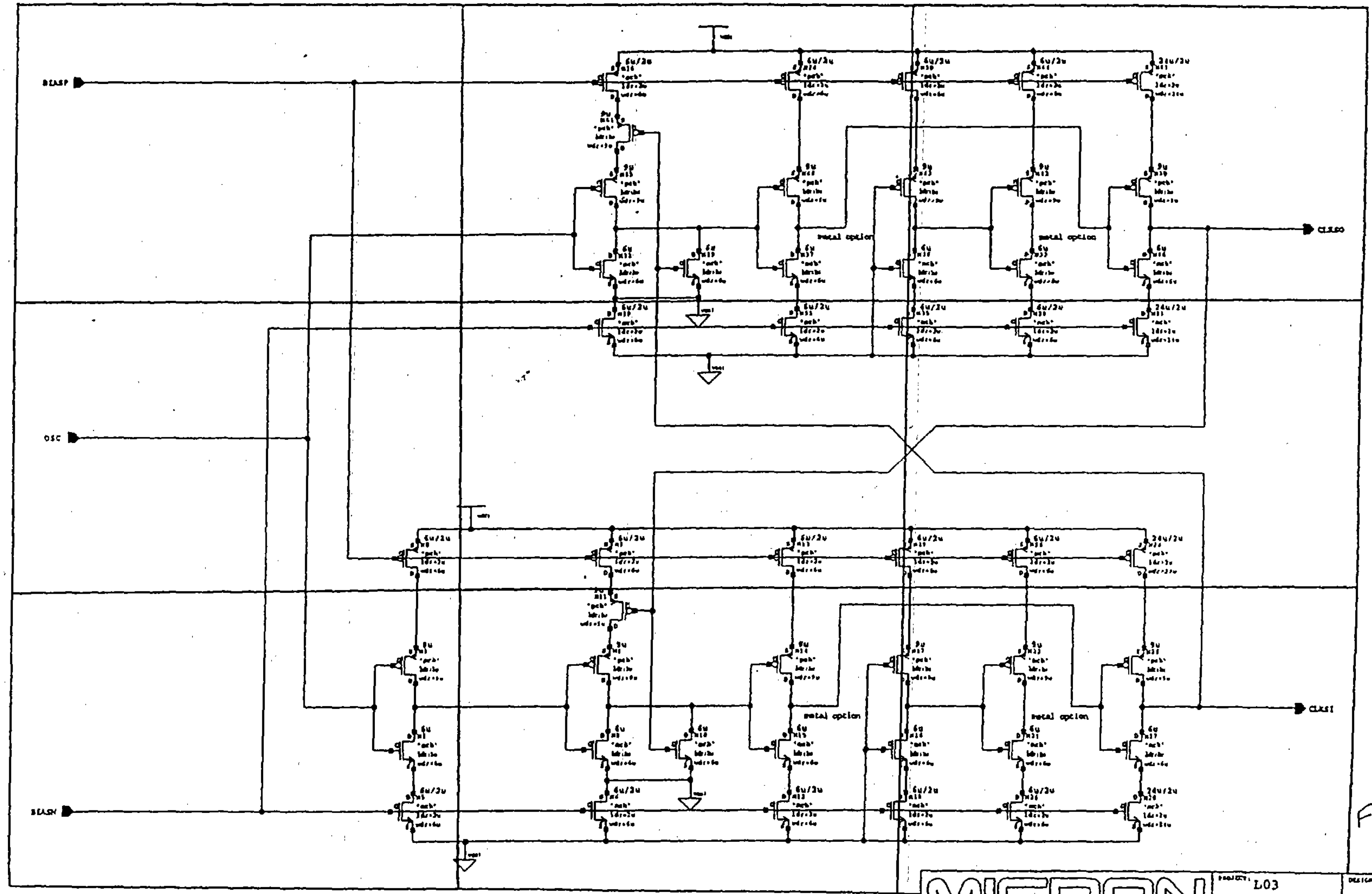


Fig. 9.0903

B8: wired cross-couples to ground

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03
JOTOOLE
Clock Generator
103reva/rcg_clkgen
B8
nil
Jan 24 09:56:43 1996

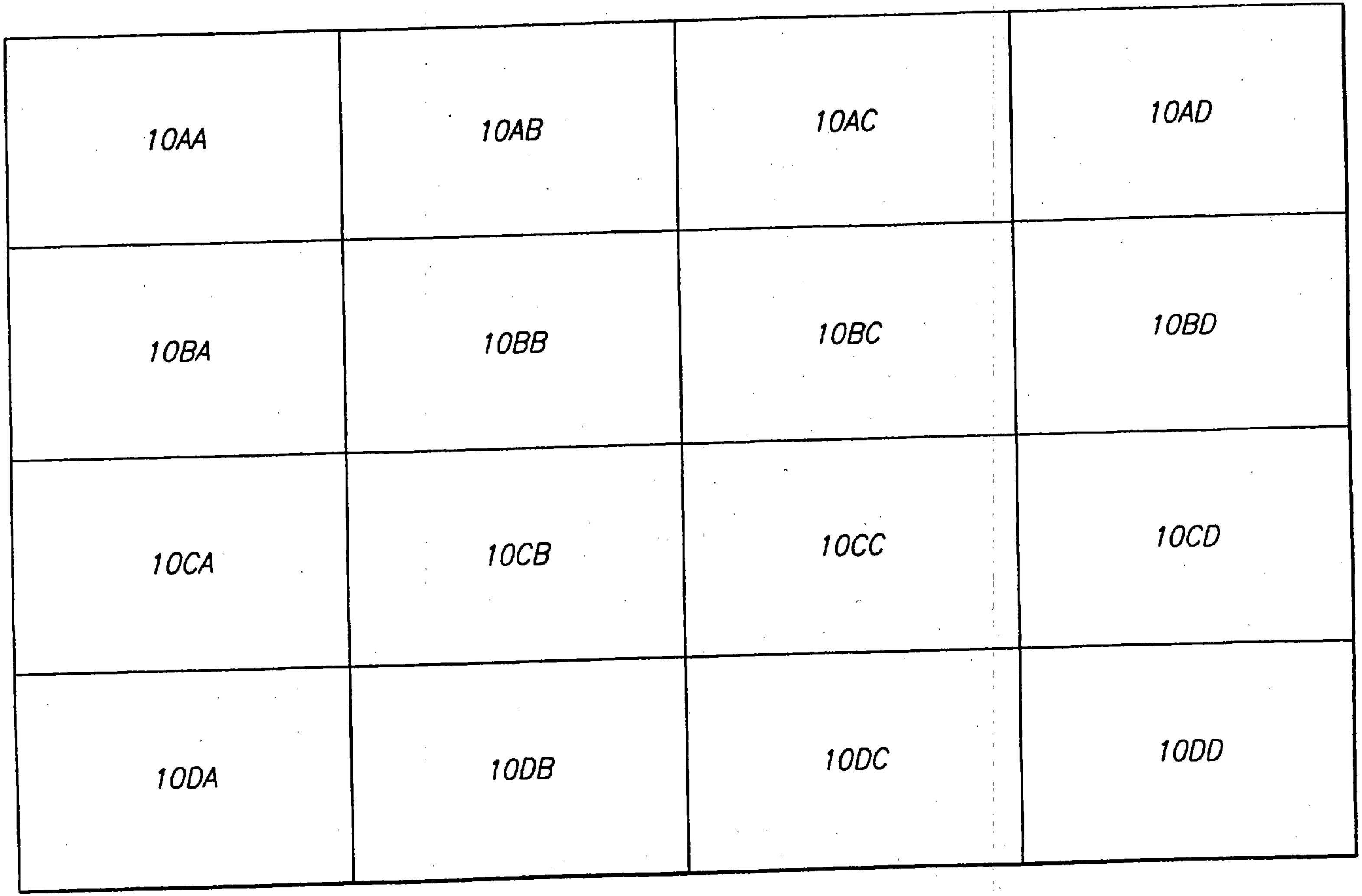

10AA
10AB
10AC
10AD
10BA
10BB
10BC
10BD
10CA
10CB
10CC
10CD
10DA
10DB
10DC
10DD

Fig 10

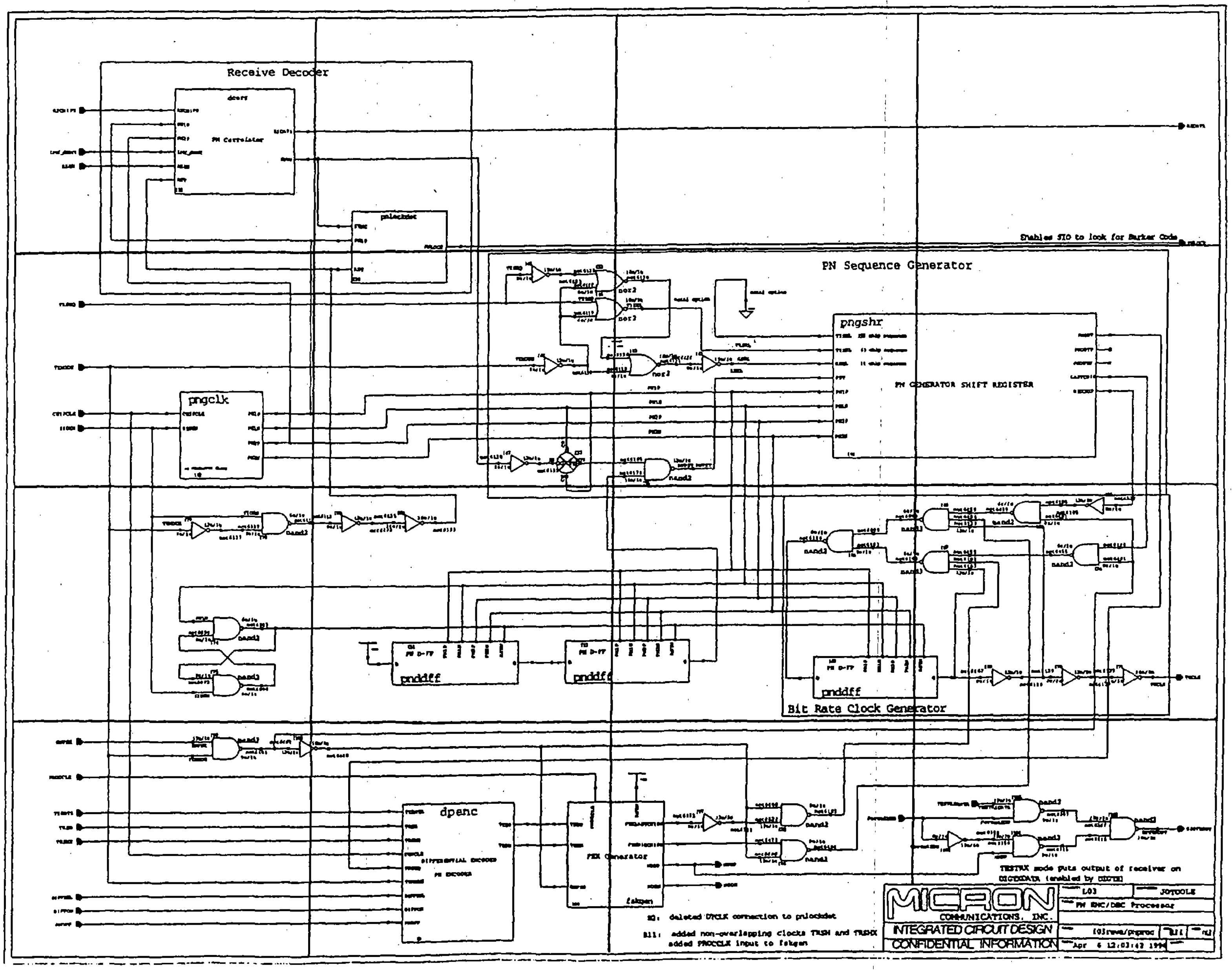

Receive Decoder
dcorr
PN Correlator
pnlockdet
PN Sequence Generator
pngshr
PN GENERATOR SHIFT REGISTER
pngclk
nor2
nand2
nand3
pnddff
PN D-FF
Bit Rate Clock Generator
dpenc
DIFFERENTIAL ENCODER
PN ENCODER
FSK Generator
fskgen
Enables SIO to look for Barker Code
TESTRX mode puts output of receiver on DICEDDATA (enabled by DIOTE)
S2: deleted DTCLK connection to pnlockdet
B11: added non-overlapping clocks TRSH and TRSHX
added PROCCLK input to fskgen
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
JOTOOLE
PN ENC/DEC Processor
[0]revb/pnproc
B11
Apr 6 12:03:42 1994

FIG. 10

	10.01BJ	10.01CJ	10.01DJ
	10.01BI	10.01CI	10.01DI
	10.01BH	10.01CH	10.01DH
10.01AG	10.01BG	10.01CG	10.01DG
10.01AF	10.01BF	10.01CF	10.01DF
10.01AE	10.01BE	10.01CE	10.01DE
10.01AD	10.01BD	10.01CD	10.01DD
10.01AC	10.01BC	10.01CC	10.01DC
10.01AB	10.01BB	10.01CB	10.01DB
10.01AA	10.01BA	10.01CA	

Fig. 10.01

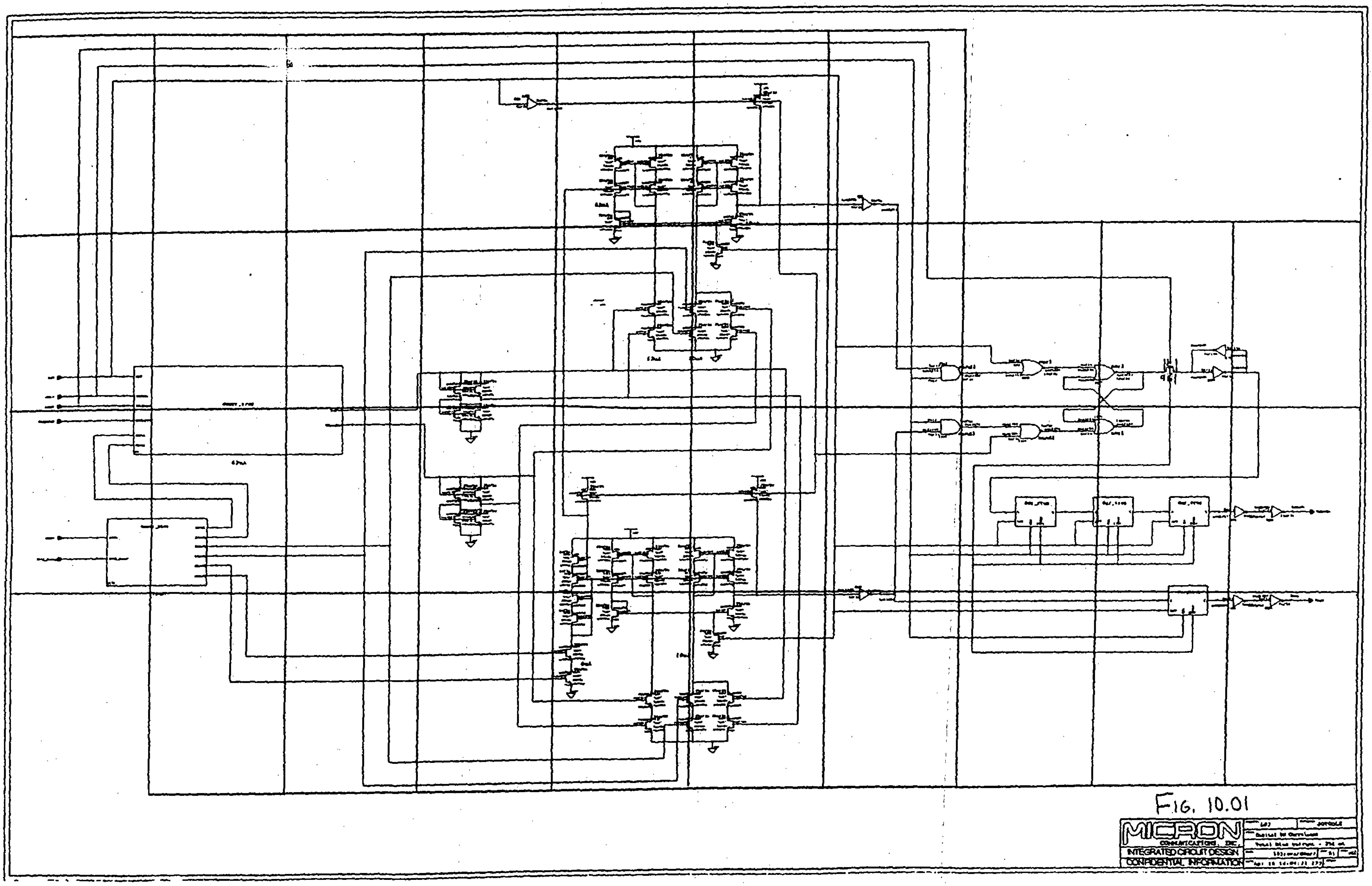

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

FIG. 10.01

10.0101AA	10.0101AB	10.0101AC	10.0101AD	10.0101AE	10.0101AF	10.0101AG
10.0101BA	10.0101BB	10.0101BC	10.0101BD	10.0101BE	10.0101BF	10.0101BG

Fig 10.0101

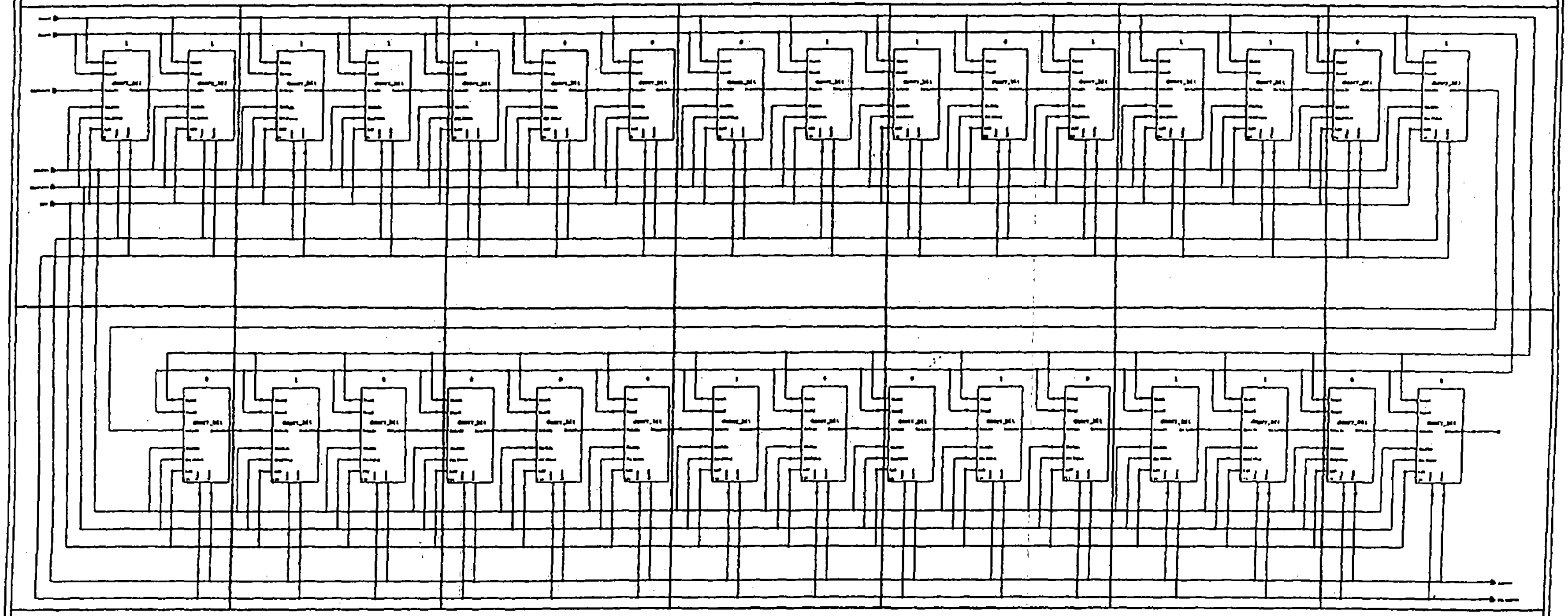
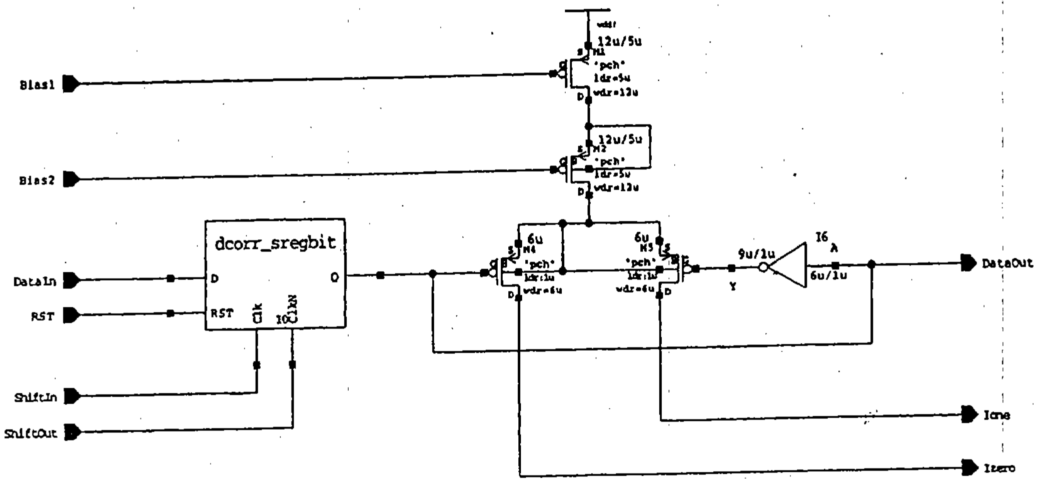


Fig. 10.0101

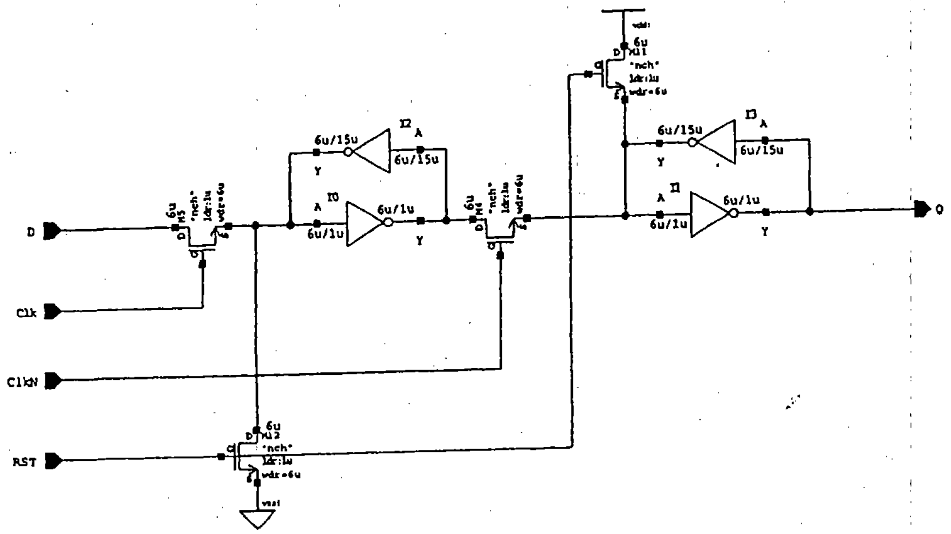
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: Correlator Bit			
NAME: 103reva/dcorr_bit	REV: B1	SIZE: A	
DATE: Sep 9 11:37:26 1994	SHEET:		

FIG. 10.010101



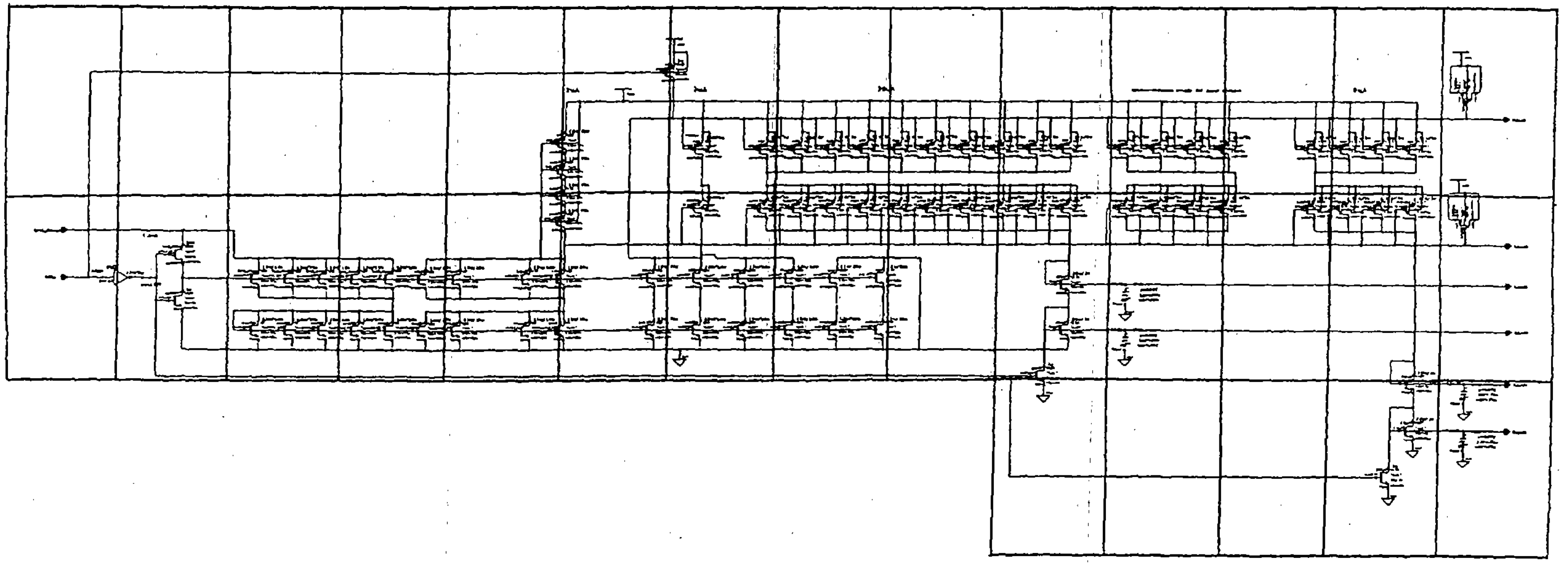
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: Shift Register Cell
NAME: l03reva/dcorr_sregbit
REV: B1
SIZE: A
DATE: Sep 9 14:08:50 1994
SHEET:

FIG. 10.01010101

10.0102AA	10.0102AB	10.0102AC	10.0102AD	10.0102AE	10.0102AF	10.0102AG	10.0102AH	10.0101AI	10.0102AJ	10.0102AK	10.0102AL	10.0102AM	10.0102AN
10.0102BA	10.0102BB	10.0102BC	10.0102BD	10.0102BE	10.0102BF	10.0102BG	10.0102BH	10.0101AI	10.0102BJ	10.0102BK	10.0102BL	10.0102BM	10.0102BN
									10.0102CJ	10.0102CK	10.0102CL	10.0102CM	10.0102CN

FIG 10.0102



10.02AA	10.02AB	10.02AC	10.02AD	10.02AE
10.02BA	10.02BB	10.02BC	10.02BD	10.02BE

Fig 10.02

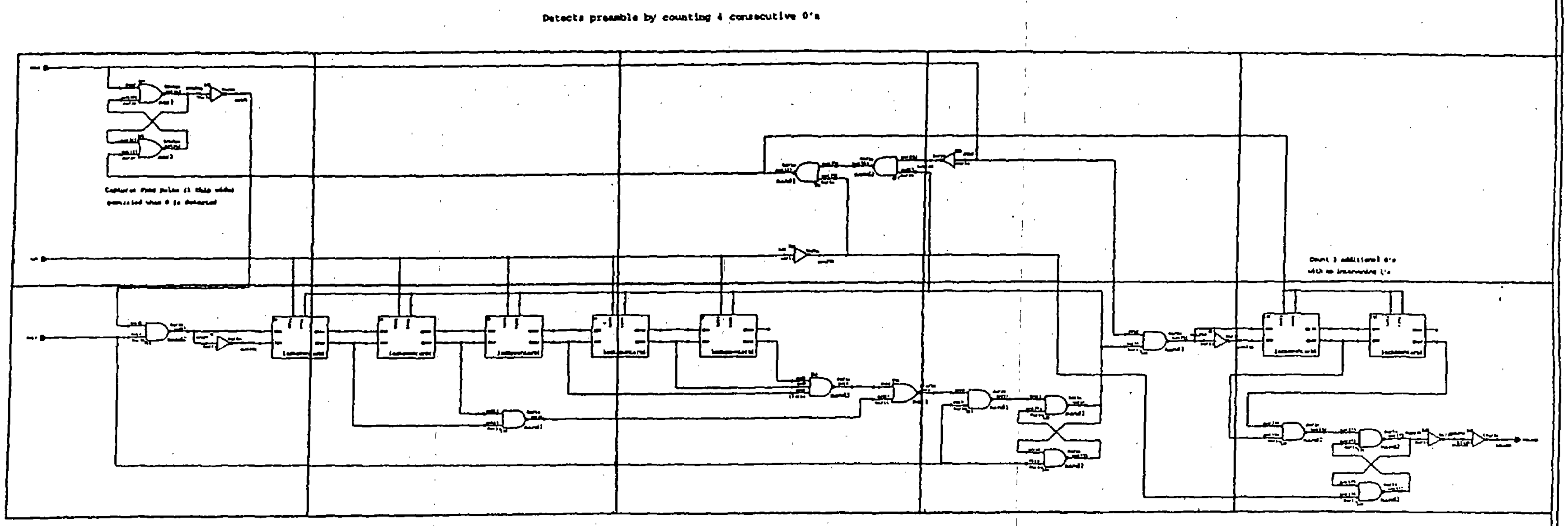

Detects preamble by counting 4 consecutive 0's
Captures [illegible] pulse (1 chip wide) generated when 0 is detected
Count 3 additional 0's with no intervening 1's

FIG. 10.02

MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

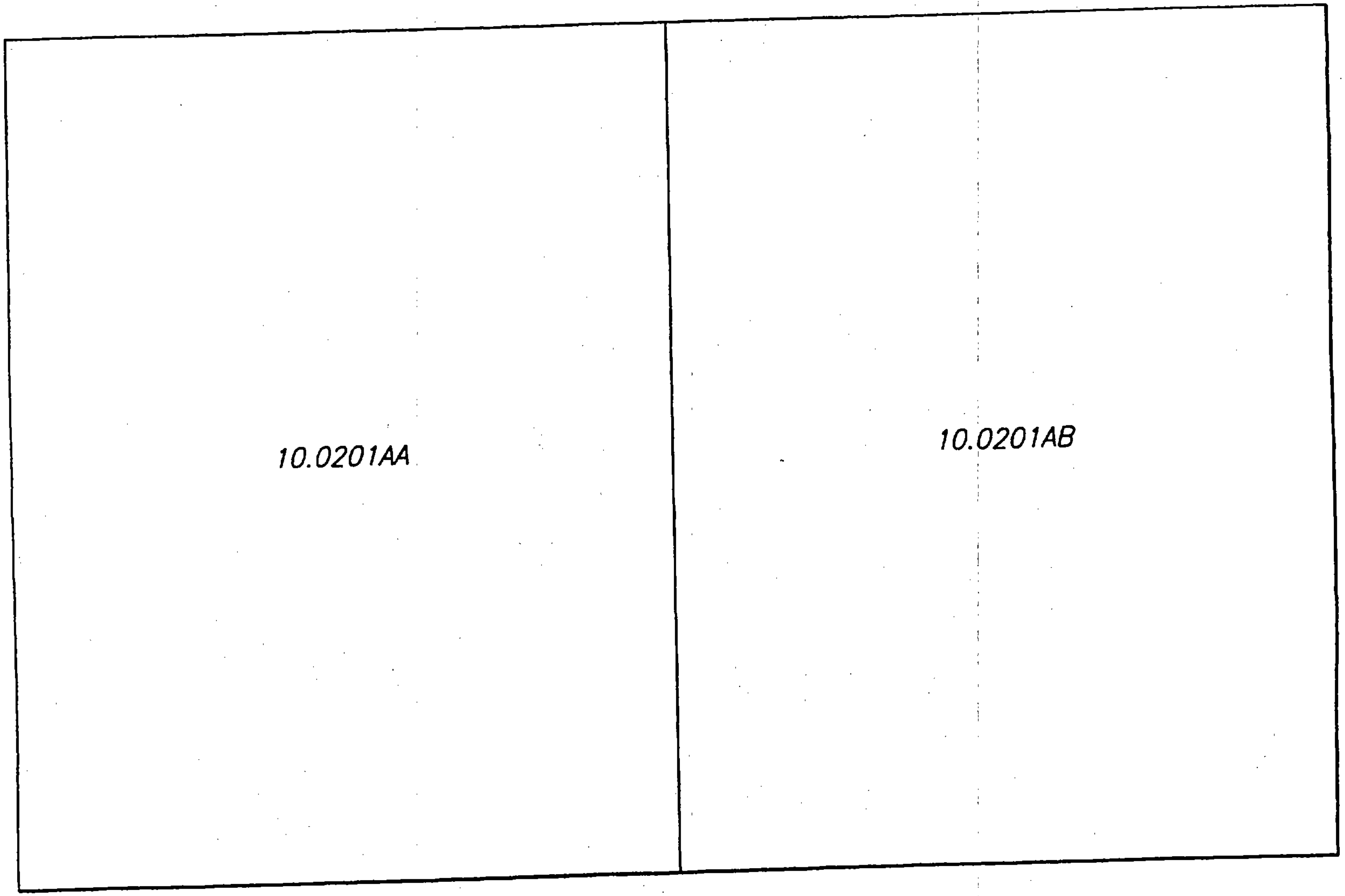
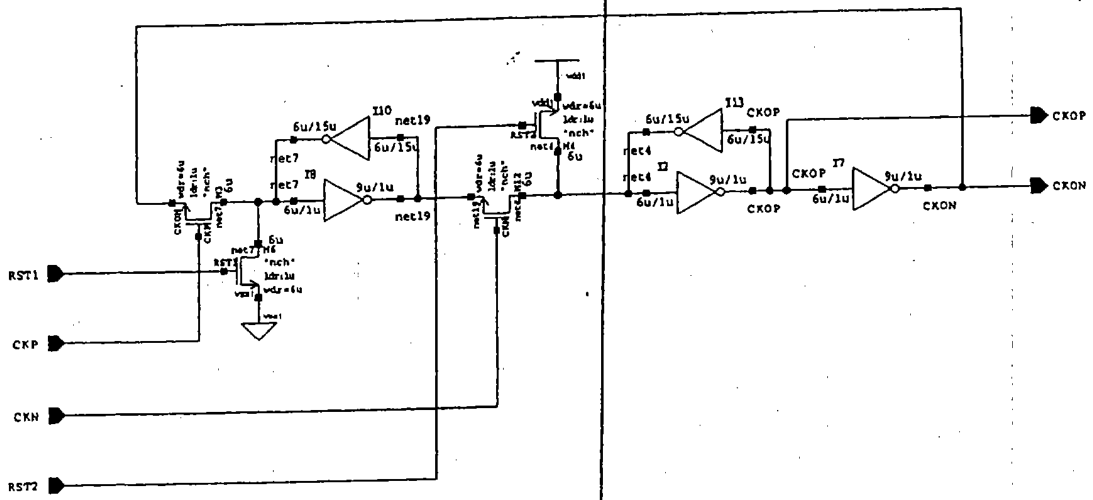


FIG 10.0201



MICRON COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

PROJECT: L03

DESIGNER: JOTOOLE

TITLE: PN Lock Detector Counter Bit

NAME: l03reva/lockcounterbit

REV: B1

SIZE: A

DATE: Aug 31 14:28:22 1994

SHEET:

FIG. 10.0201

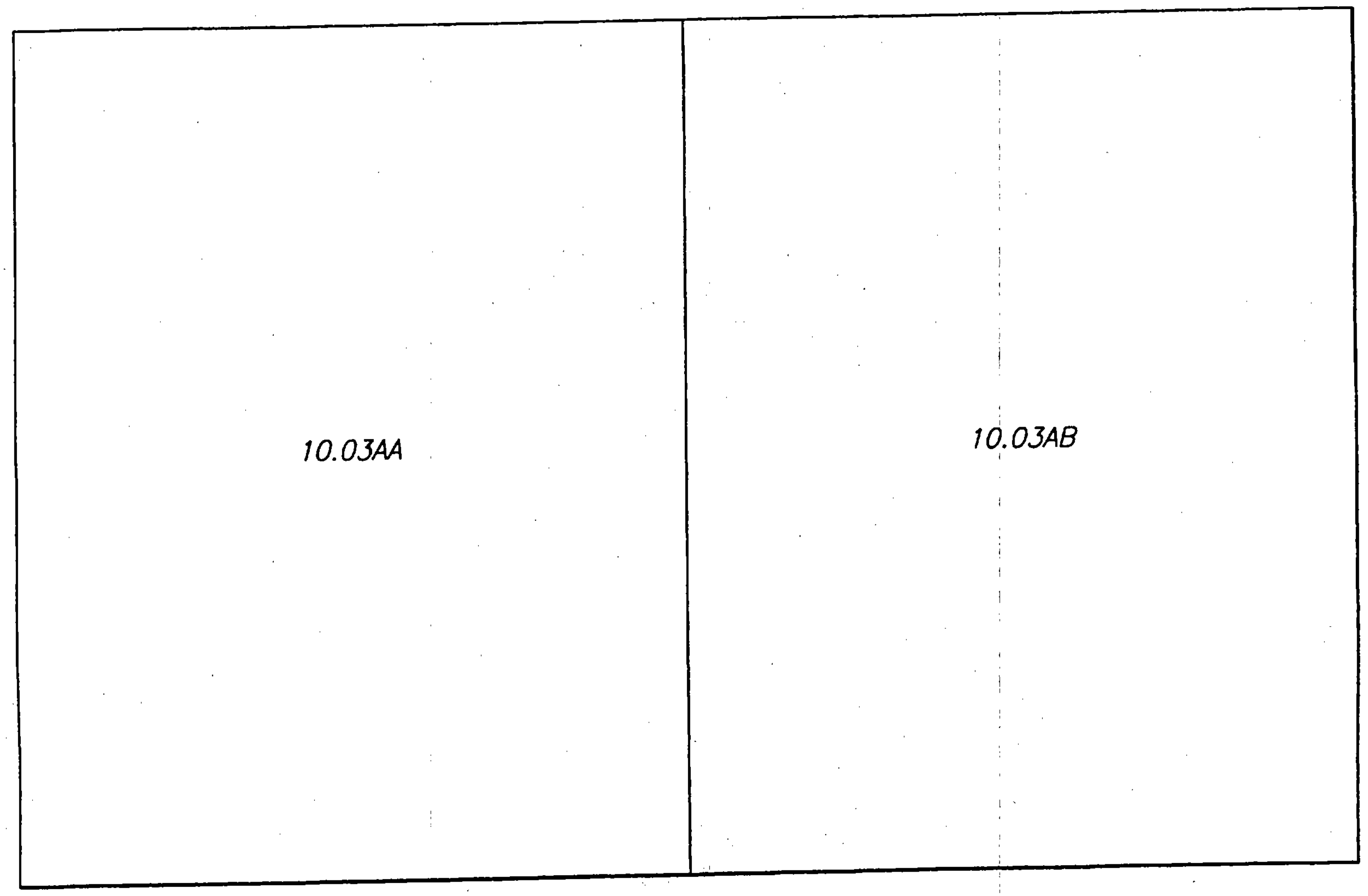
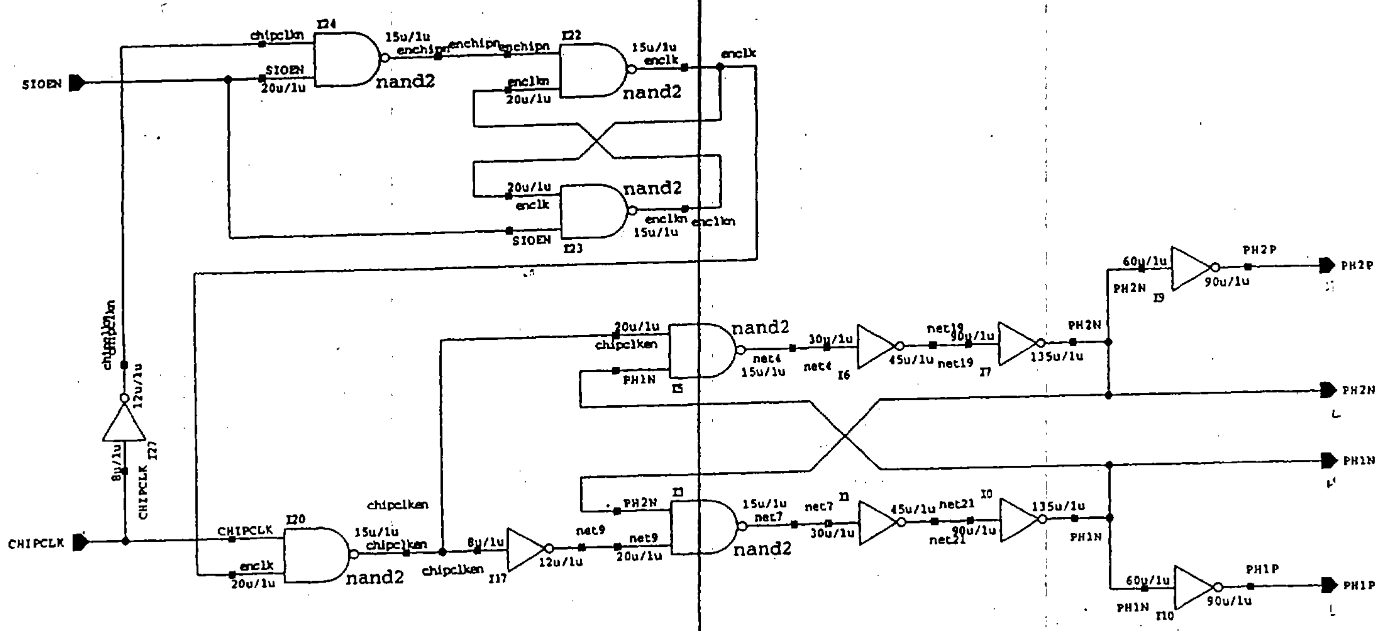


FIG 10.03



MICRON COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

PROJECT: L03

DESIGNER: Rotzoll

TITLE: PN Generator Clock

NAME: 103reva/pngclk

REV: -

SIZE: A

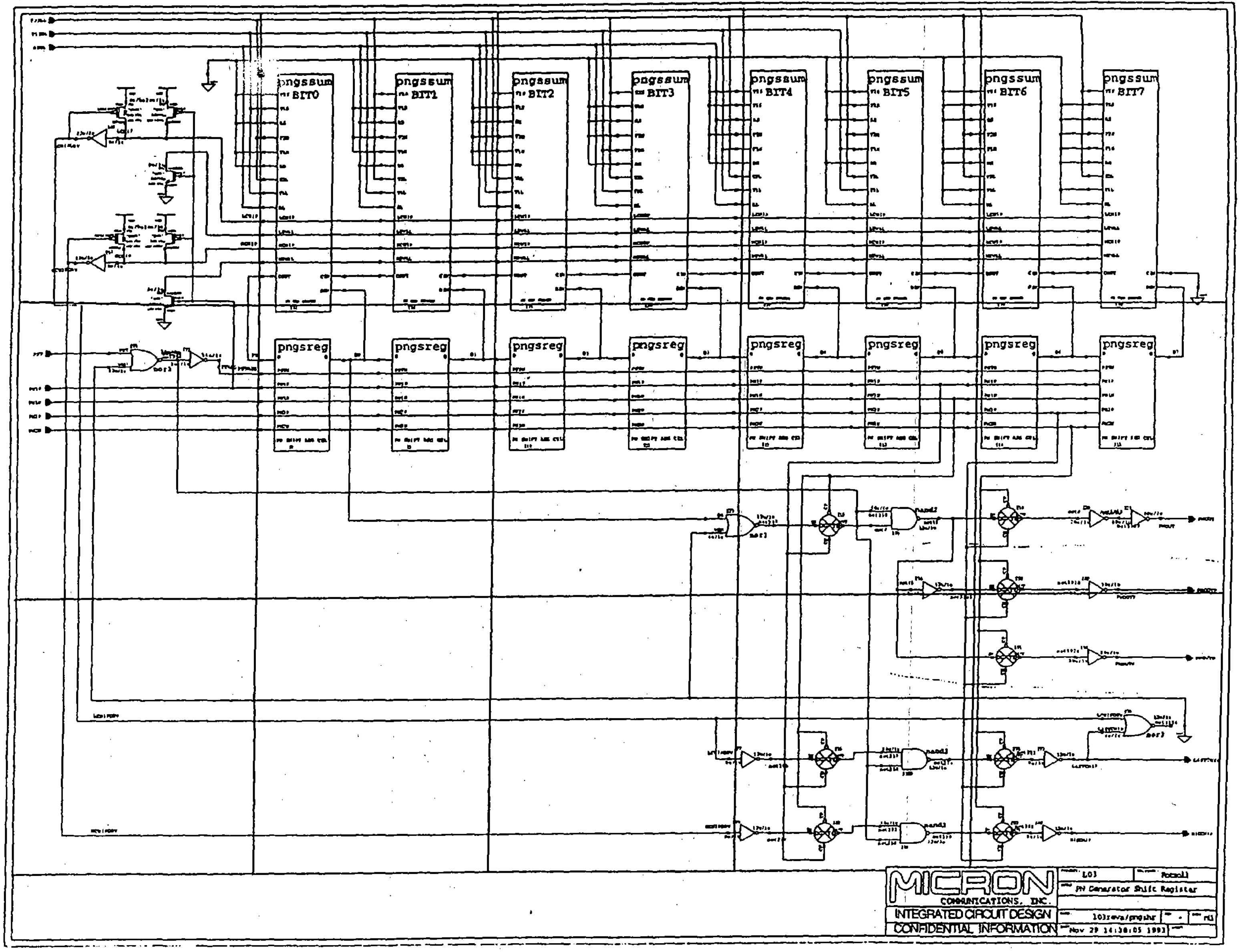
DATE: Nov 29 11:20:57 1993

SHEET:

FIG. 10.03

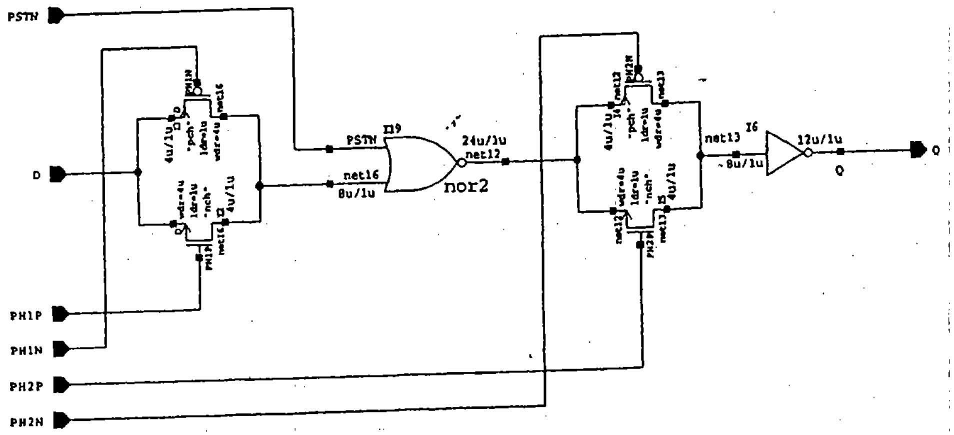
10.04AA	10.04AB	10.04AC	10.04AD	10.04AE
10.04BA	10.04BB	10.04BC	10.04BD	10.04BE
10.04CA	10.04CB	10.04CC	10.04CD	10.04CE

Fig 10.04



not used

FIG. 10.09



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: PN Generator Shift Register Cell
NAME: 103reva/pngsreg
REV: -
SIZE: A
DATE: Nov 20 21:22:37 1993
SHEET:

FIG. 10.0401

10.0402AA	10.0402AB
10.0402BA	10.0402BB
10.0402CA	10.0402CB

Fig 10.0402

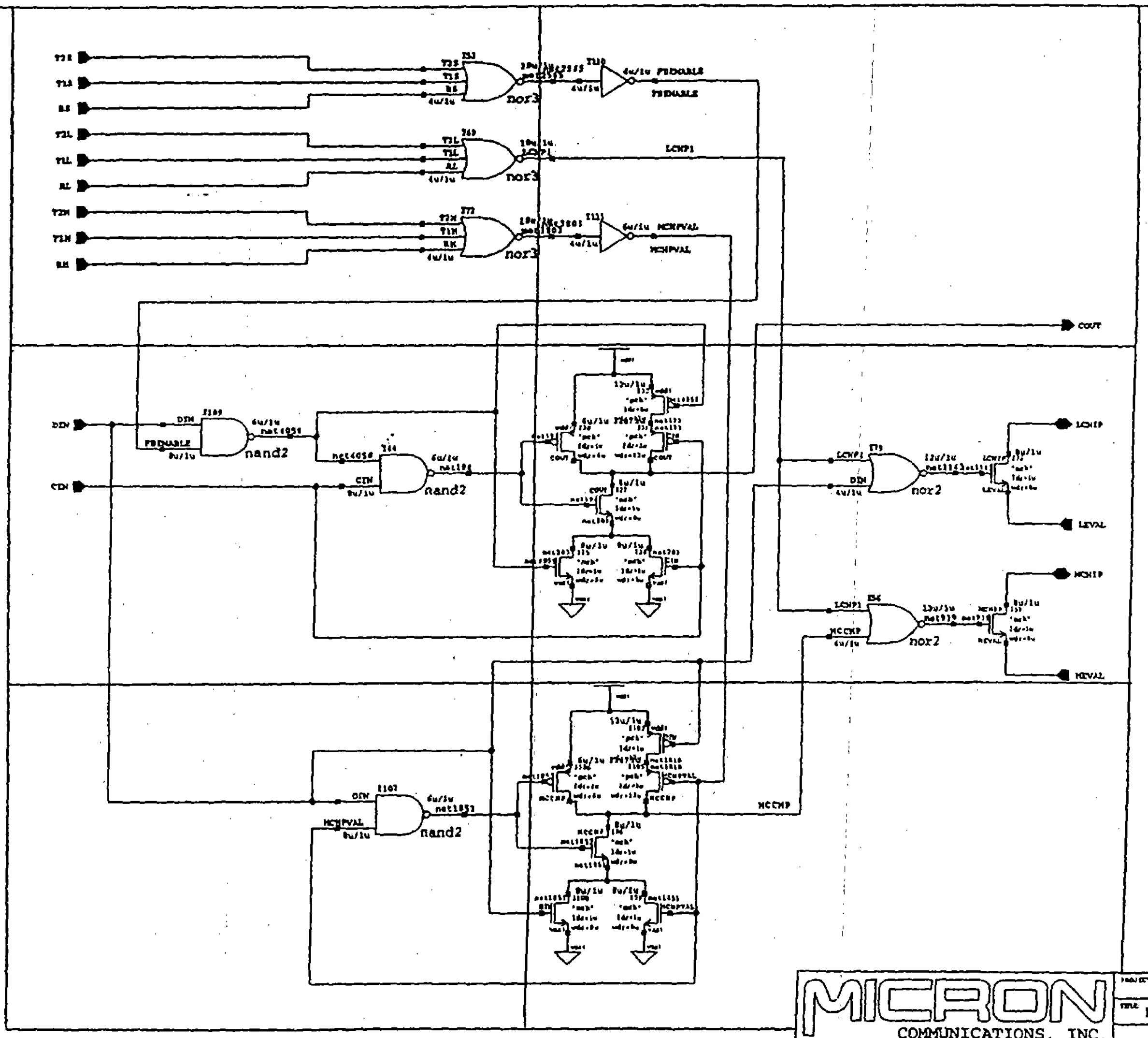
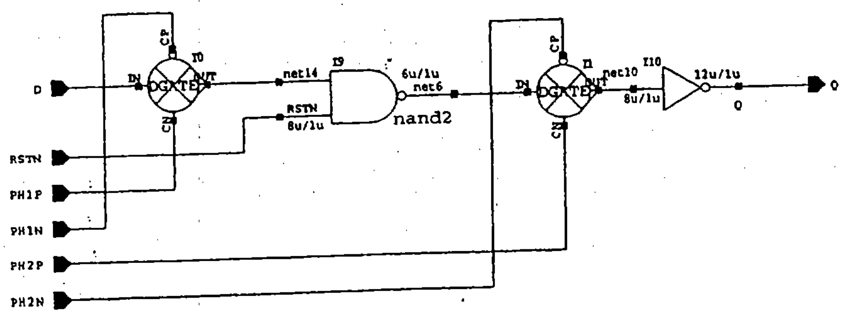


FIG. 10.0402

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03		Rotzoll	
PN Gen Shift Reg Summer			
103reva/pngssum		-	nil
Nov 20 21:23:00 1993			



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03		DESIGNER: Rotzoll	
TITLE: PN Controller D Flip-Flop			
NAME: 103reva/pnddff		REV: -	SIZE: A
DATE: Nov 26 18:12:59 1993		SHEET:	

FIG. 10.05

10.06AA	10.06AB	10.06AC	10.06AD							
10.06BA	10.06BB	10.06BC	10.06BD	10.06BE	10.06BF	10.06BG	10.06BH	10.06BI	10.06BJ	10.06BK
10.06CA	10.06CB	10.06CC	10.06CD	10.06CE	10.06CF	10.06CG	10.06CH	10.06CI	10.06CJ	10.06CK
10.06DA	10.06DB	10.06DC	10.06DD	10.06DE	10.06DF	10.06DG	10.06DH			

FIG 10.06

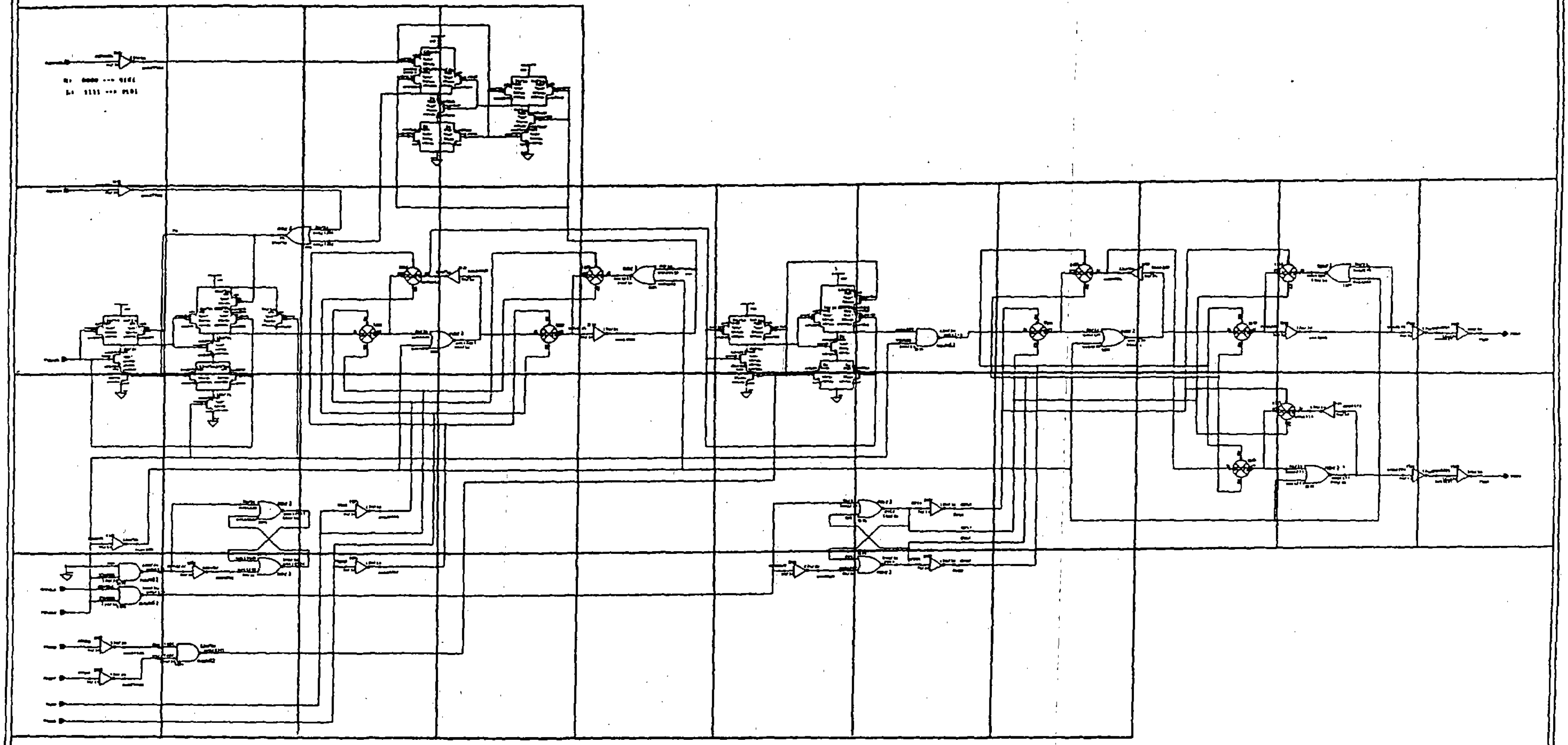
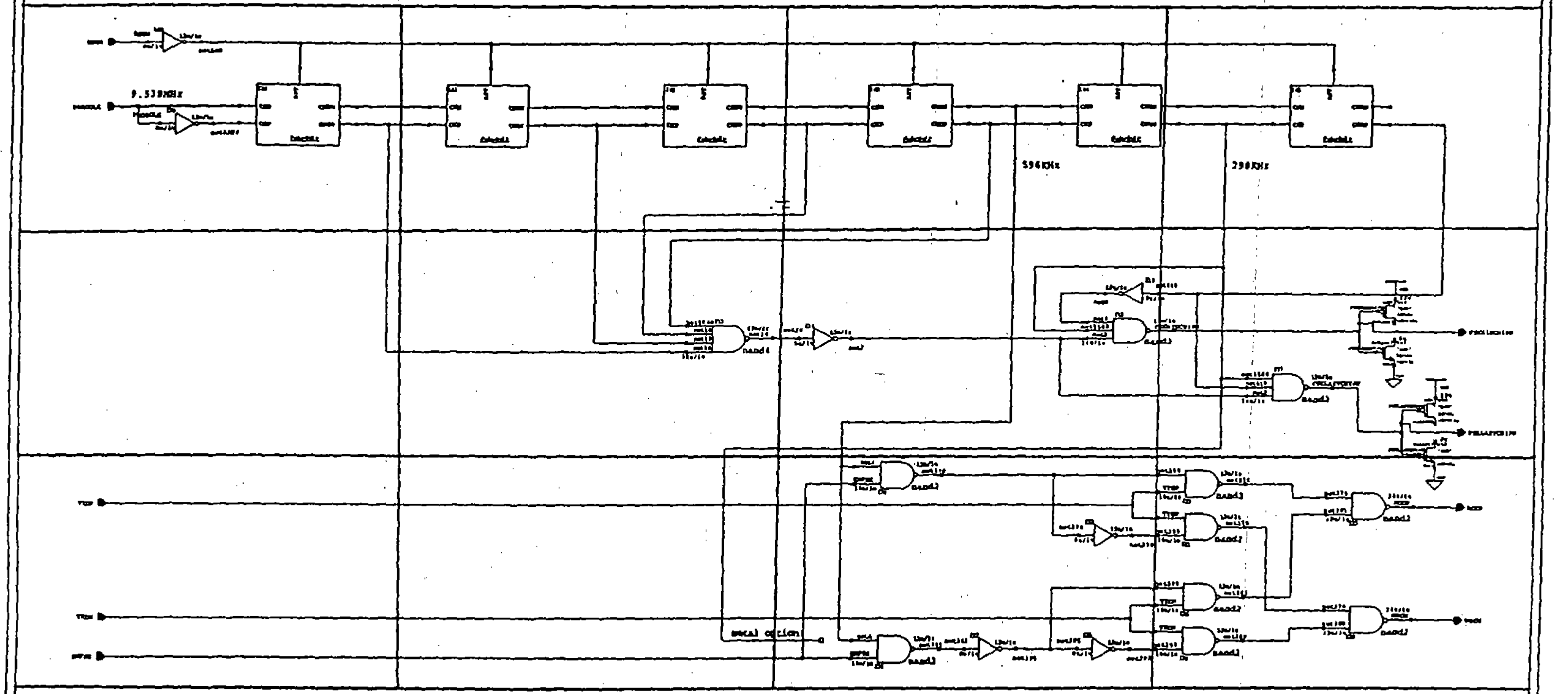


Fig. 10.06

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

10.07AA	10.07AB	10.07AC	10.07AD
10.07BA	10.07BB	10.07BC	10.07BD
10.07CA	10.07CB	10.07CC	10.07CD

Fig 10.07



B6: inverted mid and last chip outputs

B8: converted to PSK with 596KHz subcarrier

B11: changed input clock to PROCCLK so that mbs works in lowrate

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

L03	JOYDOLE
PSK/FSK Generator	
10)revs/fskpen	B11
Apr 6 11:07:10 1994	

FIG. 10.07

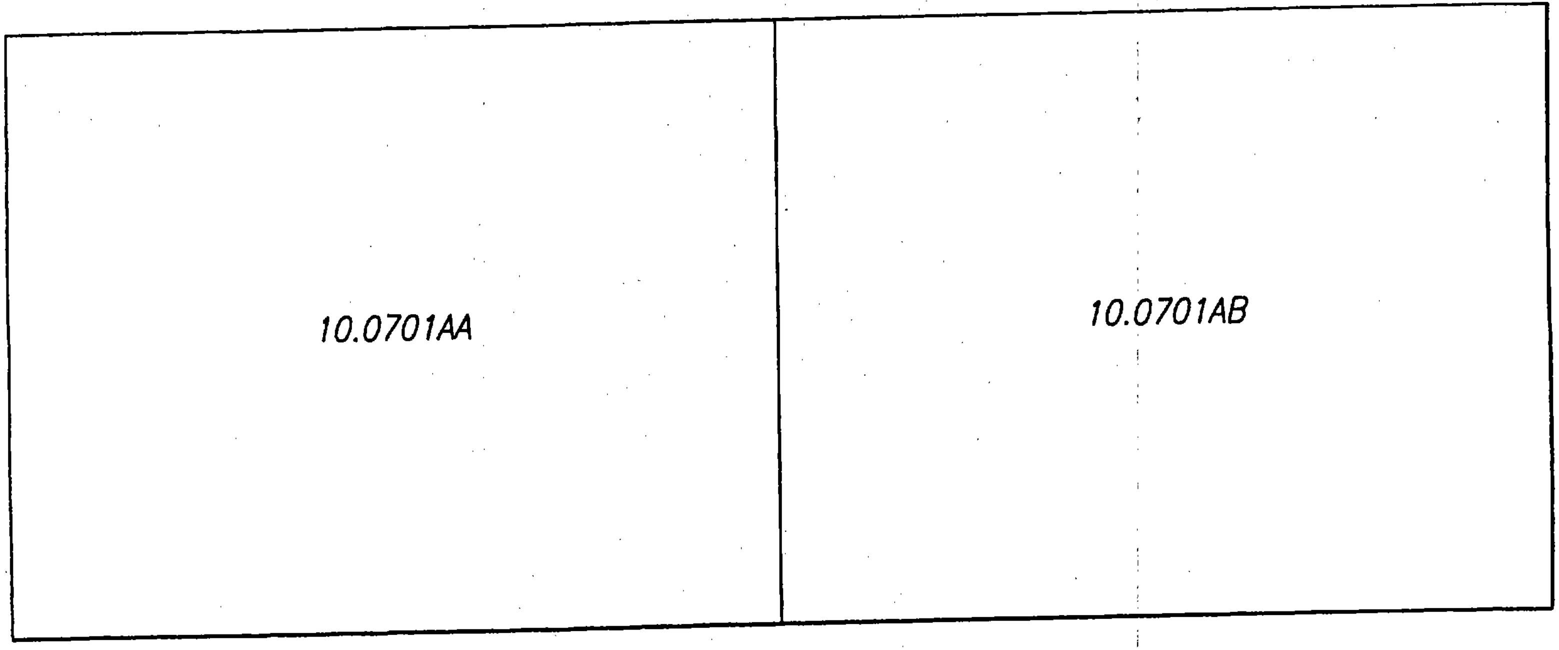
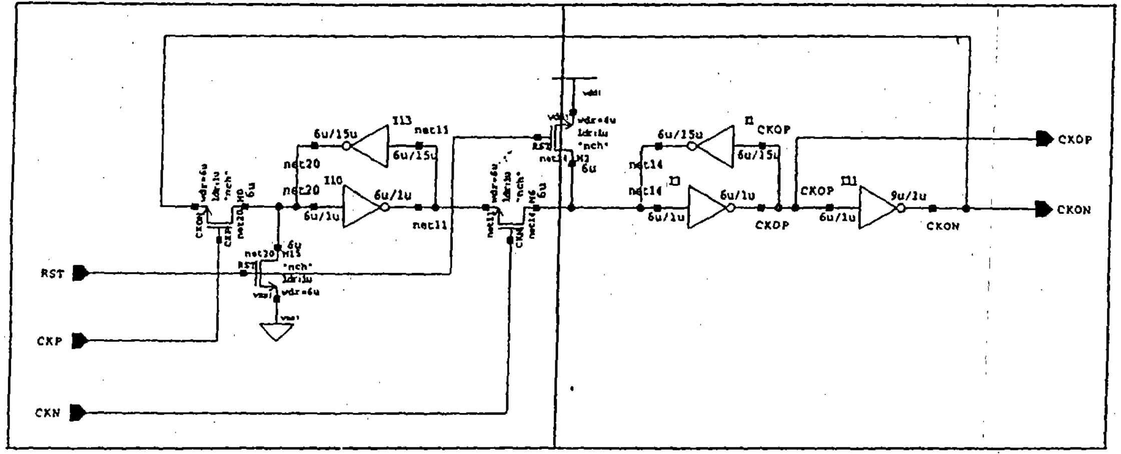


Fig 10.0701



MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03			DESIGNER: JOTOOLE		
TITLE: FSK Counter Bit					
Same as wuabort_cbit					
NAME: 103reva/fskcbit		REV: B1		SIZE: A	
DATE: Apr 17 15:42:44 1995			SHEET:		

FIG. 10.0701

MI40-030

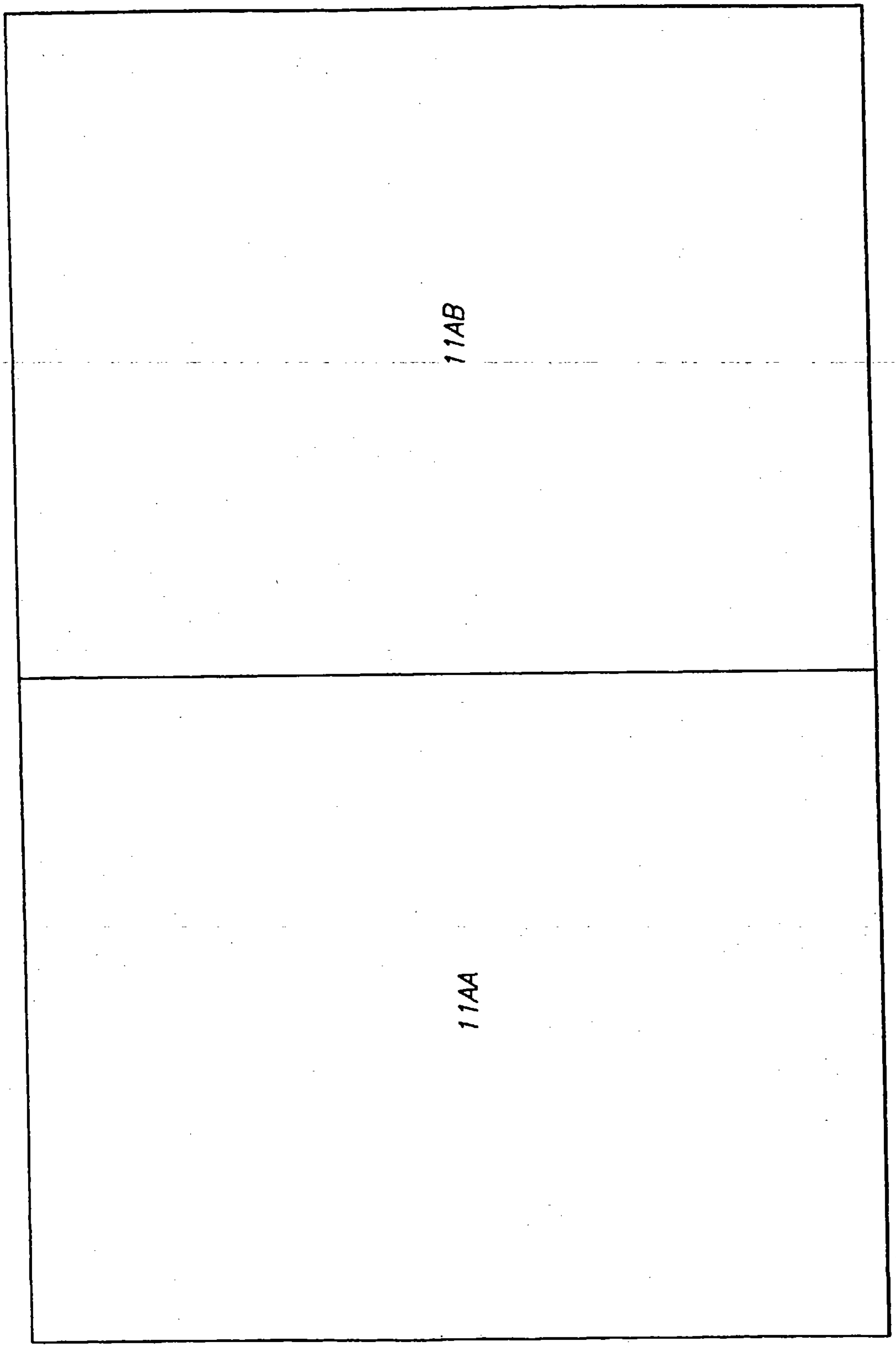
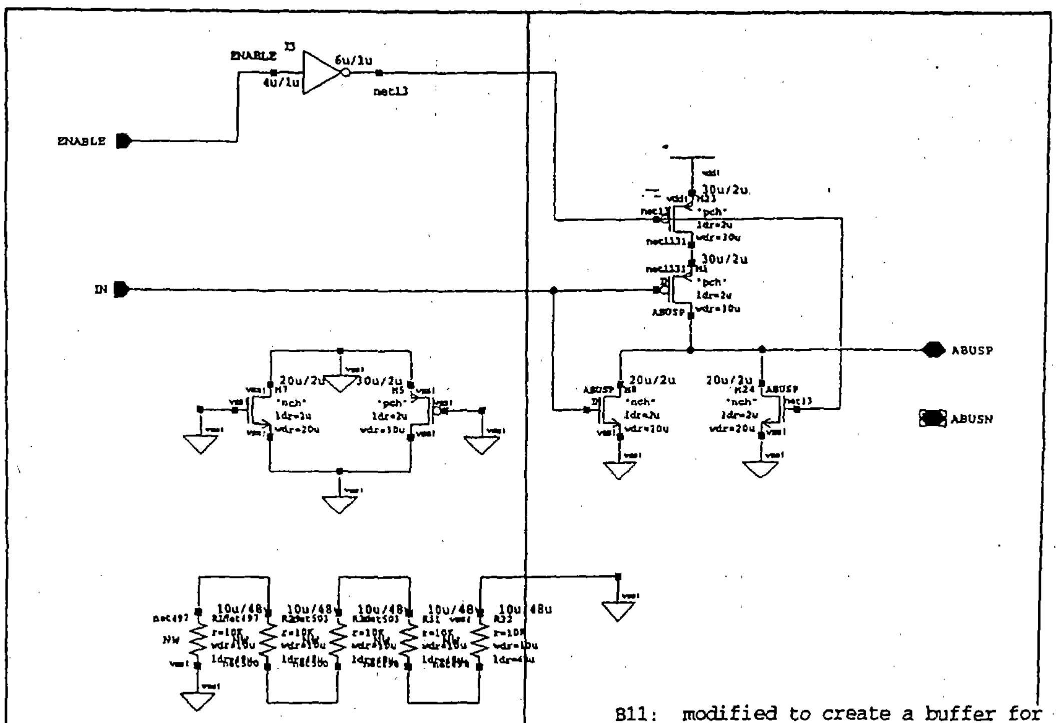


Fig. 11



B11: modified to create a buffer for the opamp output

the battery voltage divider is now part of tsn

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Battery Analog I/O Buffer	
NAME: 103reva/batalg	REV: B11 SIZE: A
DATE: Apr 8 10:19:56 1996	SHEET:

Fig. 11

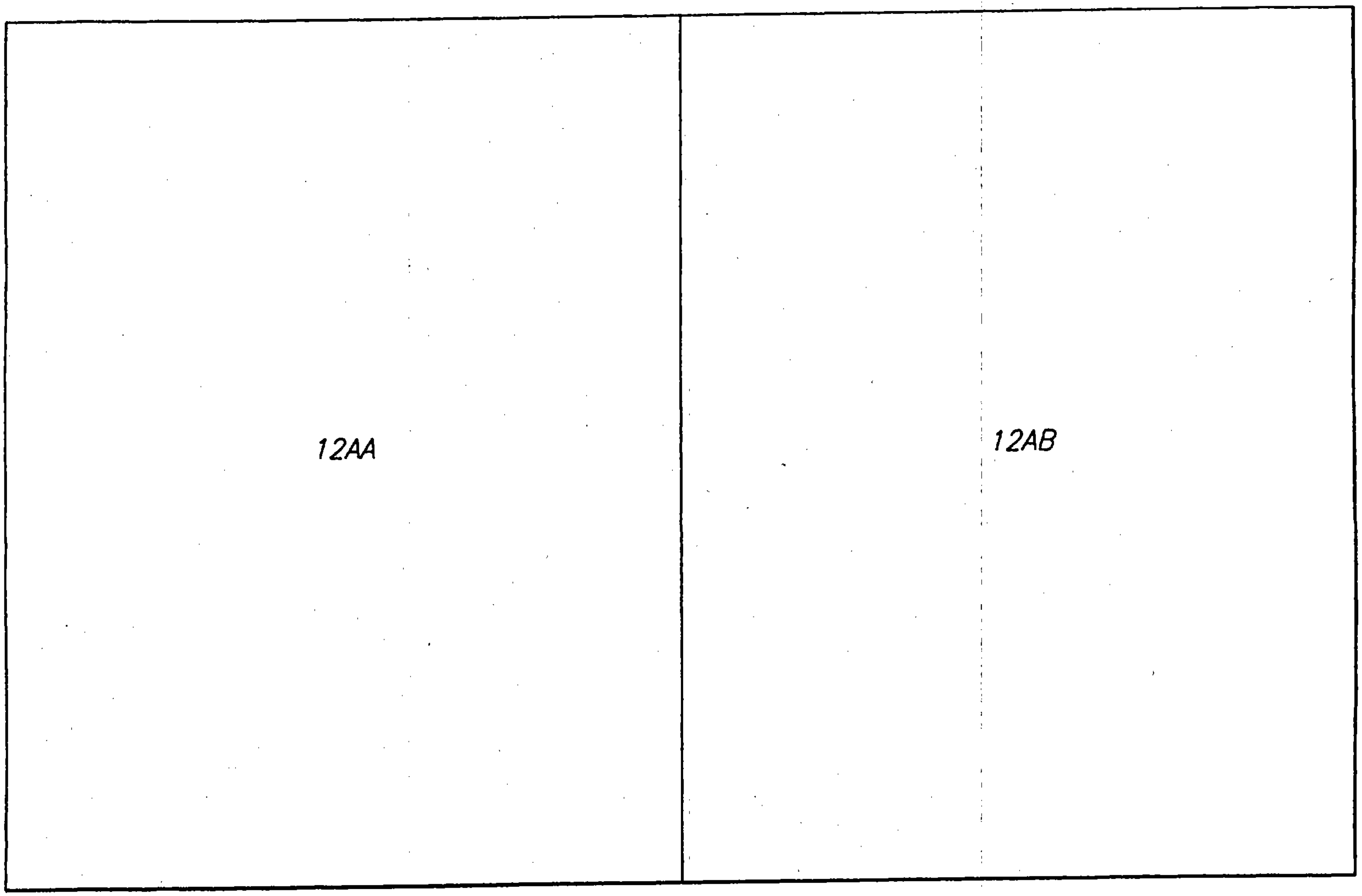
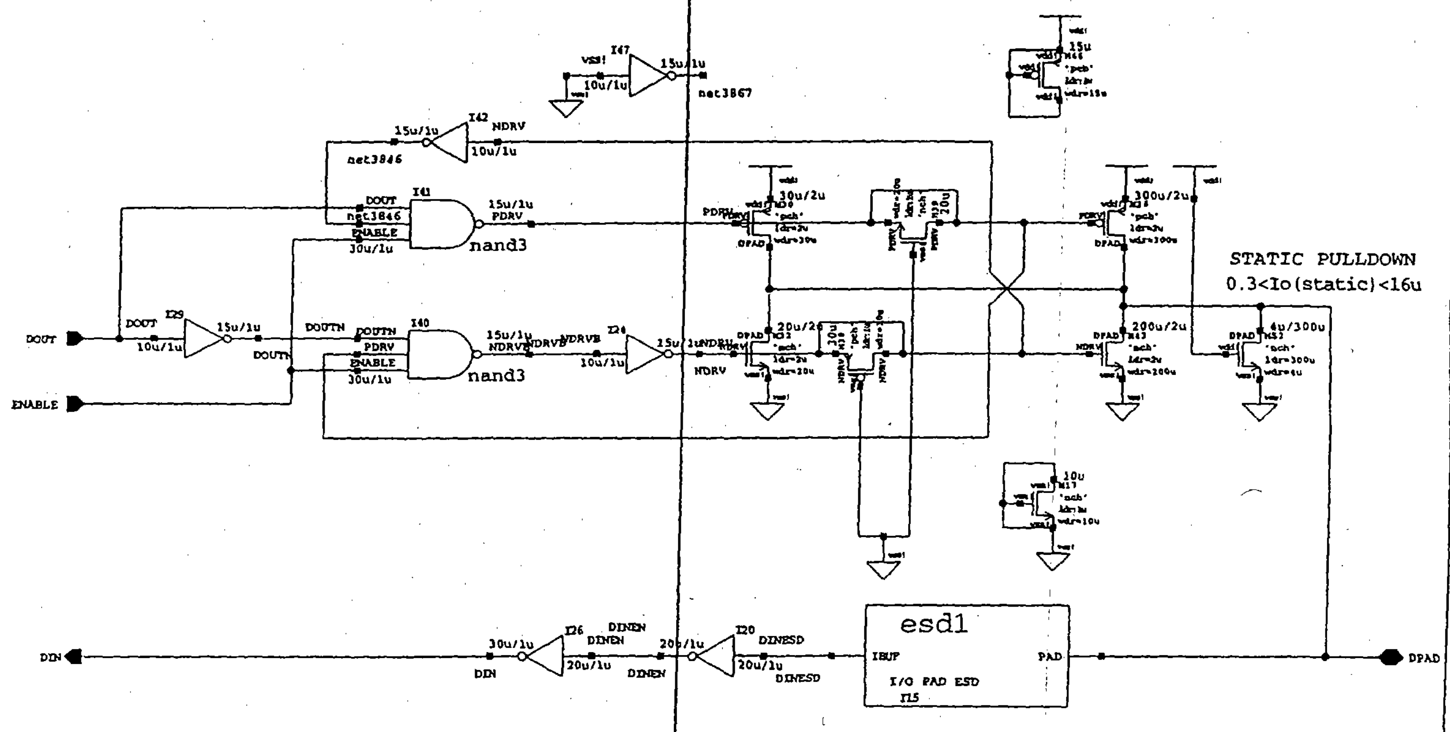


Fig 12

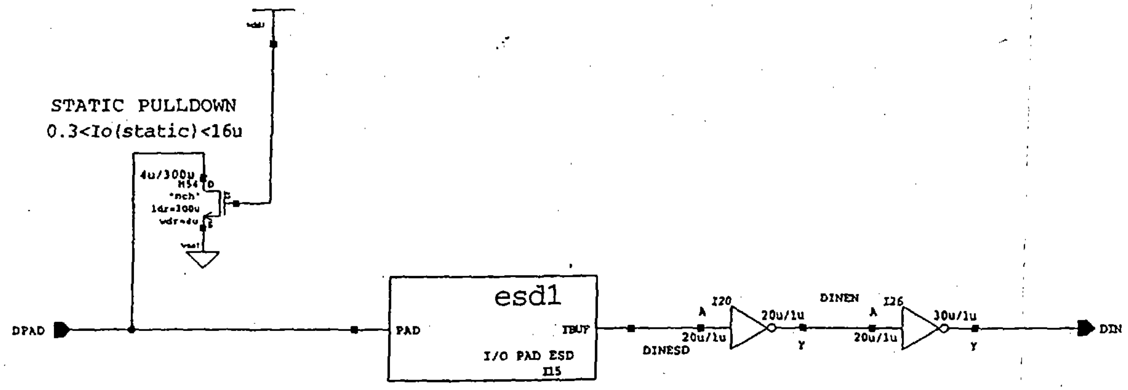


B15: eliminated feedback devices to improve drive to large loads

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: Digital I/O Pad Buffer
NAME: 103reva/paddig
REV: B15
SIZE: A
DATE: Jul 23 15:14:52 1996
SHEET:

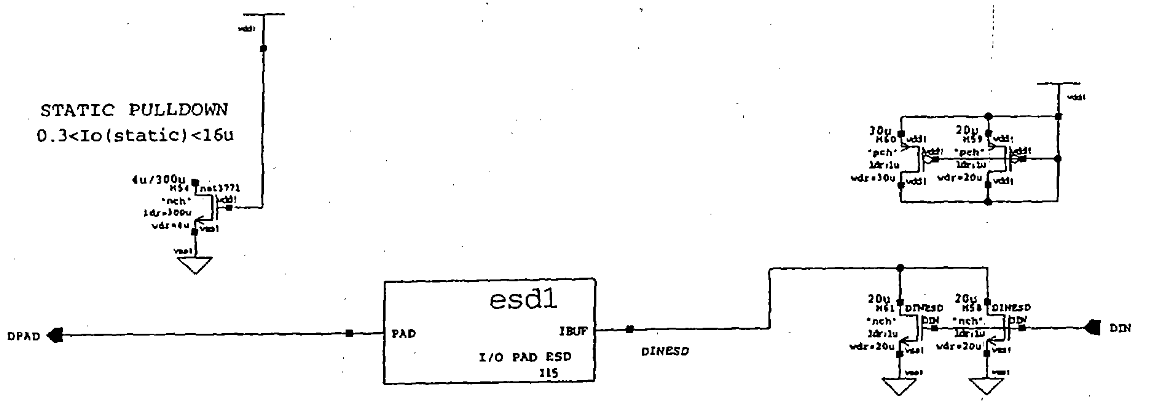
Fig 12AA-AB



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: Digital Input Pad Buffer
NAME: 103reva/paddigin
REV: B1
SIZE: A
DATE: Apr 11 11:10:35 1995
SHEET:

FIG. 13

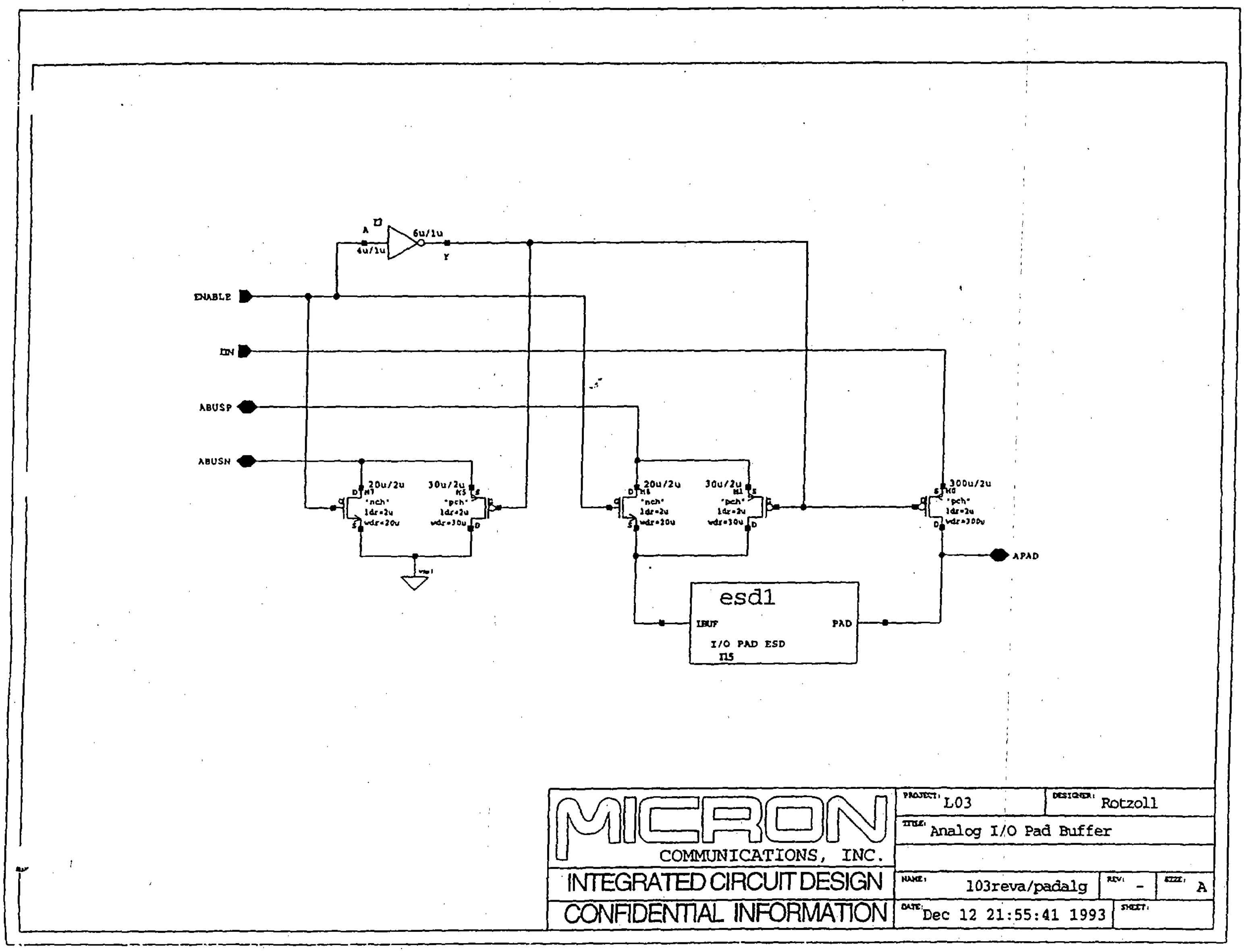


MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: JOTOOLE
TITLE: Digital Input Pad Buffer
NAME: 103reva/paddigin2
REV: B13
SIZE: A
DATE: May 24 18:28:29 1996
SHEET:

B13: new cell for WAKEUP* output

FIG 13.5



I1
A
4u/1u
6u/1u
Y
ENABLE
DIN
ABUSP
ABUSN
20u/2u
M7
D
G
S
"nch"
ldr=2u
wdr=20u
30u/2u
M5
"pch"
ldr=2u
wdr=30u
20u/2u
M6
"nch"
ldr=2u
wdr=20u
30u/2u
M1
"pch"
ldr=2u
wdr=30u
300u/2u
M0
"pch"
ldr=2u
wdr=300u
vss!
APAD
esd1
IBUF
PAD
I/O PAD ESD
I15
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
PROJECT: L03
DESIGNER: Rotzoll
TITLE: Analog I/O Pad Buffer
NAME: 103reva/padalg
REV: -
SIZE: A
DATE: Dec 12 21:55:41 1993
SHEET:

FIG. 14

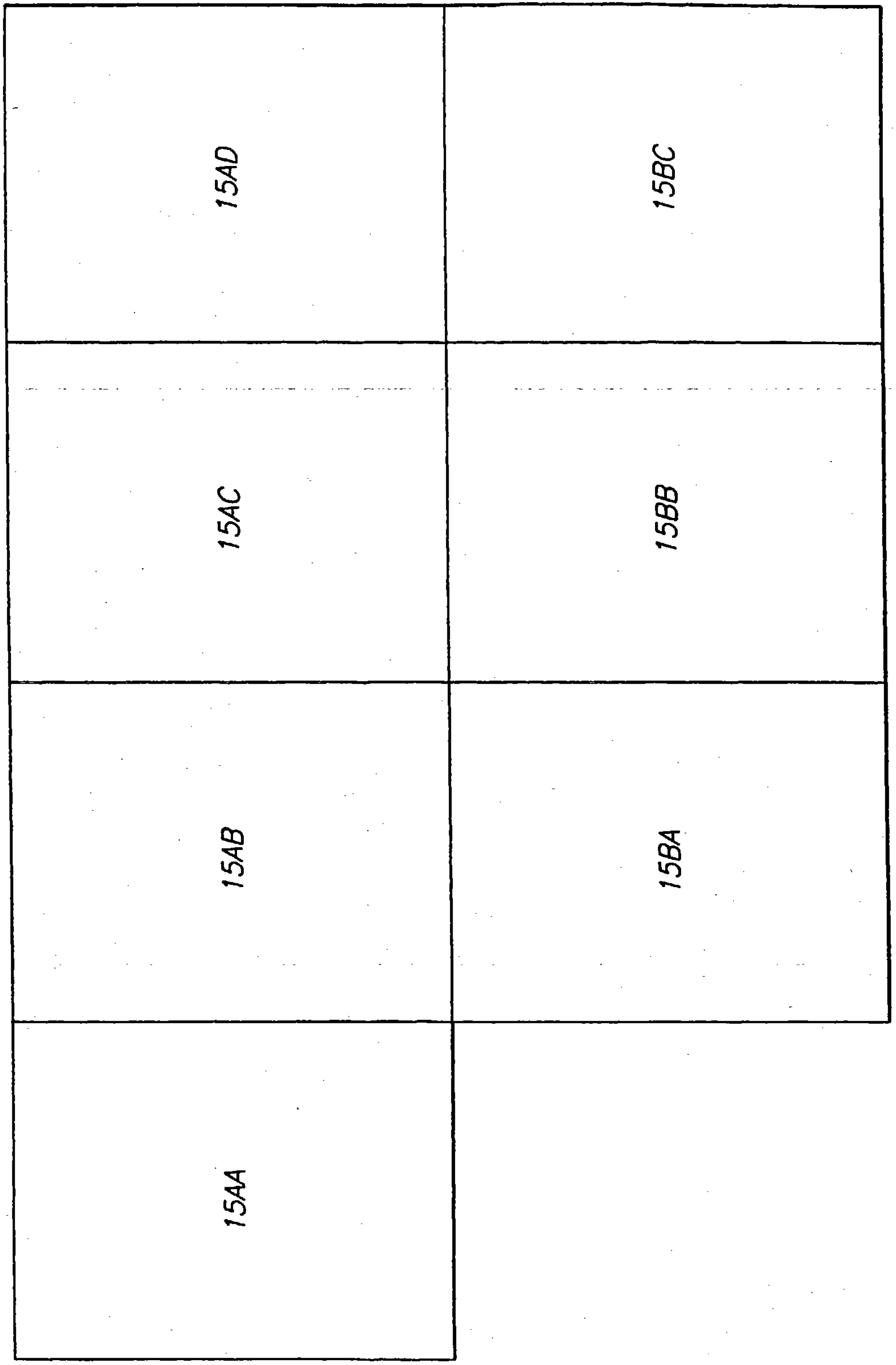


Fig. 15

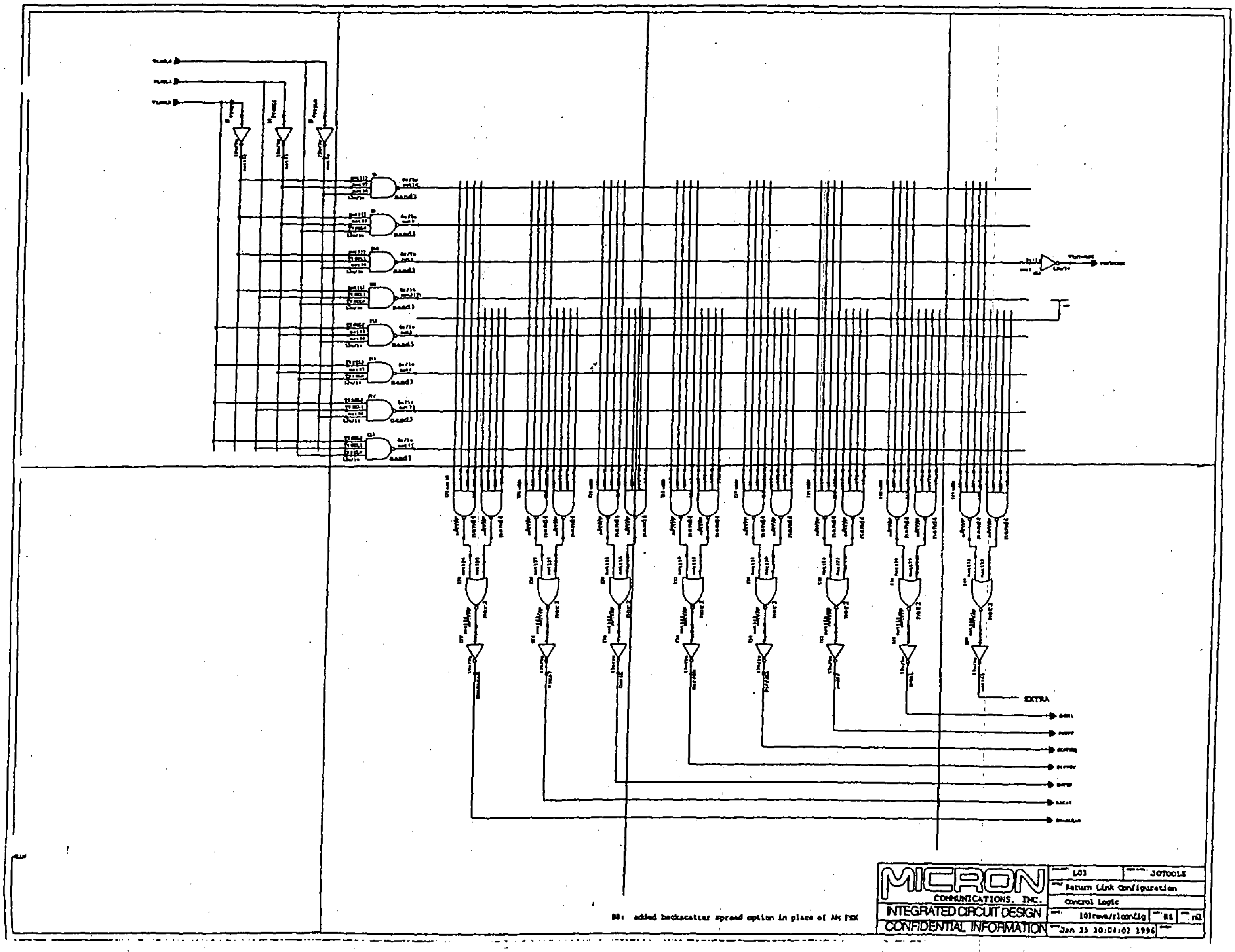

EXTRA
88: added backscatter spread option in place of AM FSK
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
JOTOOLS
Return Link Configuration
Control Logic
101rewa/rlconfig
88
n1
Jan 25 20:04:02 1996

FIG.15

M140-030

Fig 16

16EH	16EG	16EF	16EE	16ED	16EC	16EB	16EA
16DH	16DG	16DF	16DE	16DD	16DC	16DB	16DA
16CH	16CG	16CF	16CE	16CD	16CC	16CB	16CA
16BH	16BG	16BF	16BE	16BD	16BC	16BB	16BA
16AH	16AG	16AF	16AE	16AD	16AC	16AB	16AA

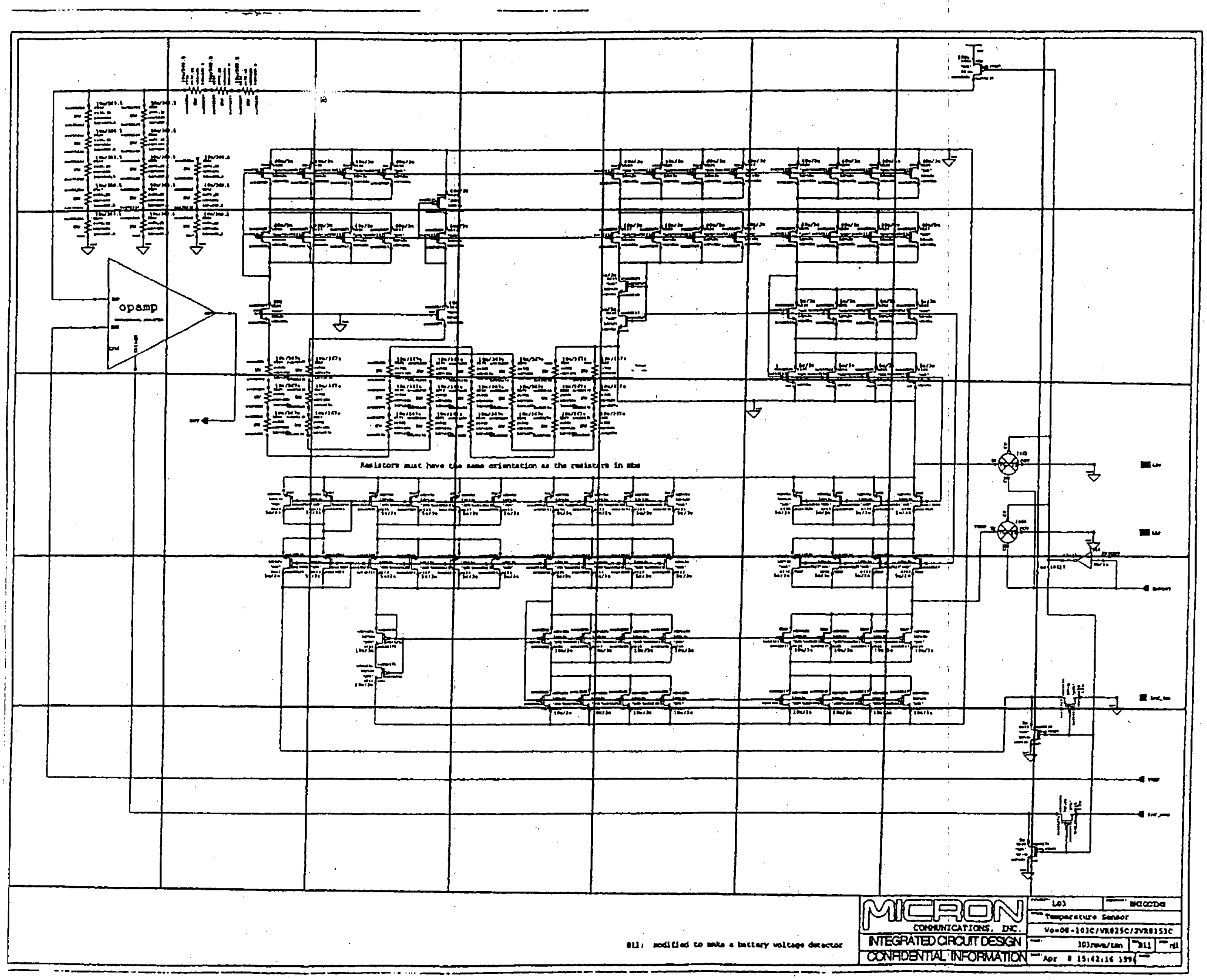

opamp
Resistors must have the same orientation as the resistors in sbs
B11: modified to make a battery voltage detector
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
Temperature Sensor
Vo=08-103C/VR025C/2VR8153C
103rews/tmn
B11
Apr 8 15:42:16 199

FIG. 16

16.01AA	16.01AB	16.01AC	16.01AD	16.01AE	16.01AF	16.01AG		
16.01BA	16.01BB	16.01BC	16.01BD	16.01BE	16.01BF	16.01BG	16.01BH	16.01BI
16.01CA	16.01CB	16.01CC	16.01CD	16.01CE	16.01CF	16.01CG	16.01CH	16.01CI
16.01DA	16.01DB	16.01DC	16.01DD	16.01DE	16.01DF	16.01DG	16.01DH	16.01DI

Fig 16.01

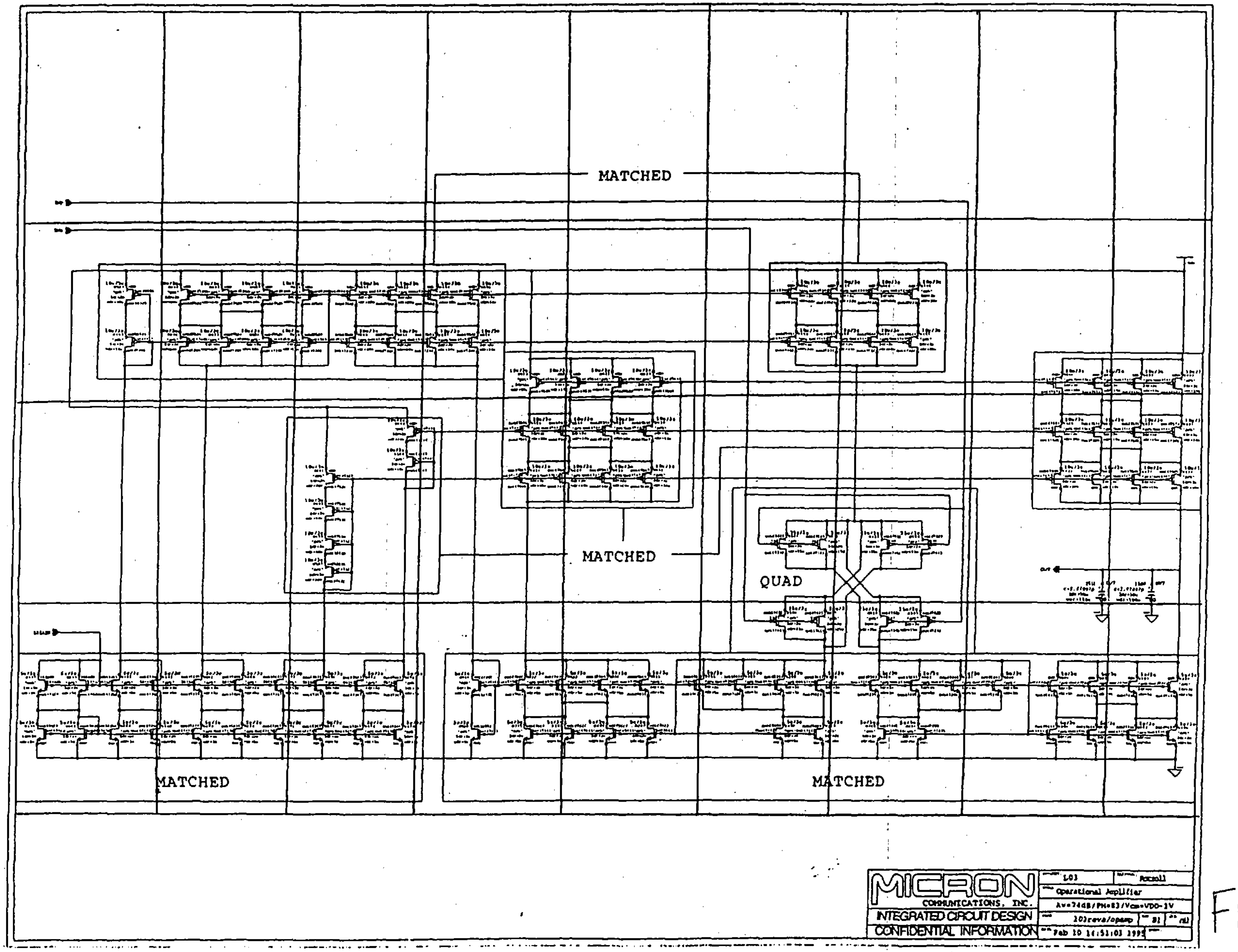

MATCHED
MATCHED
QUAD
out
MATCHED
MATCHED
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION
L03
Operational Amplifier
Av=74dB/PM=83/Vcm=VDD-1V
103reva/opamp
81
Feb 10 14:51:03 1995

FIG.16.01

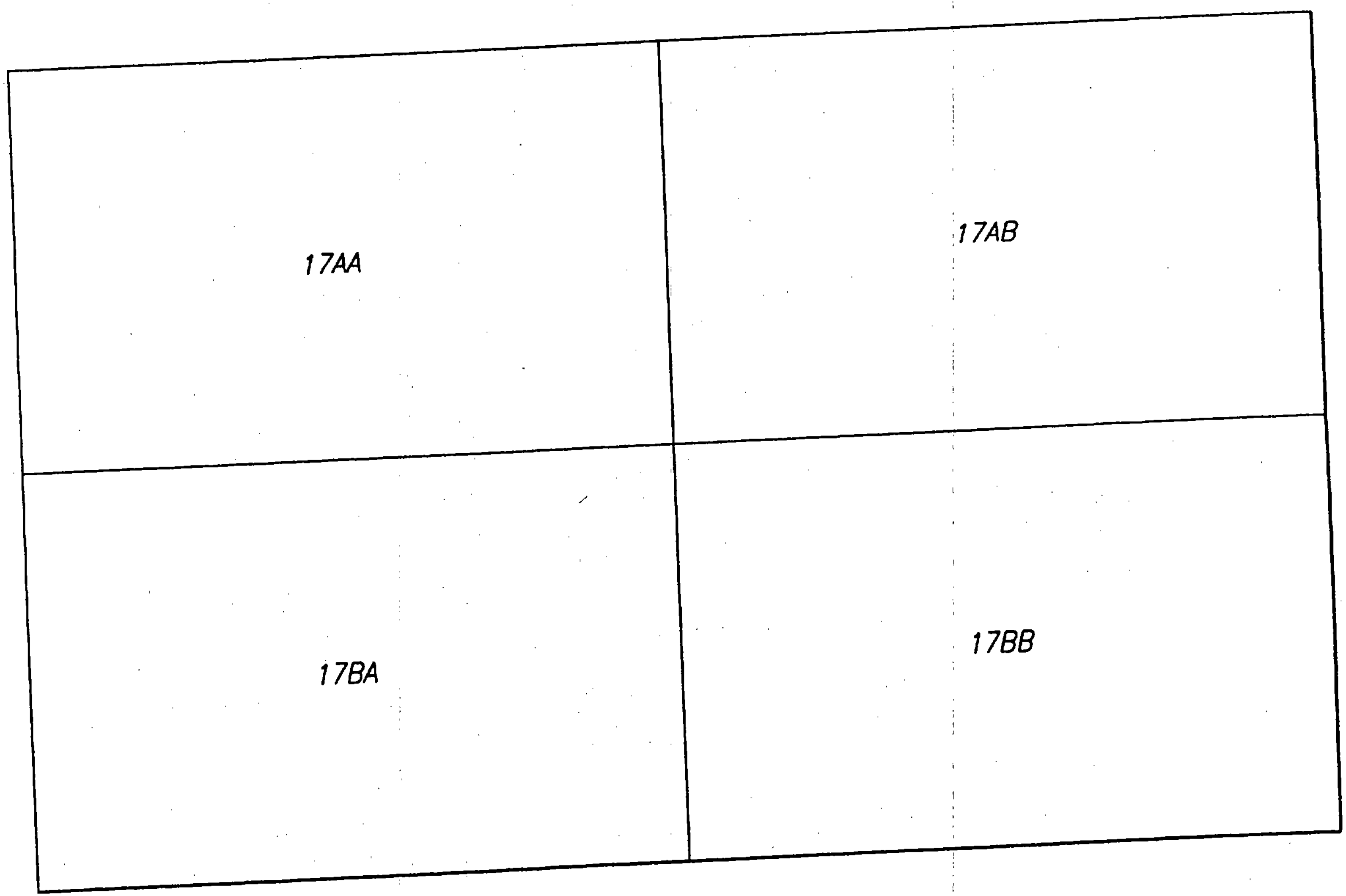


FIG 17

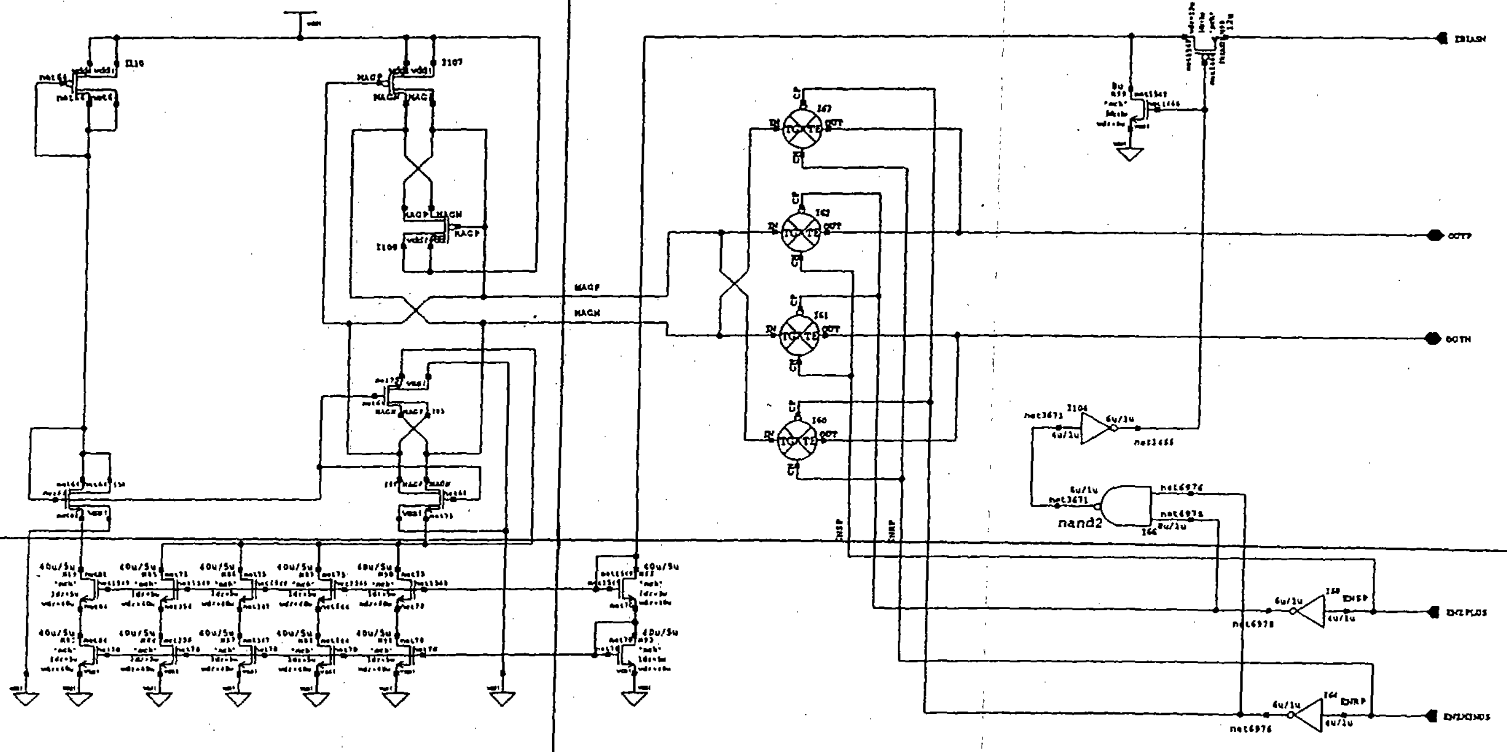


FIG. 17

B8: fixed control logic

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03		DESIGNER: Rotzoll	
TITLE: Magnetic Field Sensor			
NAME: 103reva/mag	REV: B8	SIZE: nl	
DATE: Jan 9 08:58:38 1996		SHEET:	

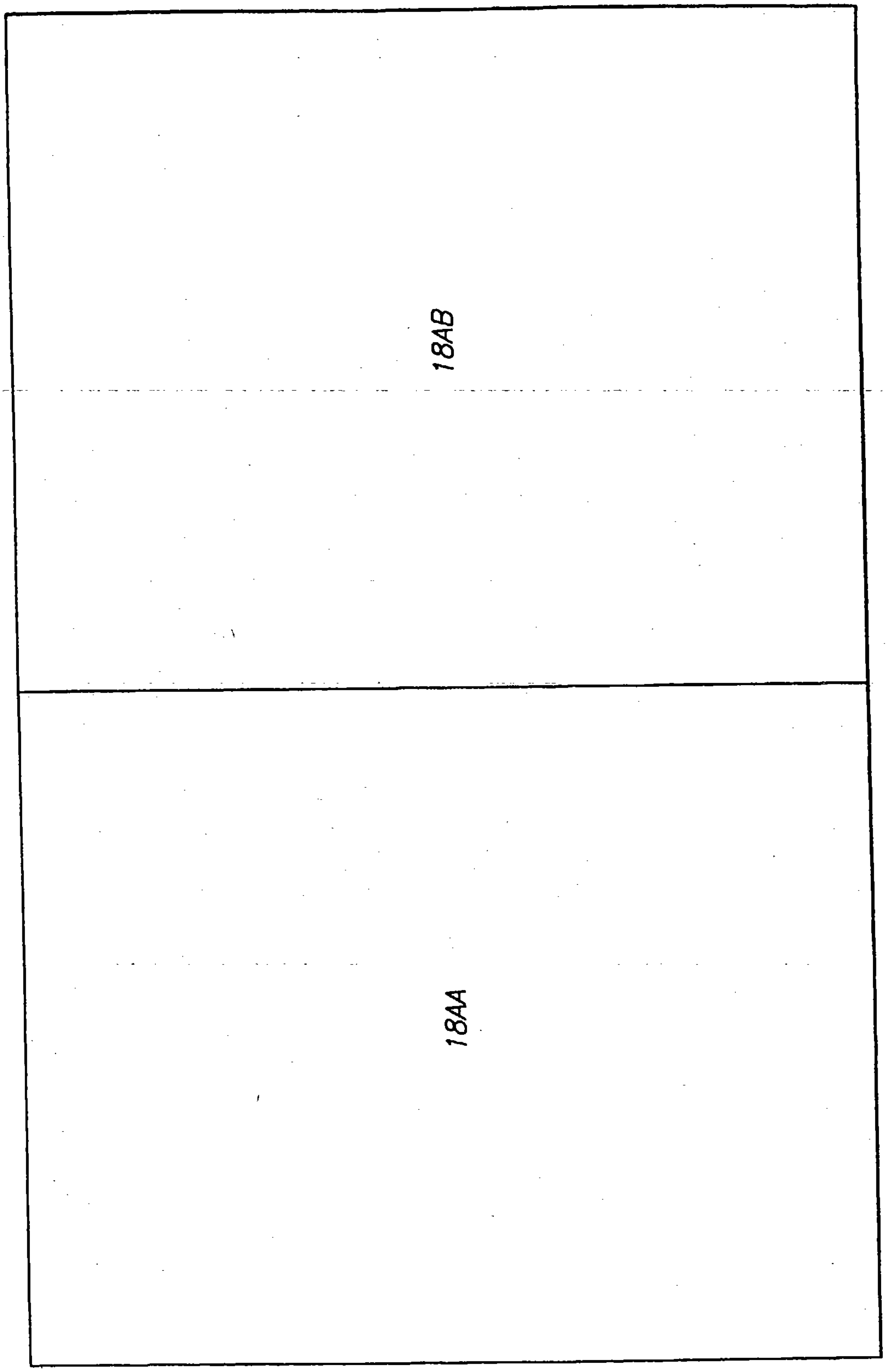


FIG. 18

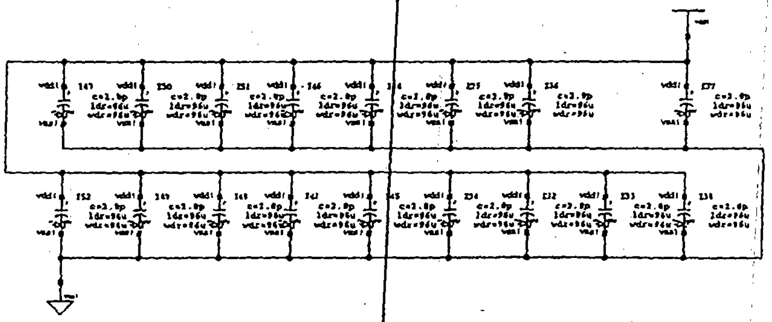


FIG. 18

B2: deleted one cap

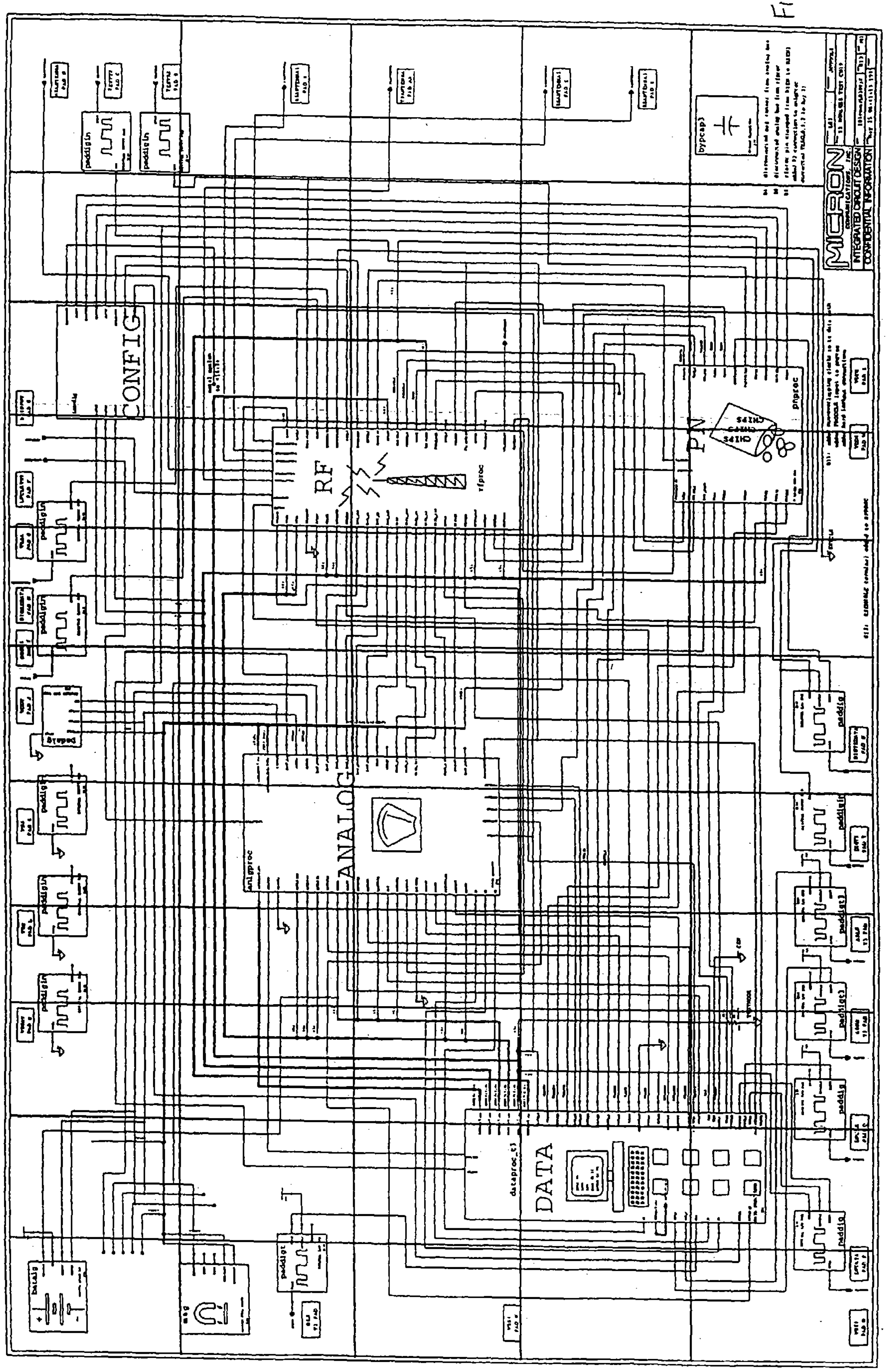
MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Chip Bypass Capacitor Ct=pF	
NAME: 103reva/bypcap3	REV: B2
DATE: Jul 28 17:43:25 1995	SHEET:

19AA	19AB	19AC	19AD	19AE	19AF	19AG	19AH	19AI	19AJ	19AK
19BA	19BB	19BC	19BD	19BE	19BF	19BG	19BH	19BI	19BJ	19BK
19CA	19CB	19CC	19CD	19CE	19CF	19CG	19CH	19CI	19CJ	19CK
19DA	19DB	19DC	19DD	19DE	19DF	19DG	19DH	19DI	19DJ	19DK
19EA	19EB	19EC	19ED	19EE	19EF	19EG	19EH	19EI	19EJ	19EK

Fig 19

F16. 19.AA-EK



CONFIG
RF
rfproc
PN
pnproc
CHIPS
ANALOG
anlgproc
DATA
dataproc_t3
paddigin
paddig
paddigt
paddigt3
bypcap
bypcap3
batalg
mag
MICRON COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

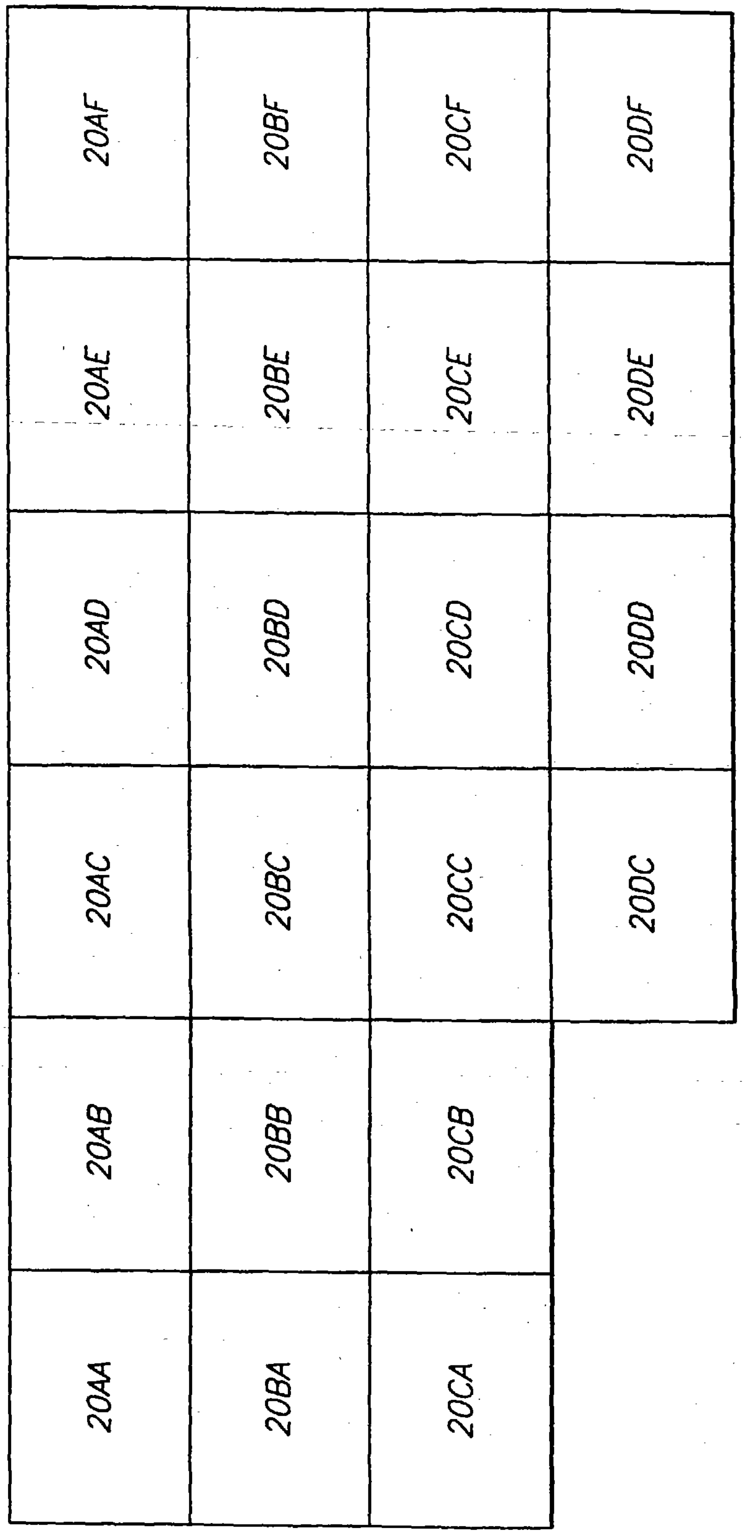
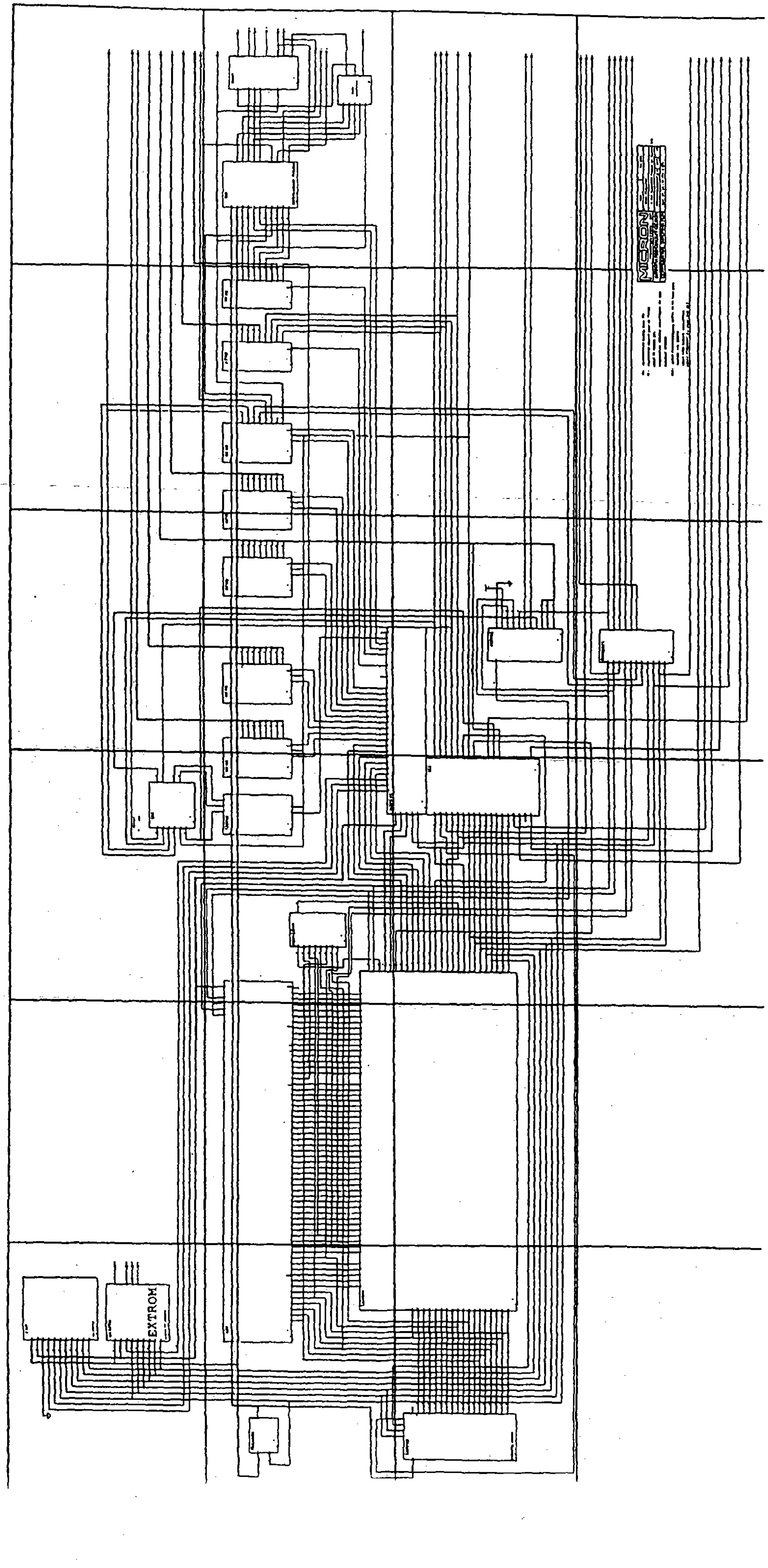

20AF
20BF
20CF
20DF
20AE
20BE
20CE
20DE
20AD
20BD
20CD
20DD
20AC
20BC
20CC
20DC
20AB
20BB
20CB
20AA
20BA
20CA

Fig 20

Fig. 20



20.01AA	20.01AB
20.01BA	20.01BB
20.01CA	20.01CB

Fig 20.01

Feb 11 11:24:23 1994

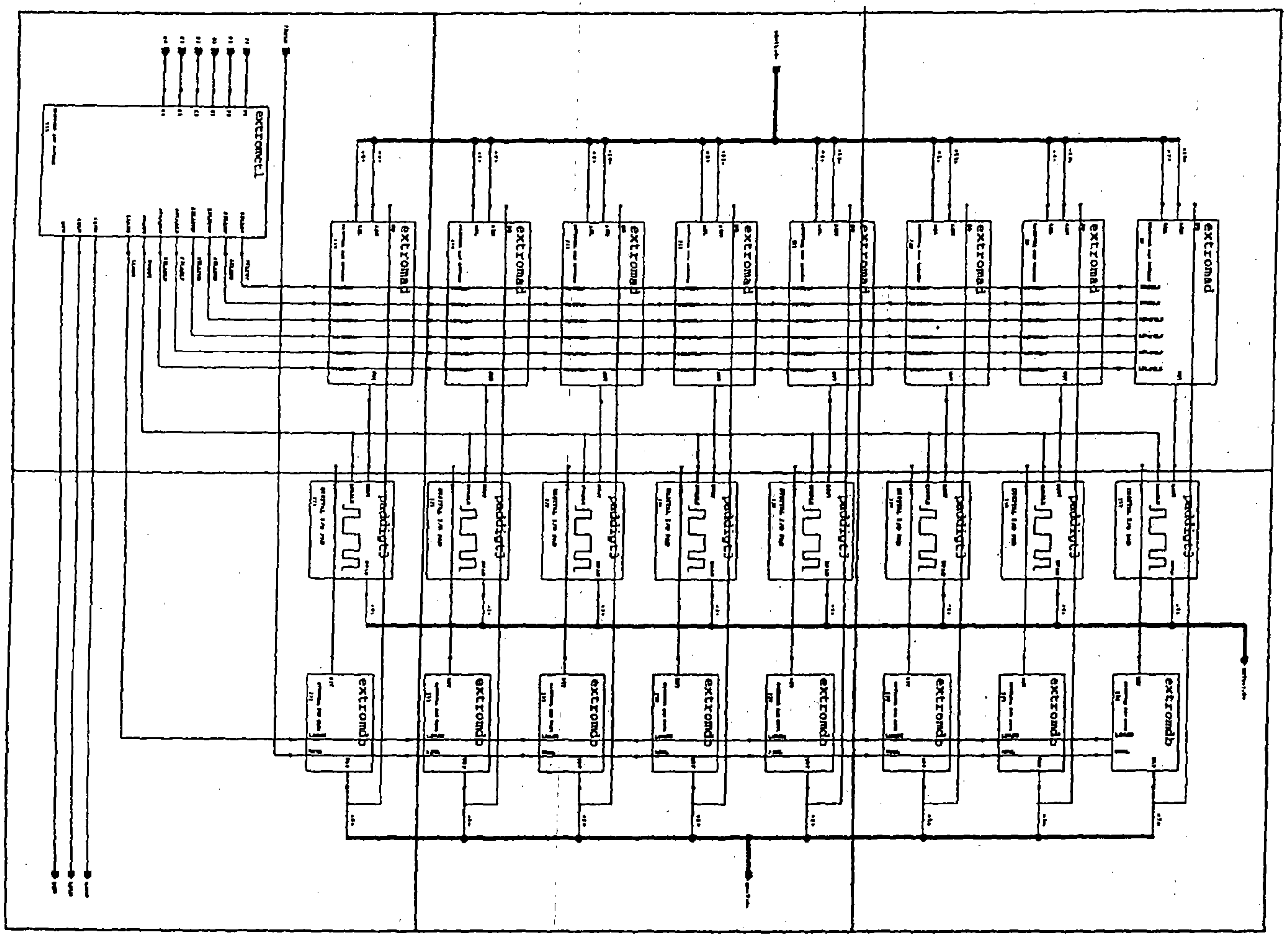
101revs/extrom

CONFIDENTIAL INFORMATION

INTEGRATED CIRCUIT DESIGN

MICRON COMMUNICATIONS, INC.

FIG. 20,01



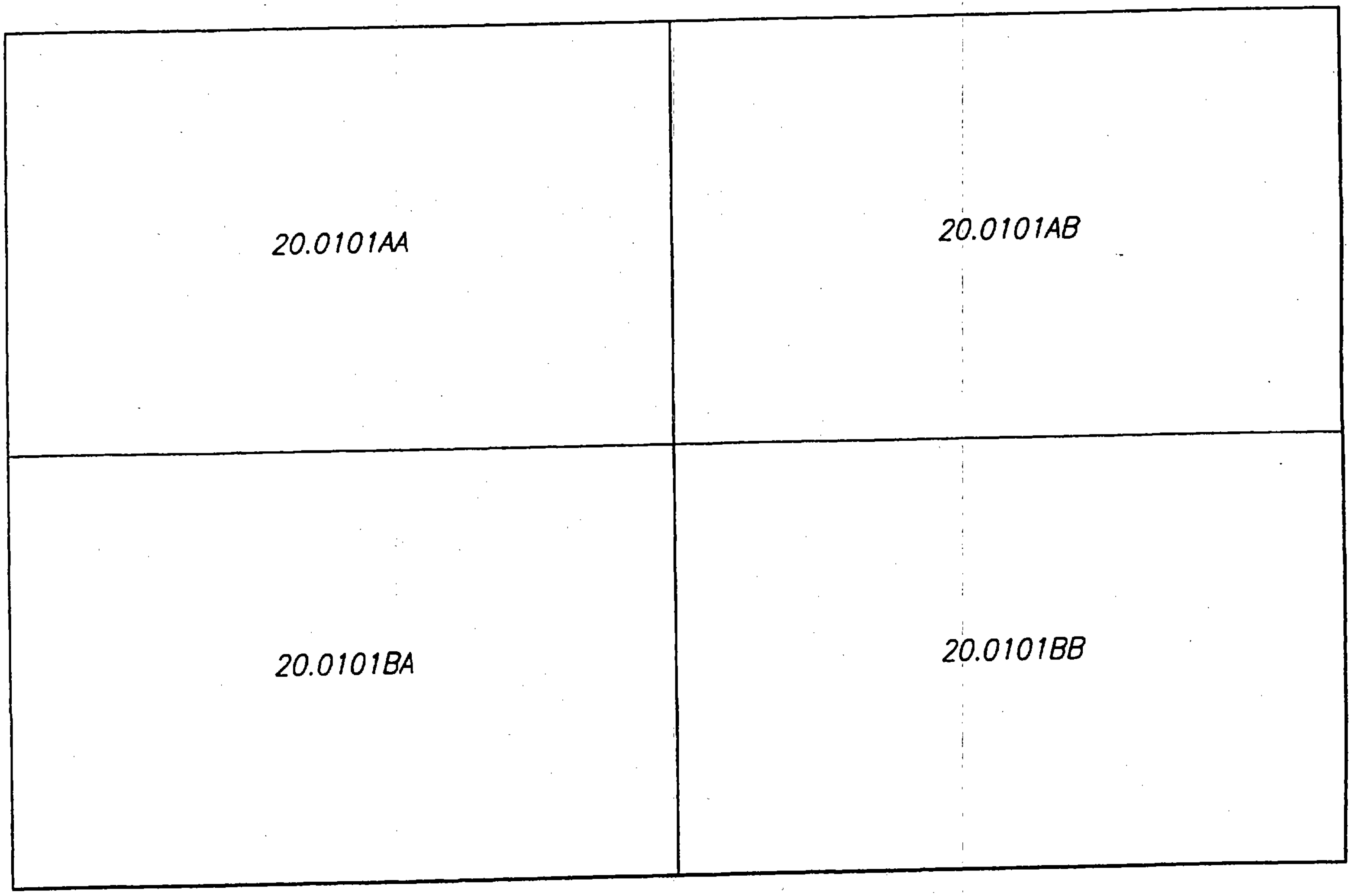


Fig 20.0101

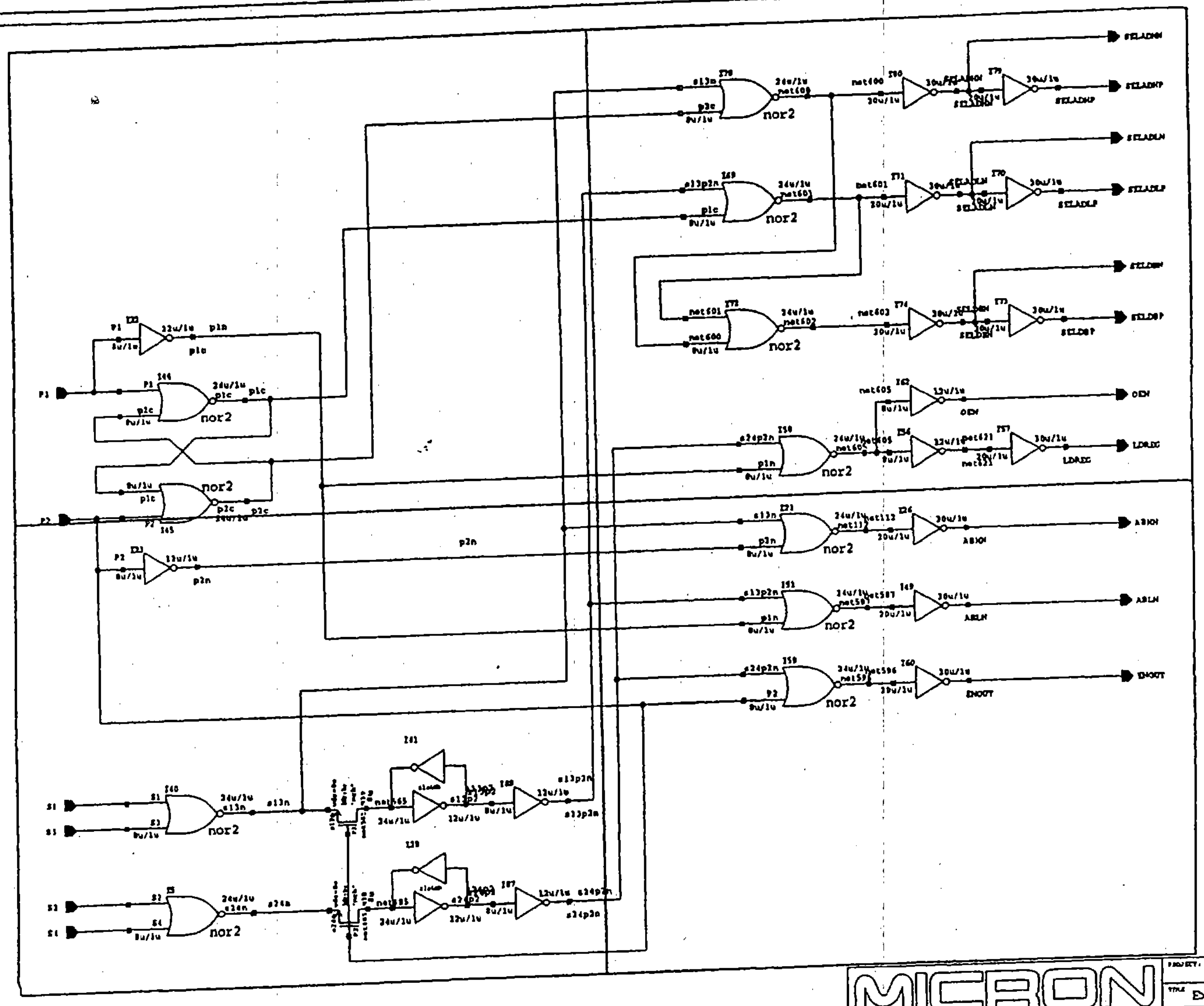
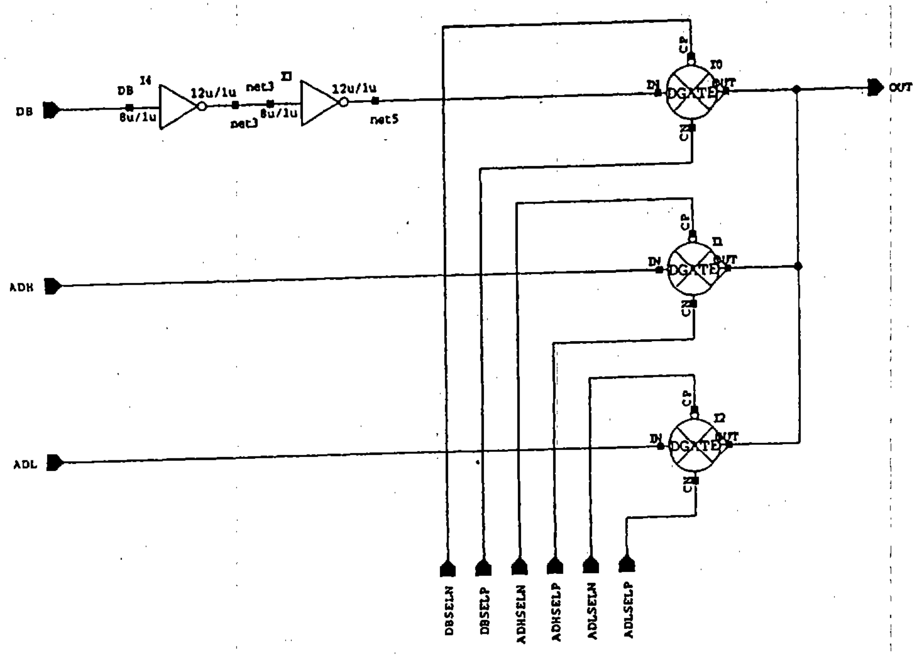


FIG. 20.0101

MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: External ROM Control Logic
NAME: 103reva/extromctl
REV: -
SIZE: nil
DATE: Dec 11 21:56:41 1993
SHEET:



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: External ROM Address Interface
NAME: 103reva/extromad
REV: -
SIZE: A
DATE: Dec 11 01:09:14 1993
SHEET:

FIG. 20.0102

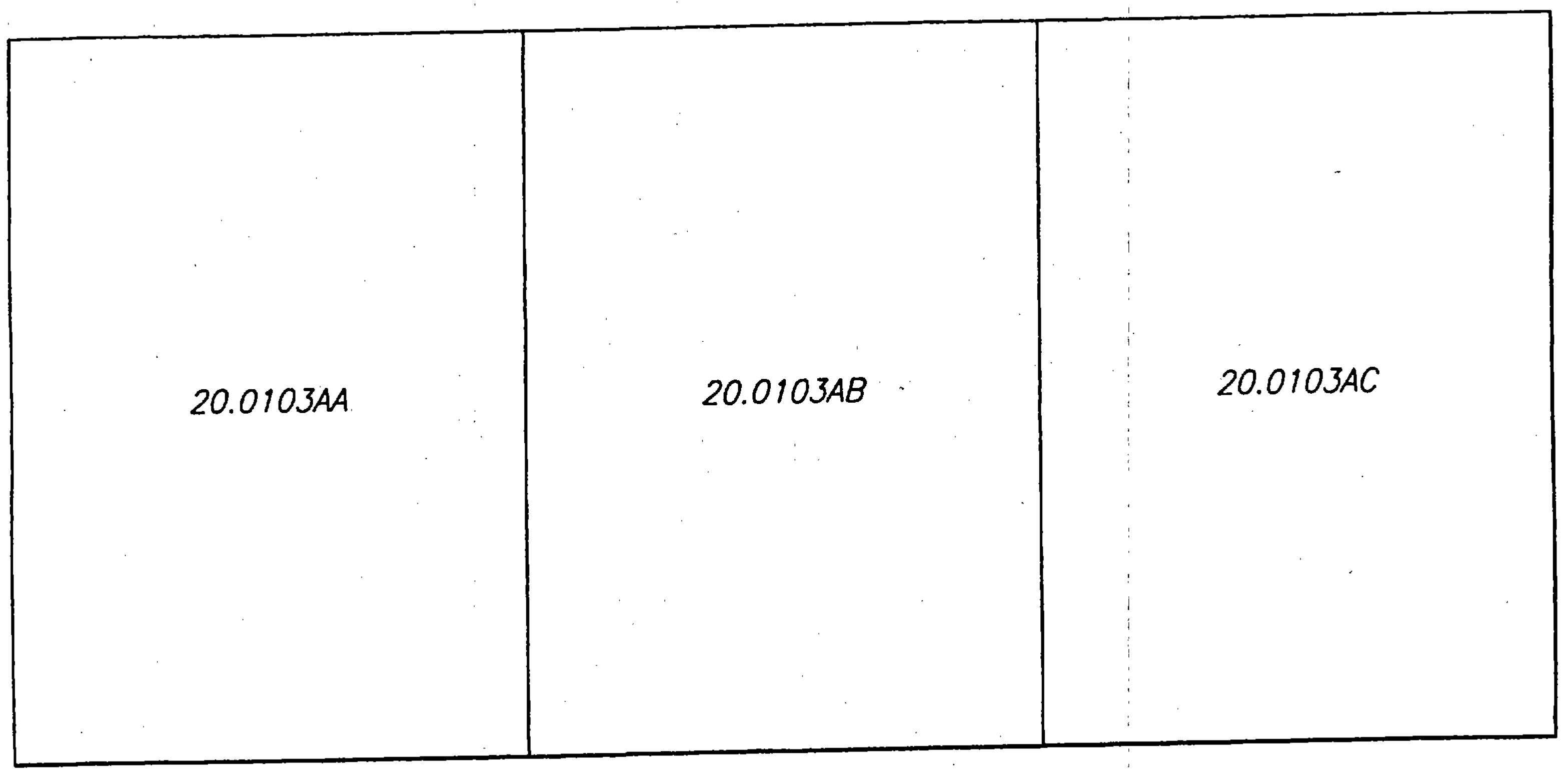
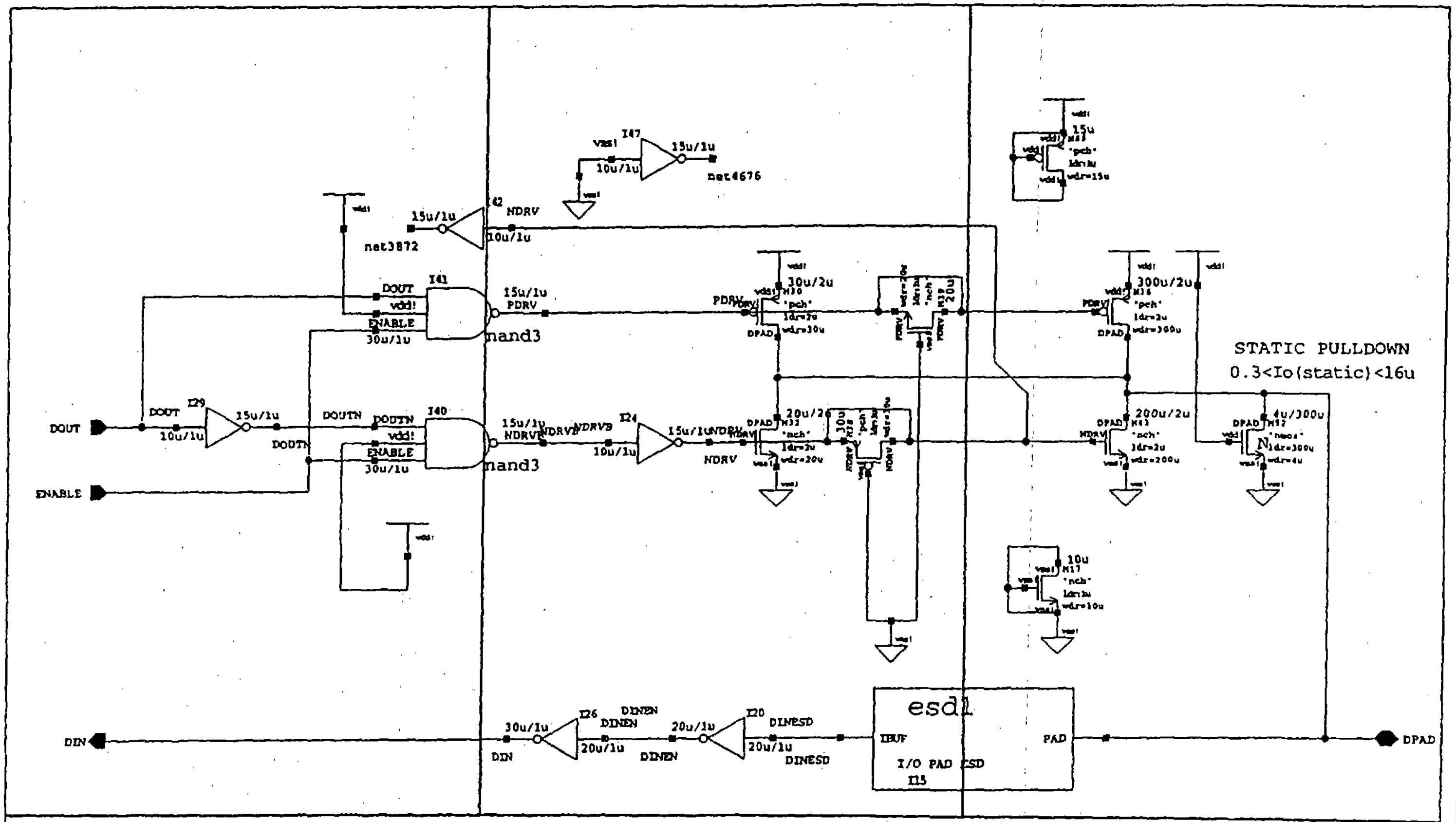


Fig 20.0103



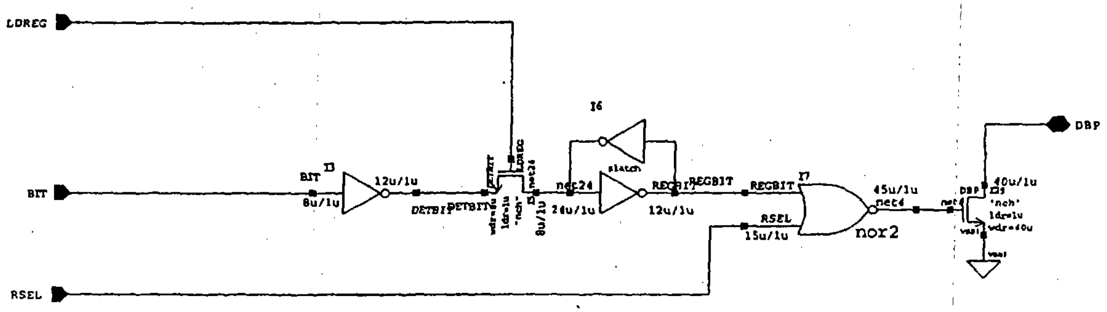
MICRON COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Digital I/O Pad Buffer	
T3 MOD	
NAME: 103reva/paddigt3	REV: B15 SIZE: A
DATE: Jul 23 15:13:39 1996	SHEET:

Fig 20.0103AA-AC



MICRON
COMMUNICATIONS, INC.
INTEGRATED CIRCUIT DESIGN
CONFIDENTIAL INFORMATION

PROJECT: L03
DESIGNER: Rotzoll
TITLE: External ROM Databus Interface
NAME: 103reva/extromdb
REV: -
SIZE: A
DATE: Dec 11 01:01:13 1993
SHEET:

Fig. 20.0104

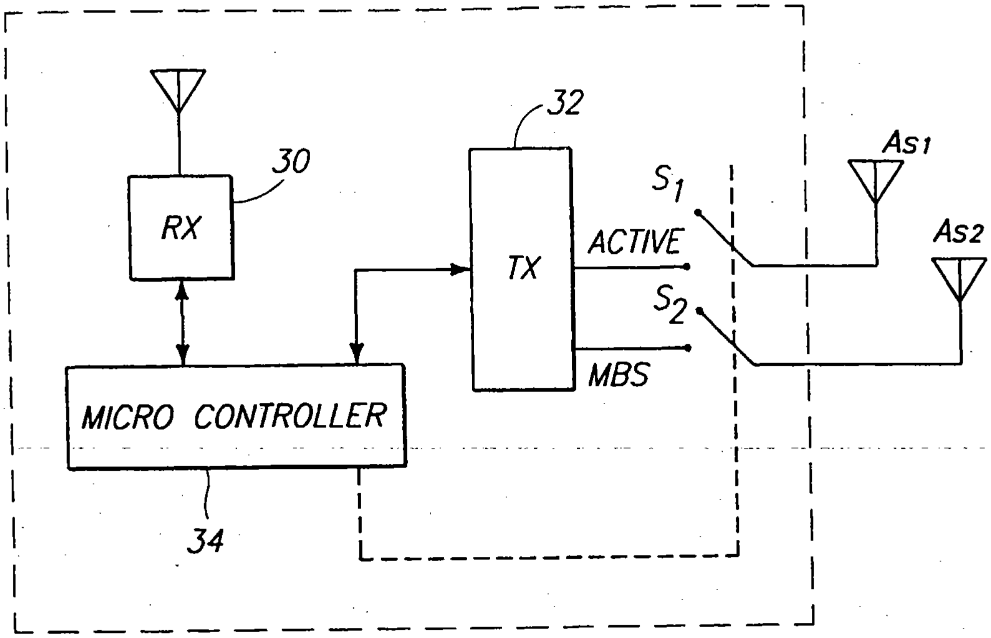

30
RX
MICRO CONTROLLER
34
32
TX
ACTIVE
MBS
S1
S2
As1
As2

Fig 21

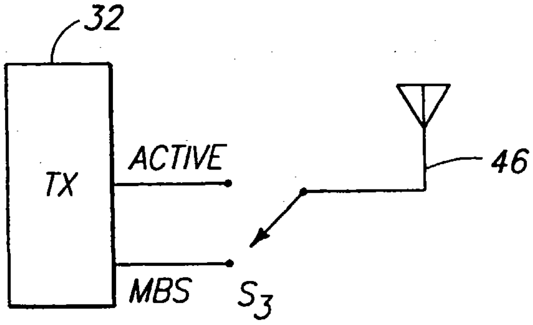
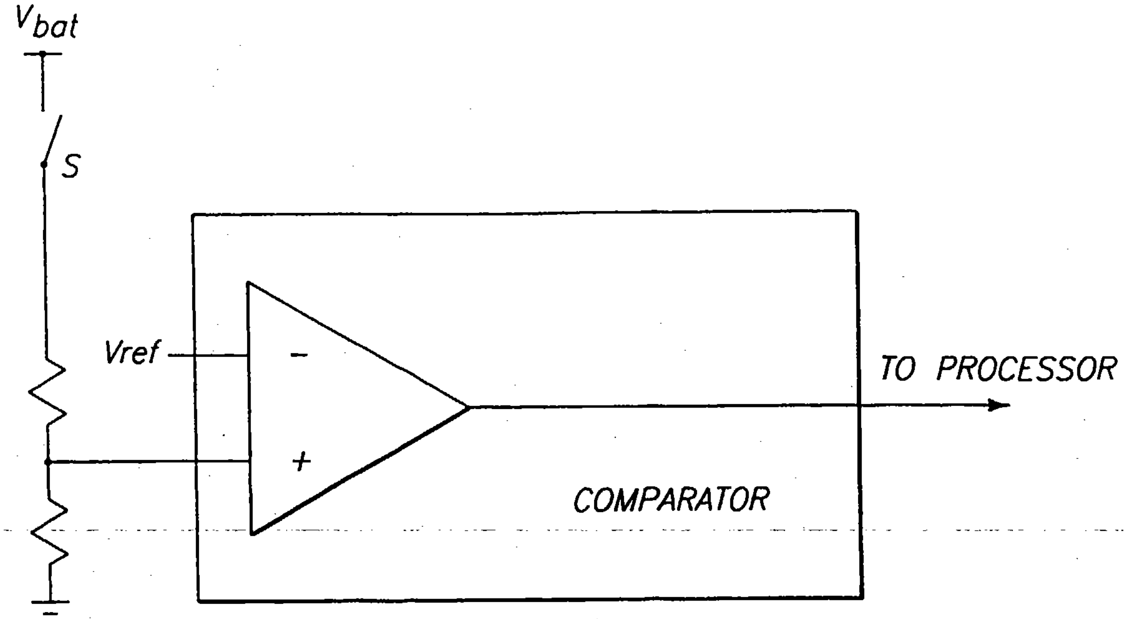

32
TX
ACTIVE
MBS
S3
46

Fig 22



V_{ref} = bandgap voltage ≈ 1.2 V for silicon

Fig 23

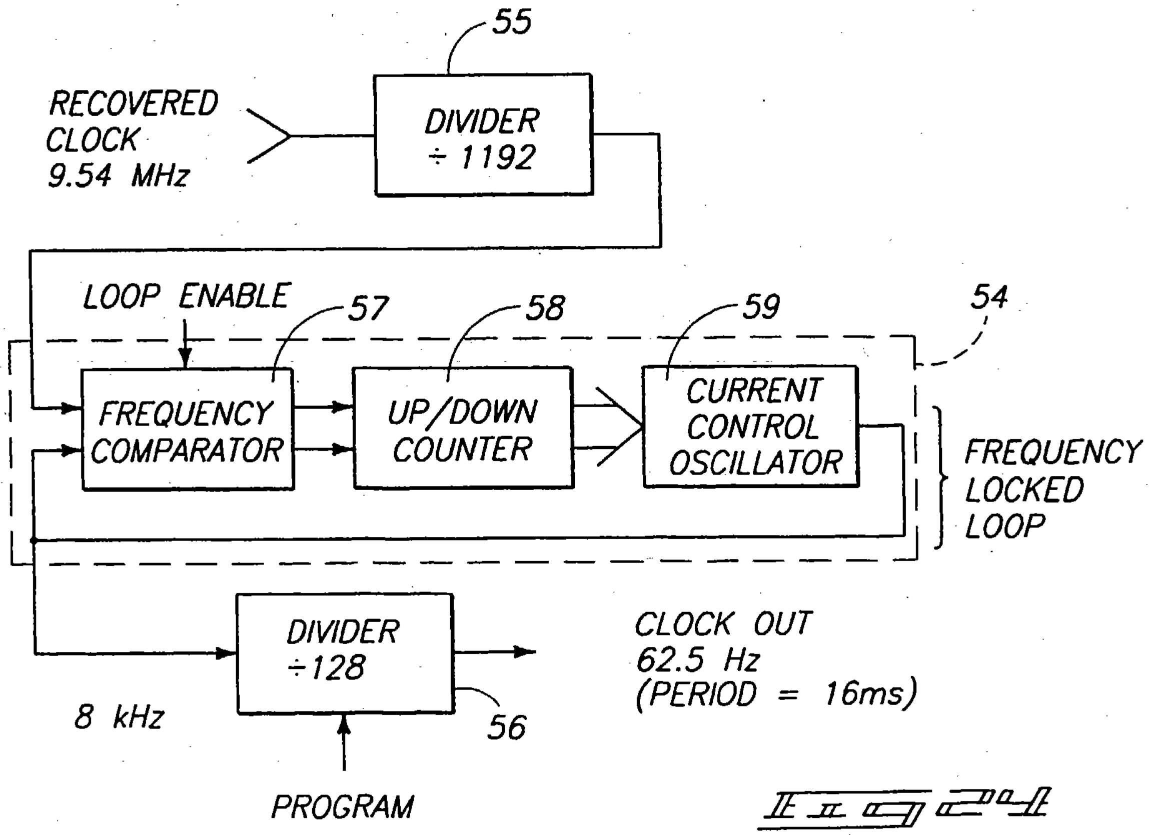


Fig 24

WAKEUP SEQUENCE

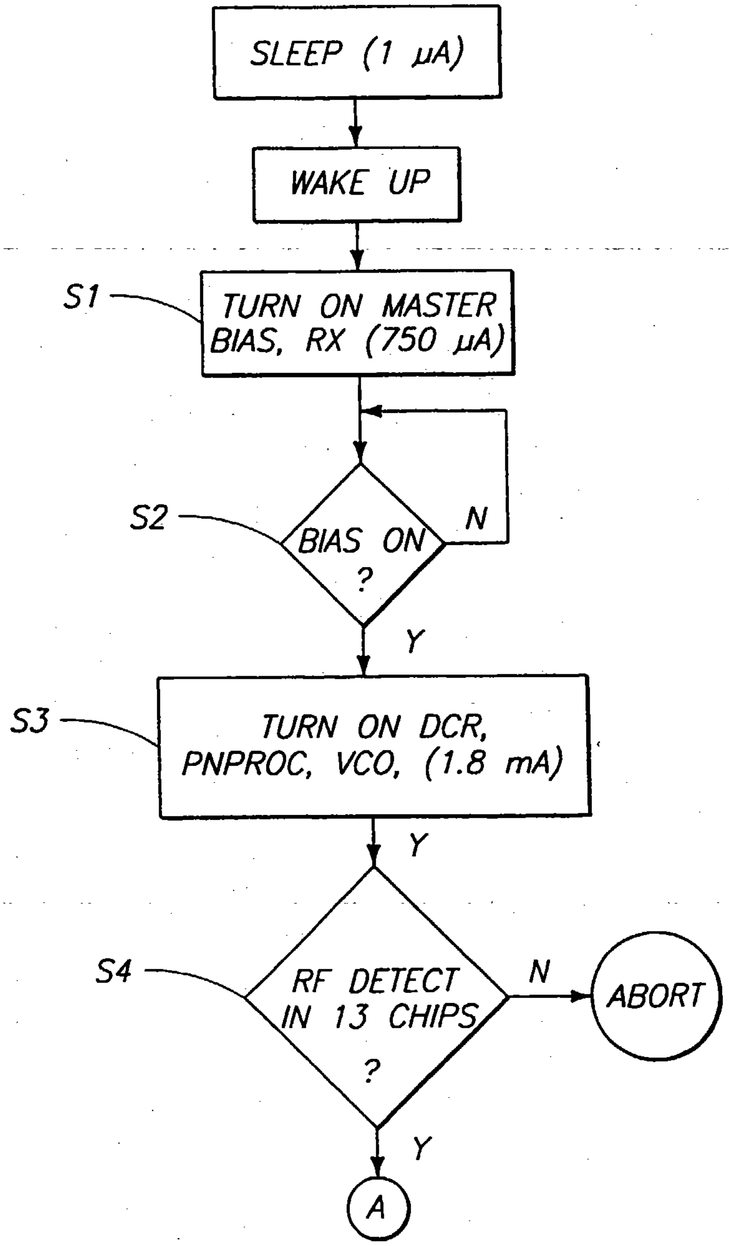


Fig 25

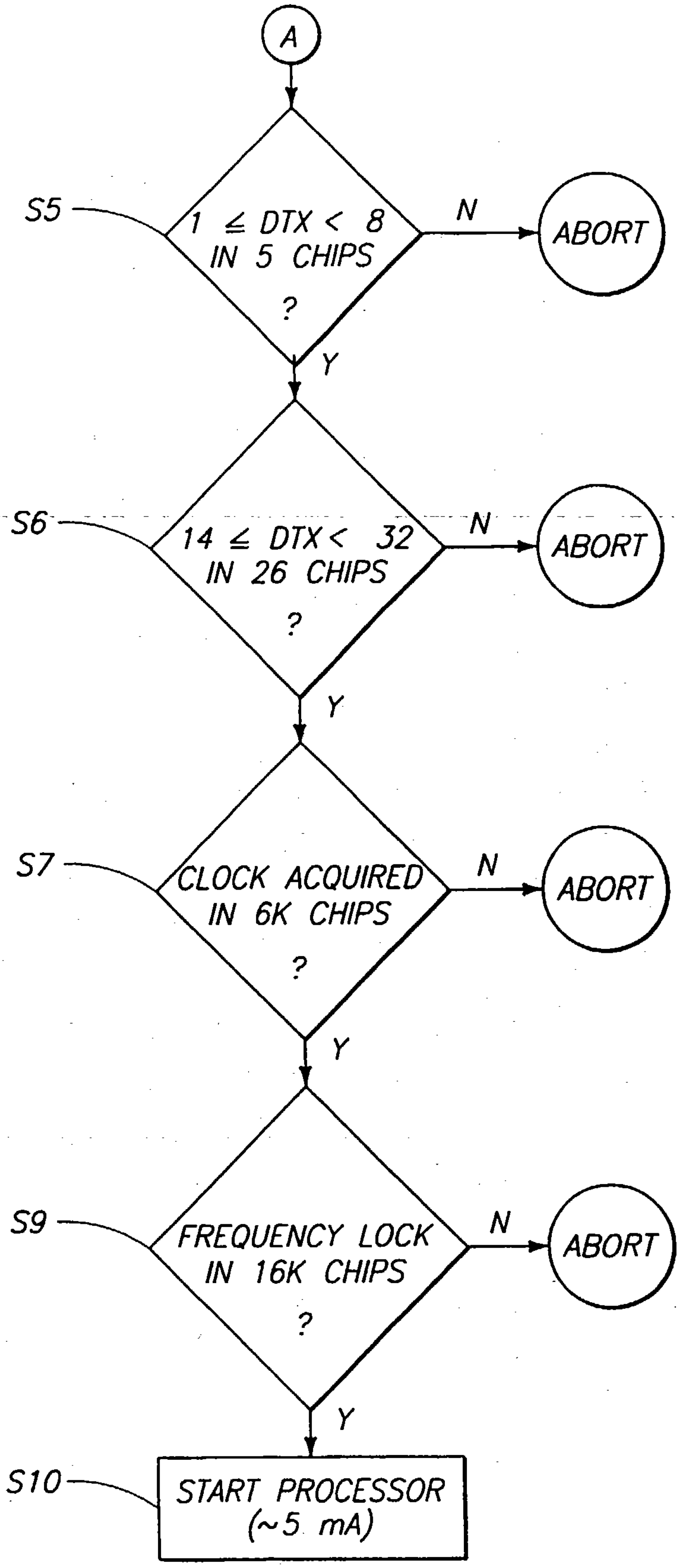

A
S5
1 ≦ DTX < 8
IN 5 CHIPS
?
N
ABORT
Y
S6
14 ≦ DTX < 32
IN 26 CHIPS
?
N
ABORT
Y
S7
CLOCK ACQUIRED
IN 6K CHIPS
?
N
ABORT
Y
S9
FREQUENCY LOCK
IN 16K CHIPS
?
N
ABORT
Y
S10
START PROCESSOR
(~5 mA)

Fig 26

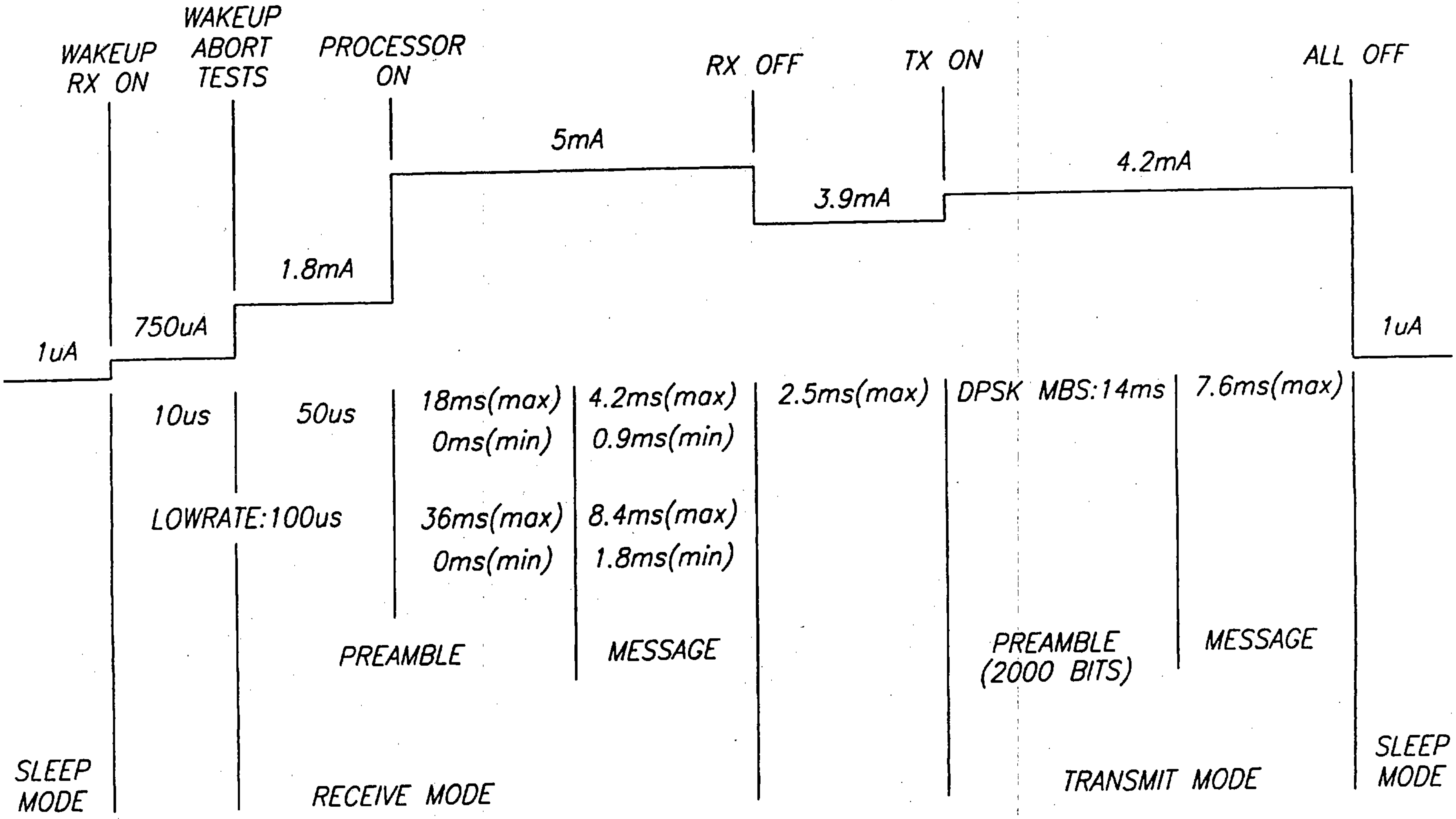

WAKEUP RX ON
WAKEUP ABORT TESTS
PROCESSOR ON
RX OFF
TX ON
ALL OFF
1uA
750uA
1.8mA
5mA
3.9mA
4.2mA
1uA
10us
50us
18ms(max)
0ms(min)
4.2ms(max)
0.9ms(min)
2.5ms(max)
DPSK MBS:14ms
7.6ms(max)
LOWRATE:100us
36ms(max)
0ms(min)
8.4ms(max)
1.8ms(min)
PREAMBLE
MESSAGE
PREAMBLE (2000 BITS)
MESSAGE
SLEEP MODE
RECEIVE MODE
TRANSMIT MODE
SLEEP MODE

FIG 27

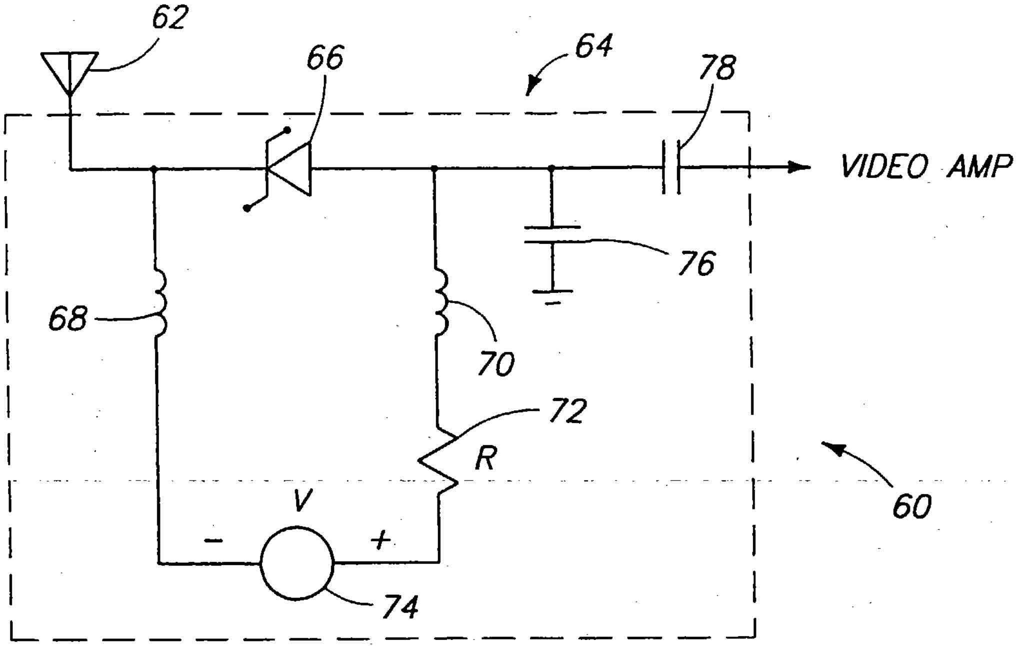

62
64
66
78
VIDEO AMP
76
68
70
72
R
V
−
+
74
60

Fig 28

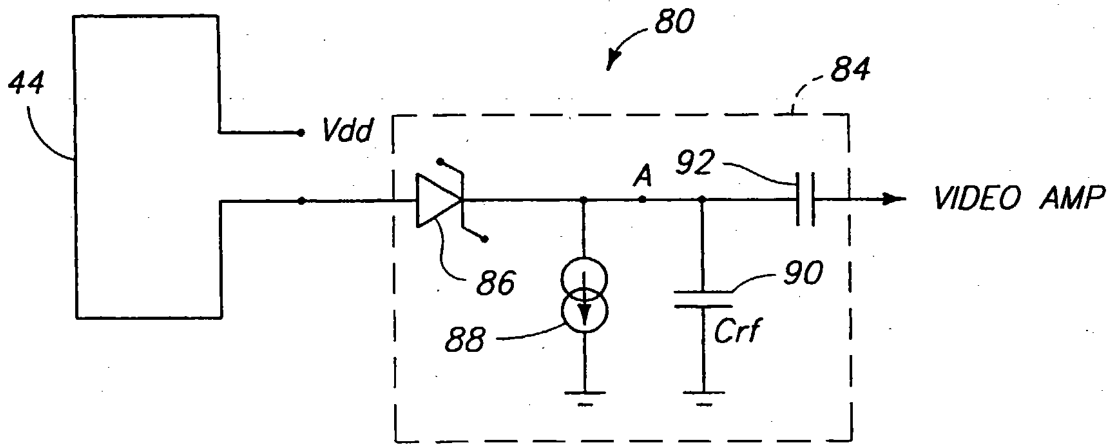

80
84
44
Vdd
A
92
VIDEO AMP
86
90
88
Crf

Fig 29

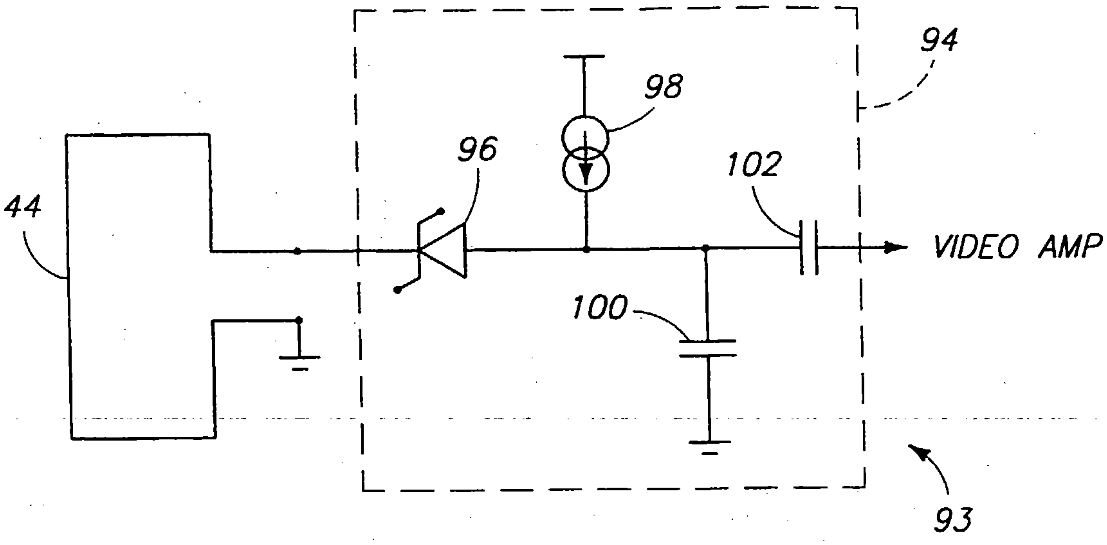

94
98
96
102
44
VIDEO AMP
100
93

Fig 30

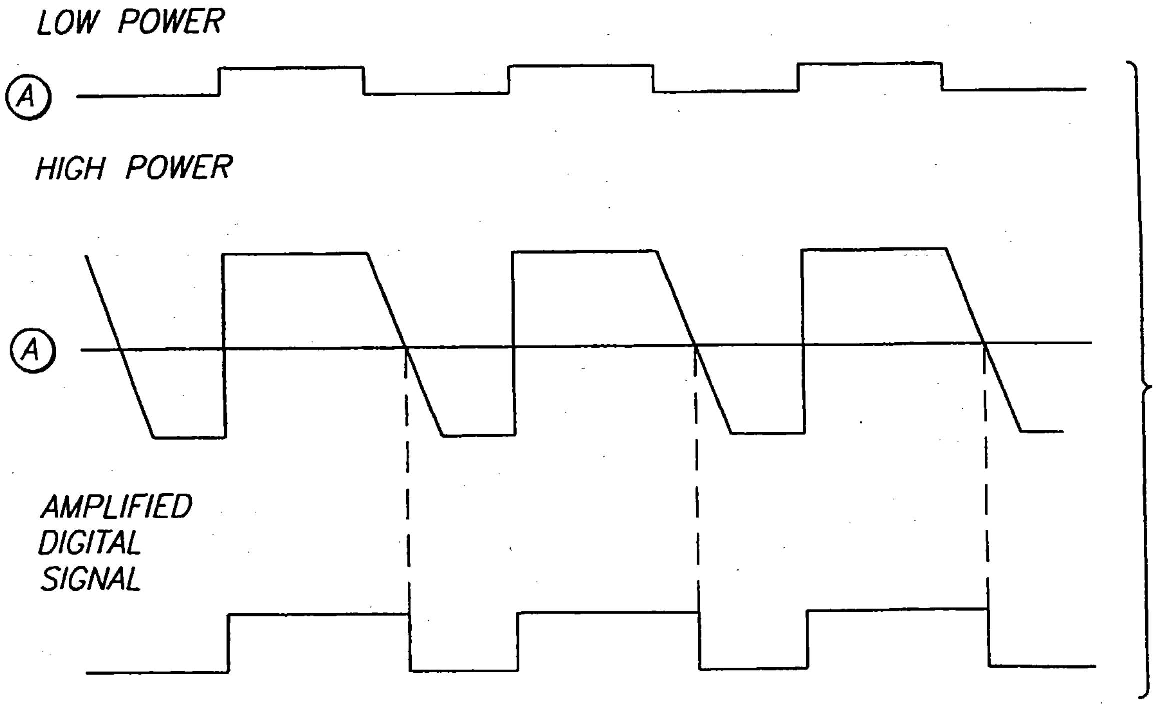

LOW POWER
A
HIGH POWER
A
AMPLIFIED
DIGITAL
SIGNAL

Fig 31

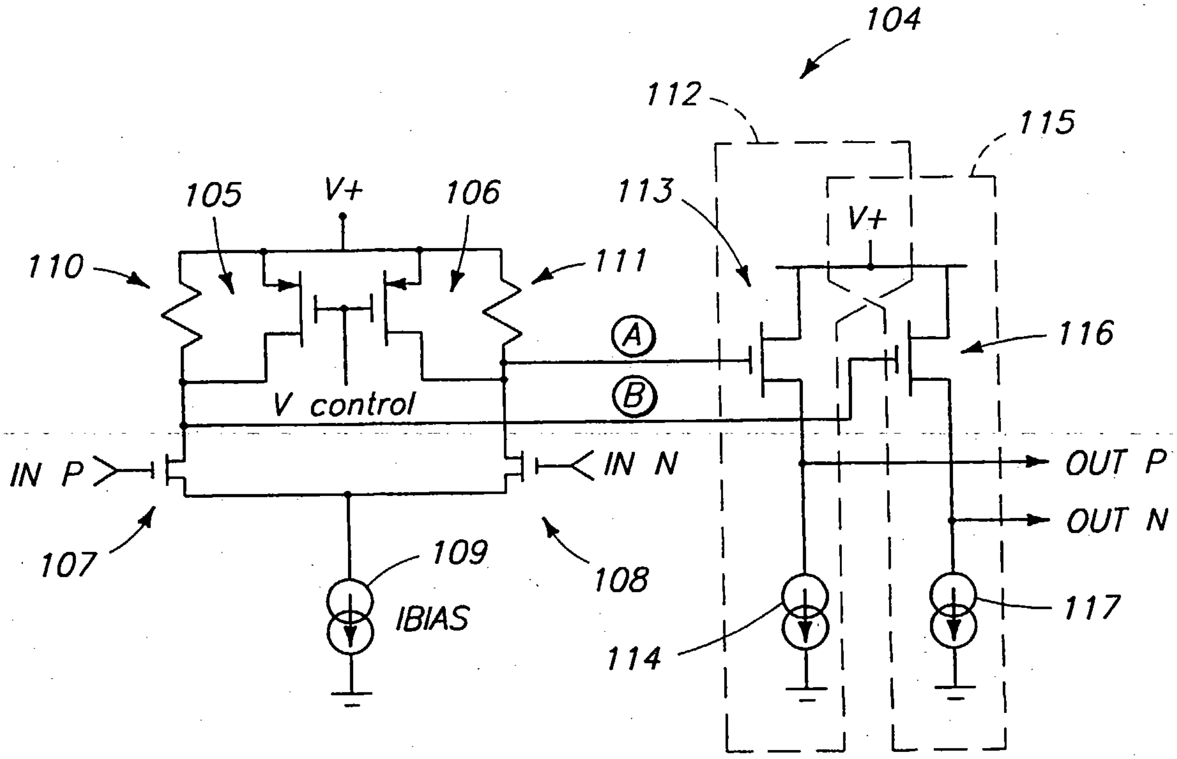

104
112
115
105
V+
106
110
111
113
V+
116
A
B
V control
IN P
IN N
OUT P
OUT N
107
109
IBIAS
108
114
117

Fig 32

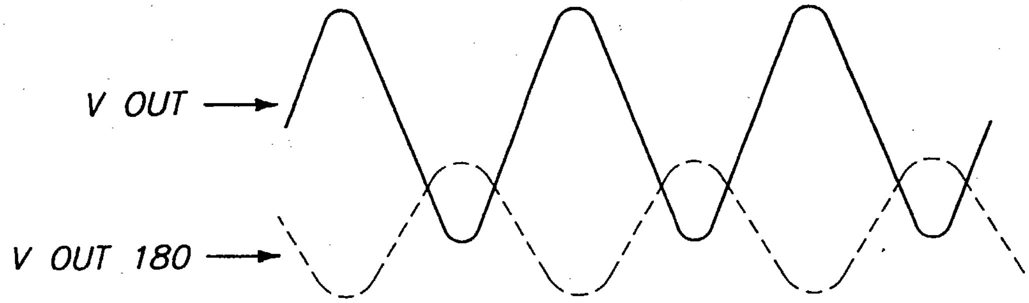

V OUT
V OUT 180

Fig 33

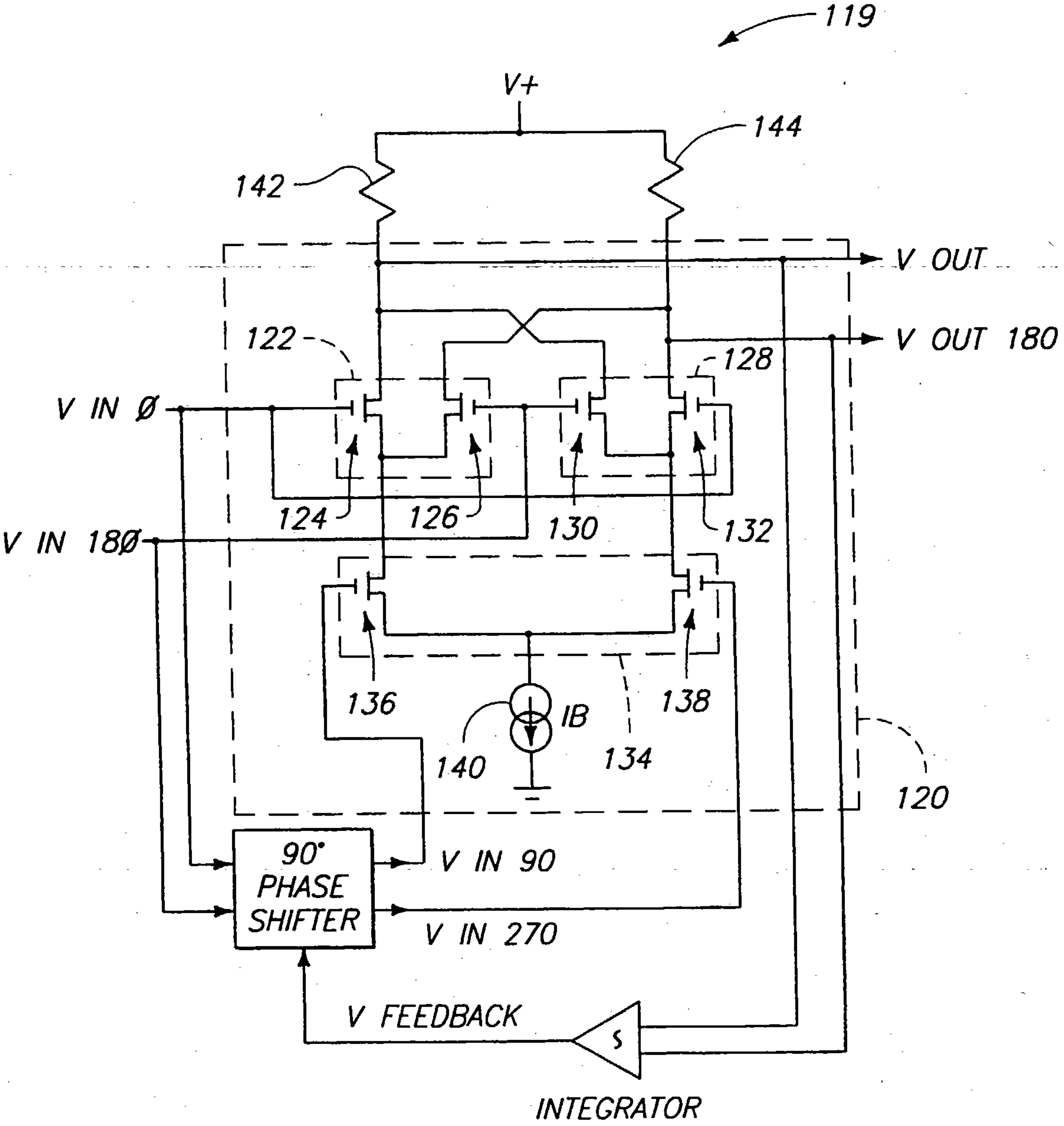

119
V+
142
144
V OUT
V OUT 180
122
128
V IN Ø
124
126
130
132
V IN 18Ø
136
138
IB
140
134
120
90° PHASE SHIFTER
V IN 90
V IN 270
V FEEDBACK
S
INTEGRATOR

Fig 34

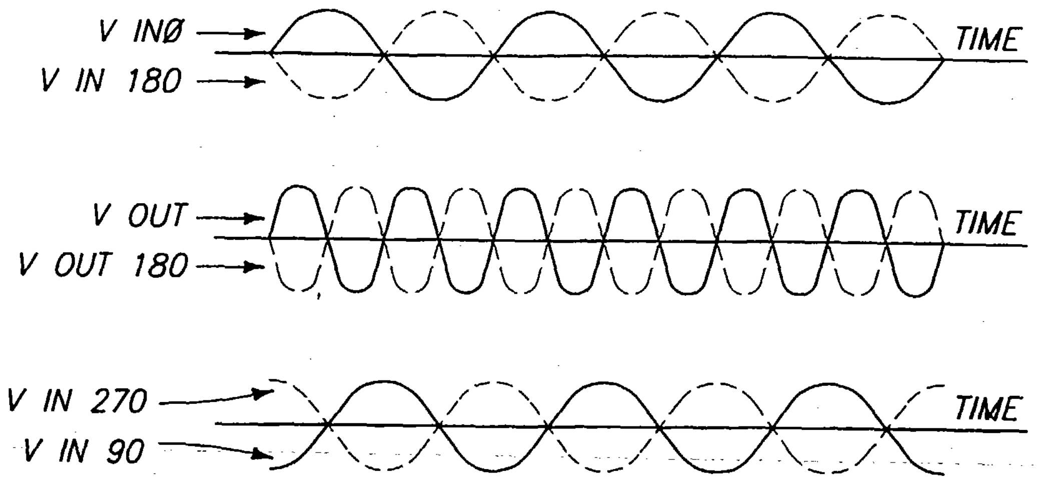

V IN0
V IN 180
TIME
V OUT
V OUT 180
TIME
V IN 270
V IN 90
TIME

Fig 35

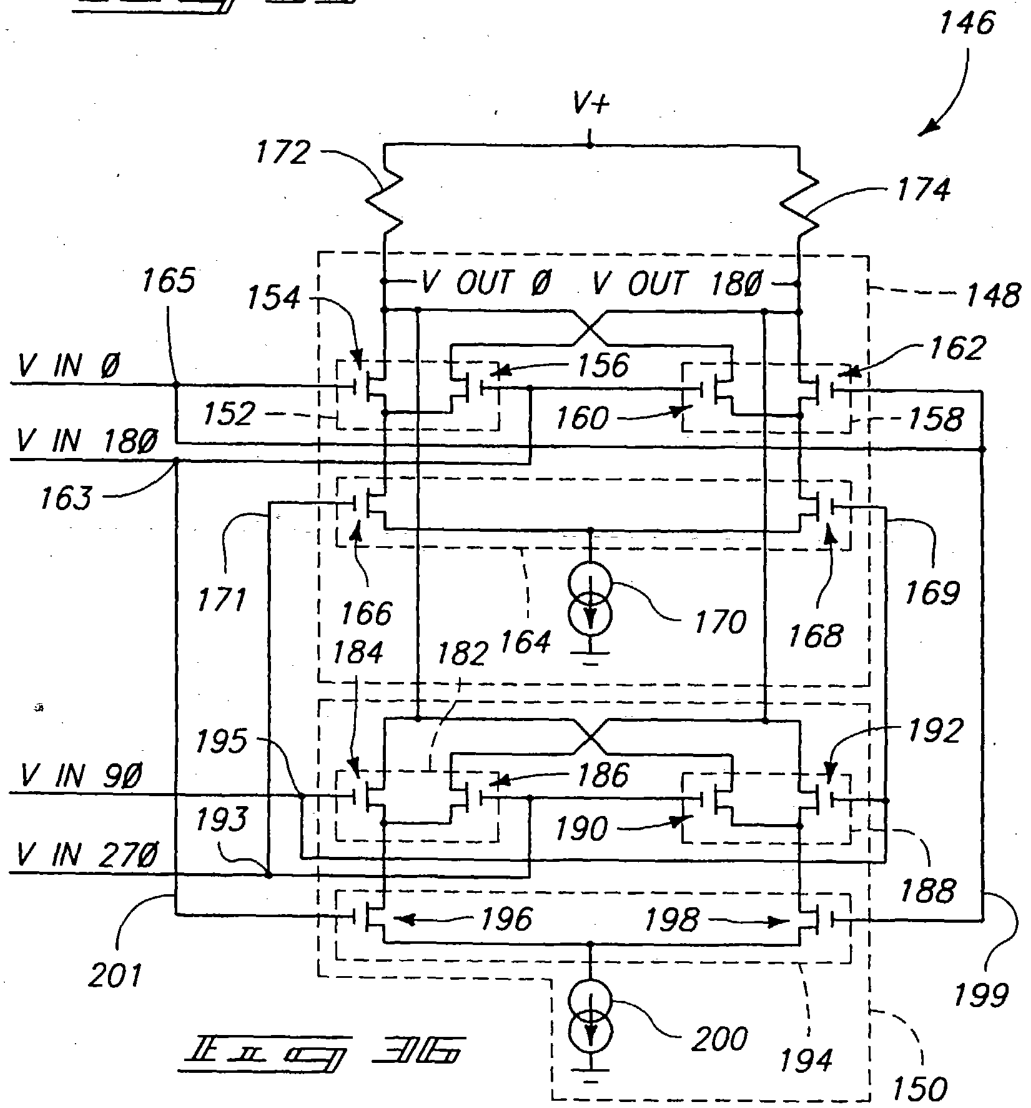

146
V+
172
174
V OUT 0
V OUT 180
148
165
154
156
162
V IN 0
152
160
158
V IN 180
163
171
166
164
170
168
169
184
182
195
186
192
V IN 90
190
193
V IN 270
188
196
198
201
199
200
194
150

Fig 36

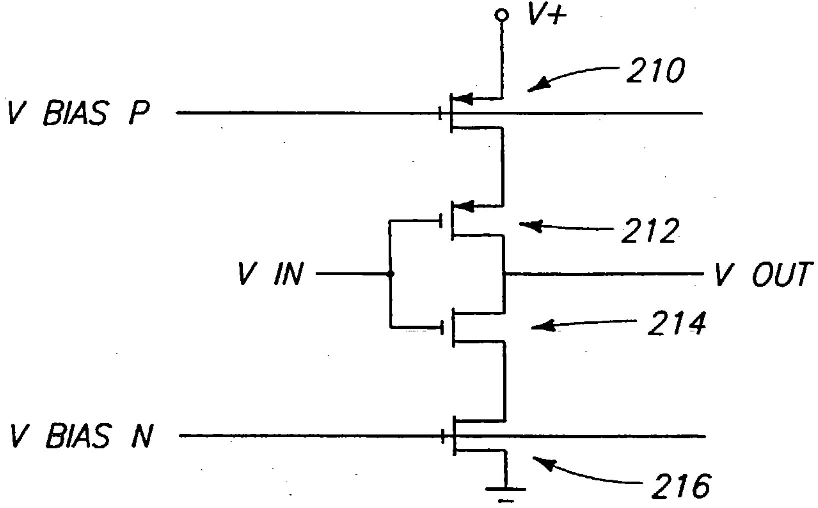


Fig 37

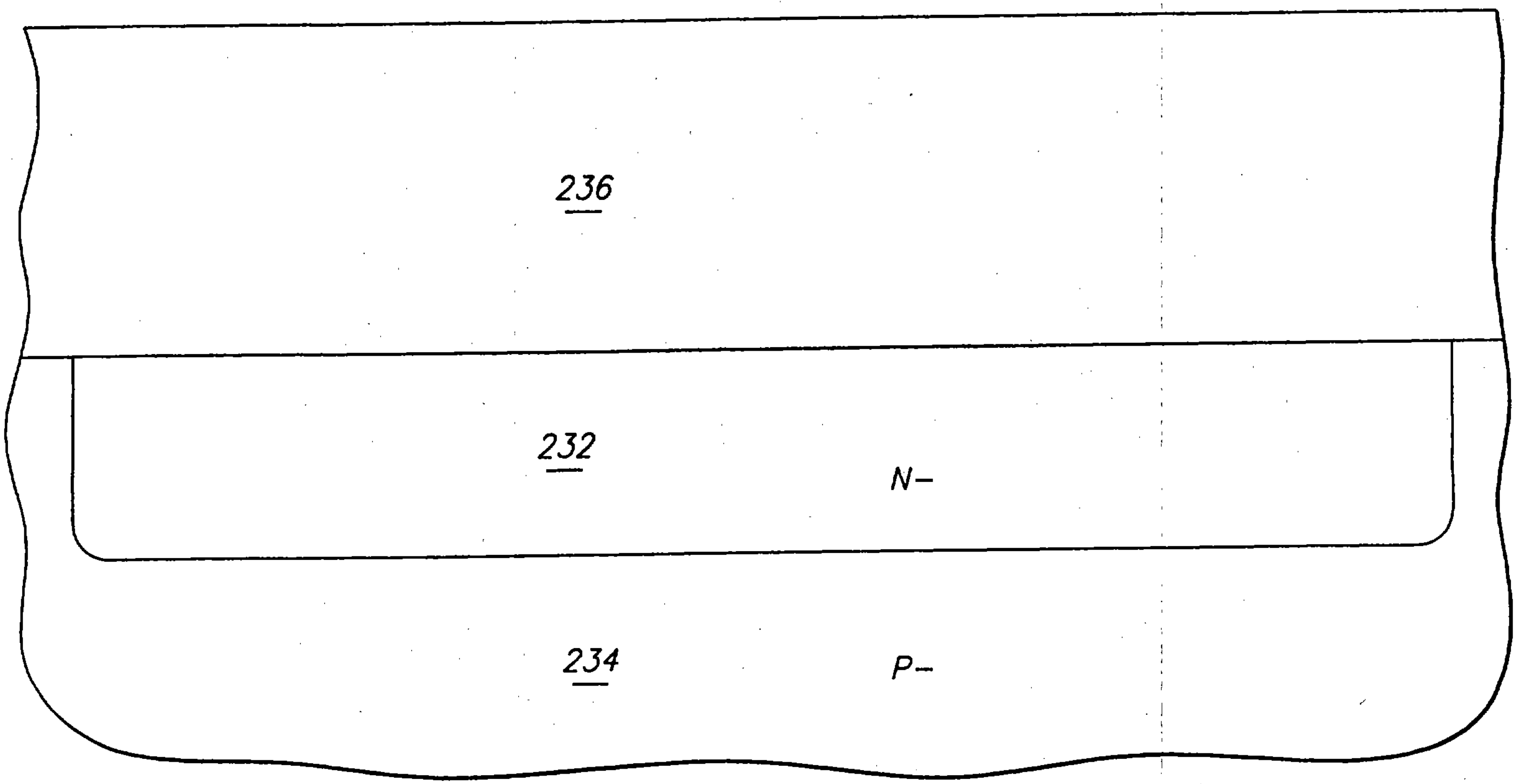


FIG 38

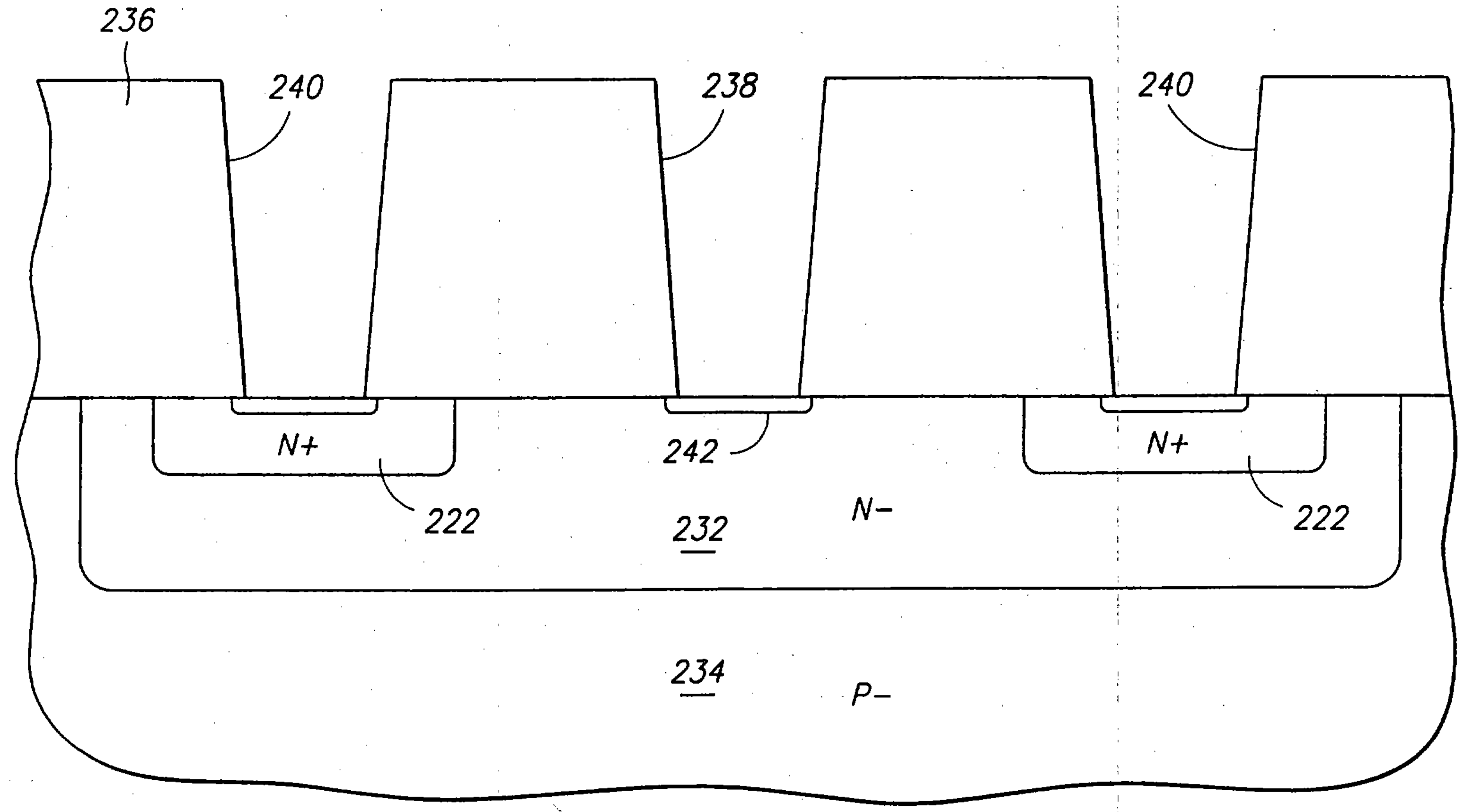


FIG 39

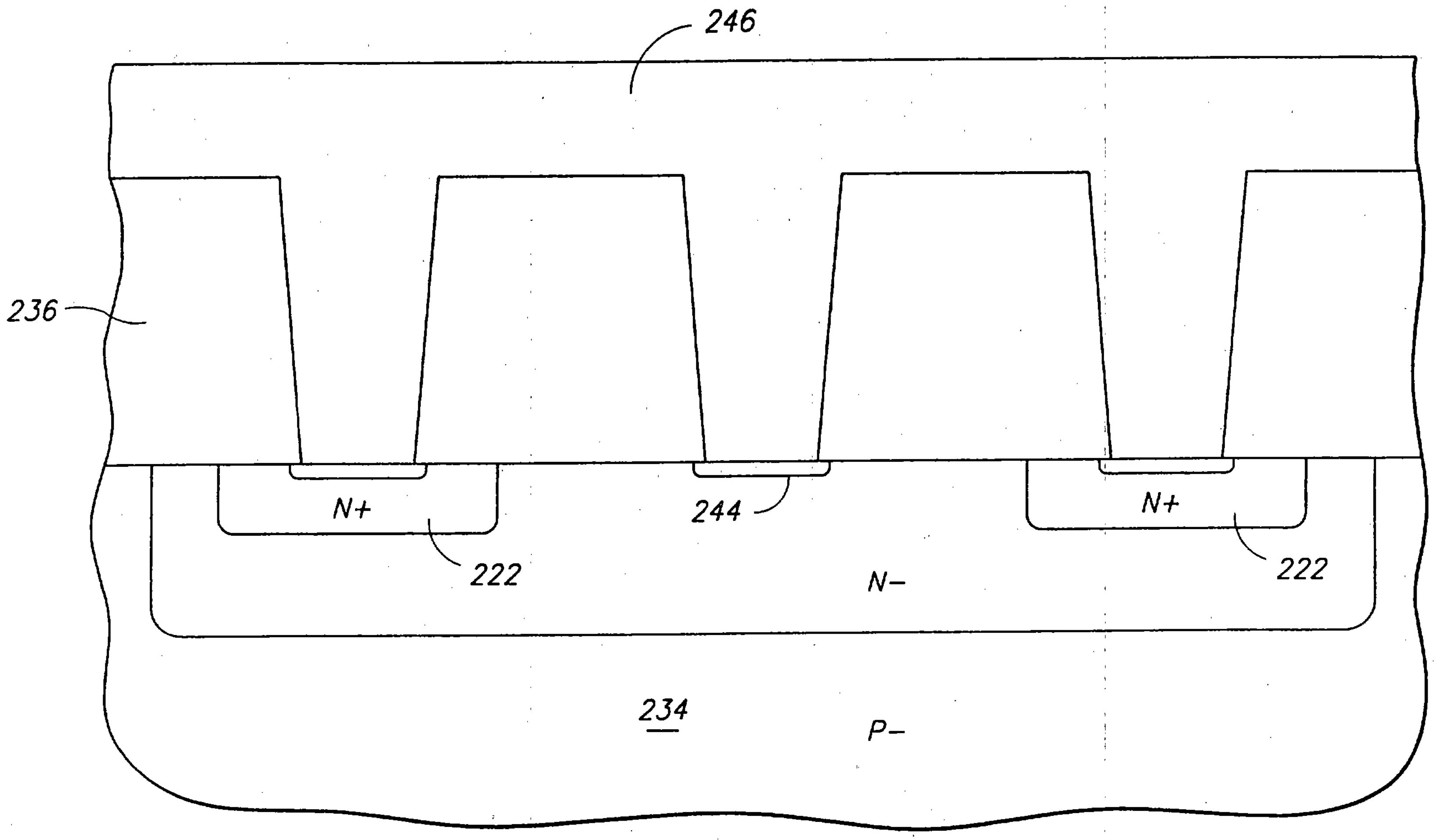


Fig. 40

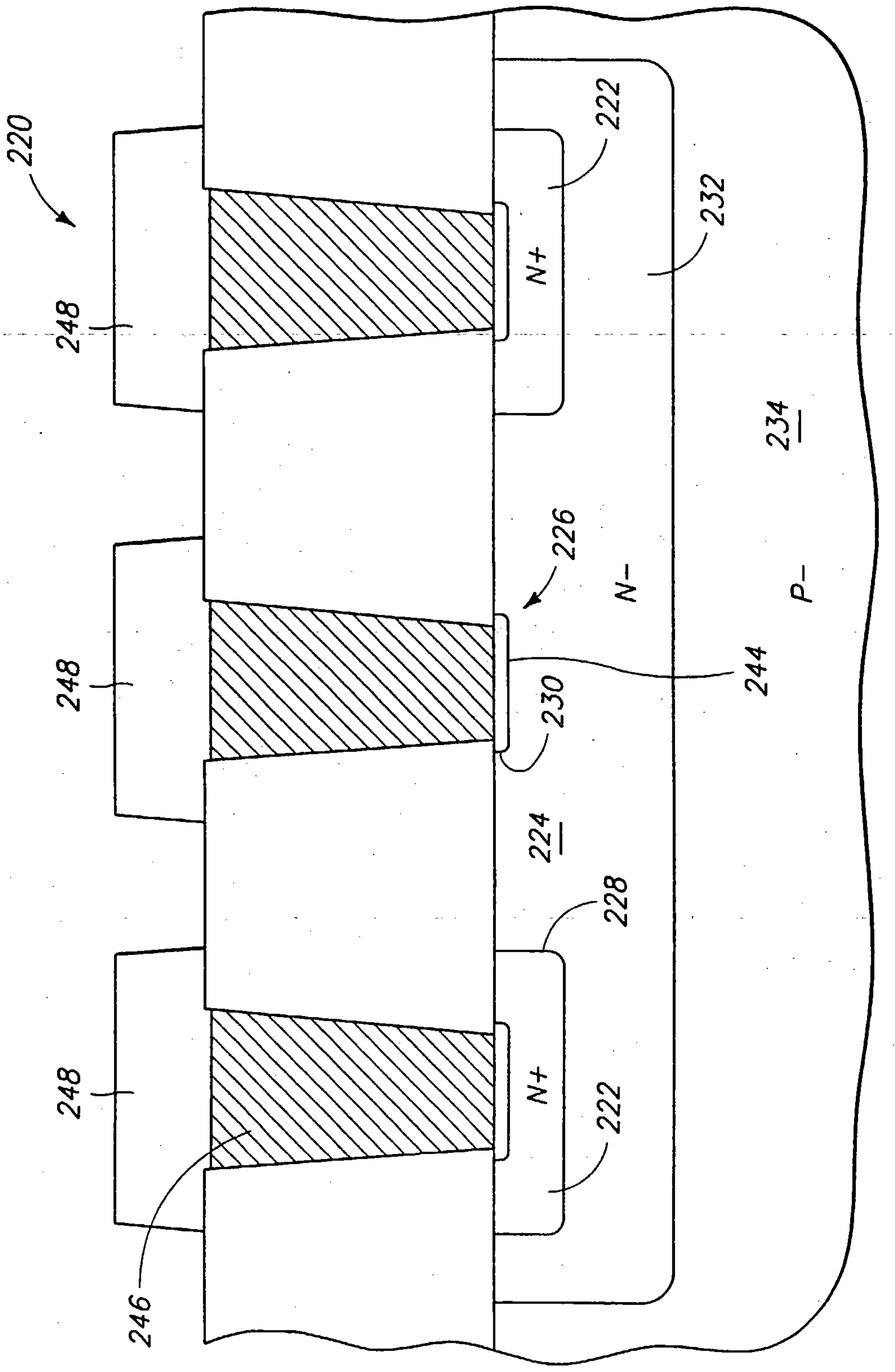


Fig. 11

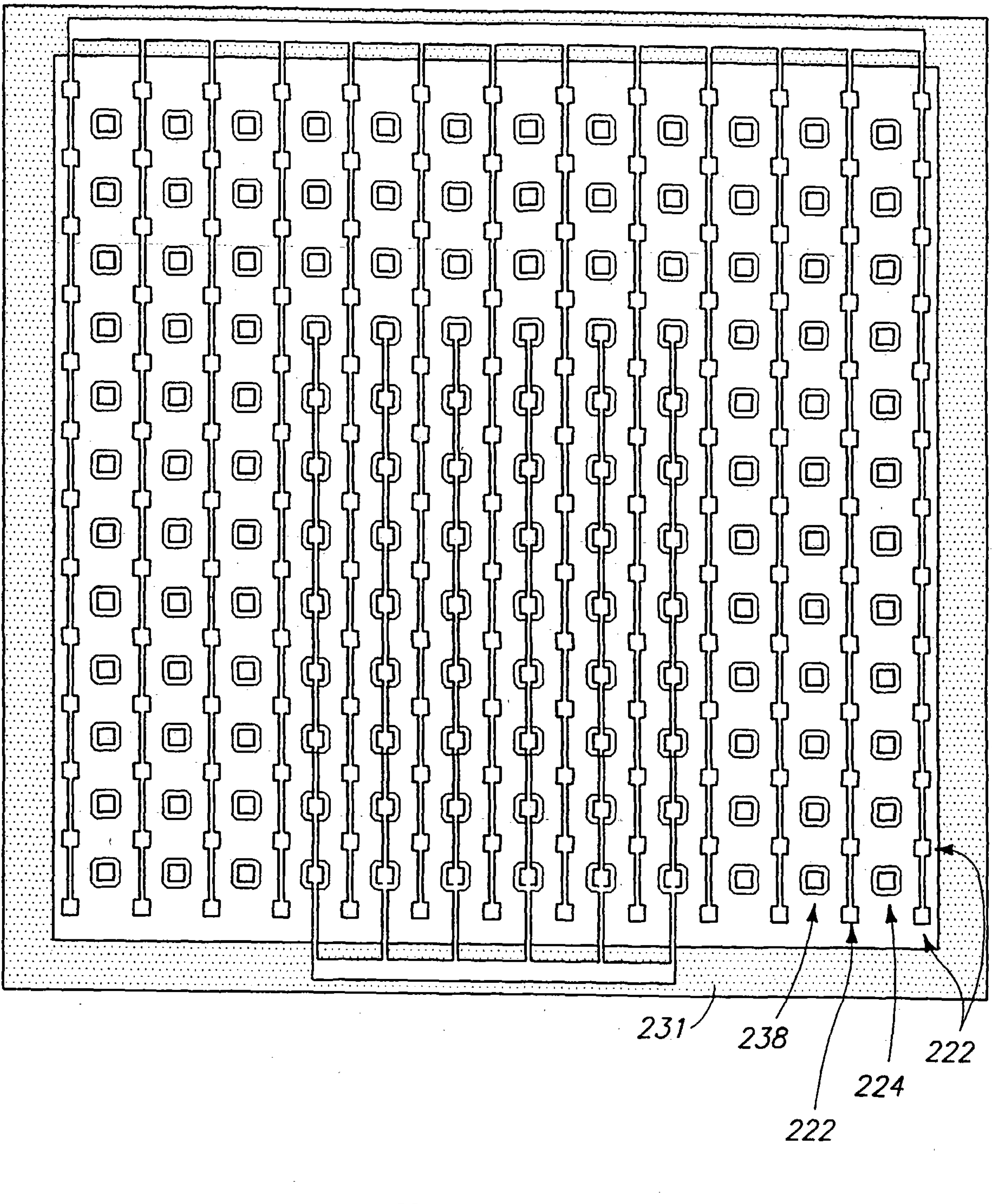


FIG 42

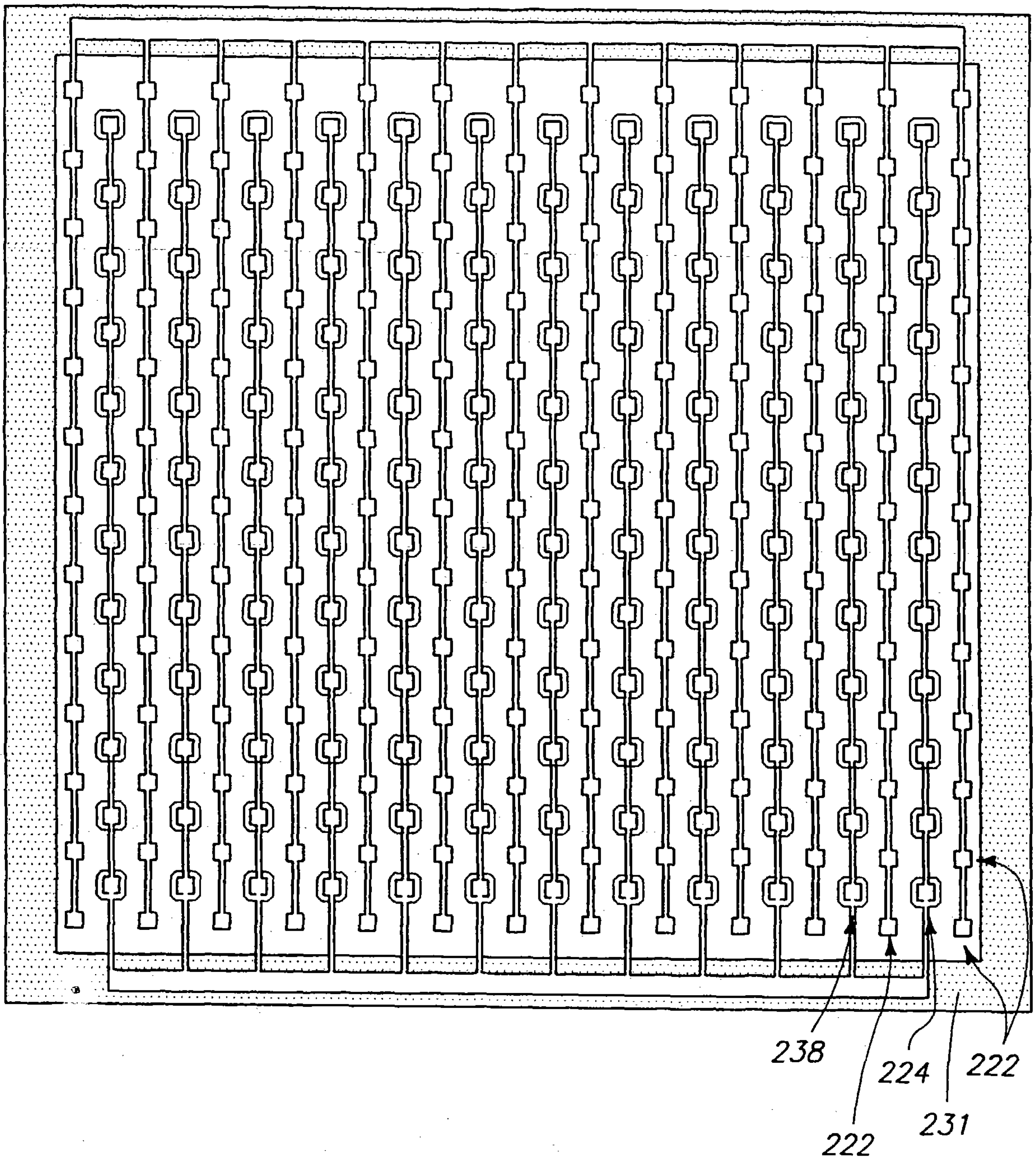


Fig 43

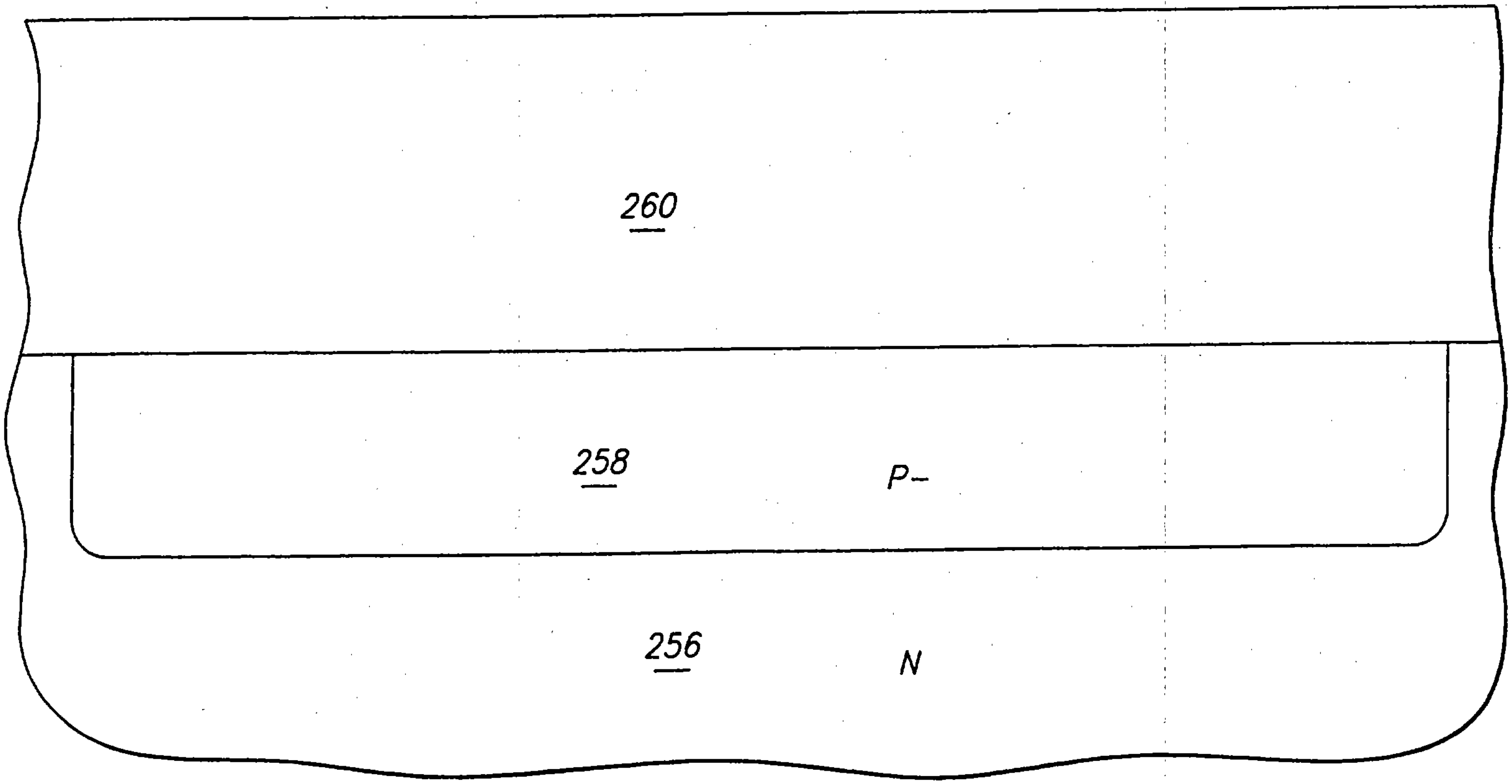


Fig 44

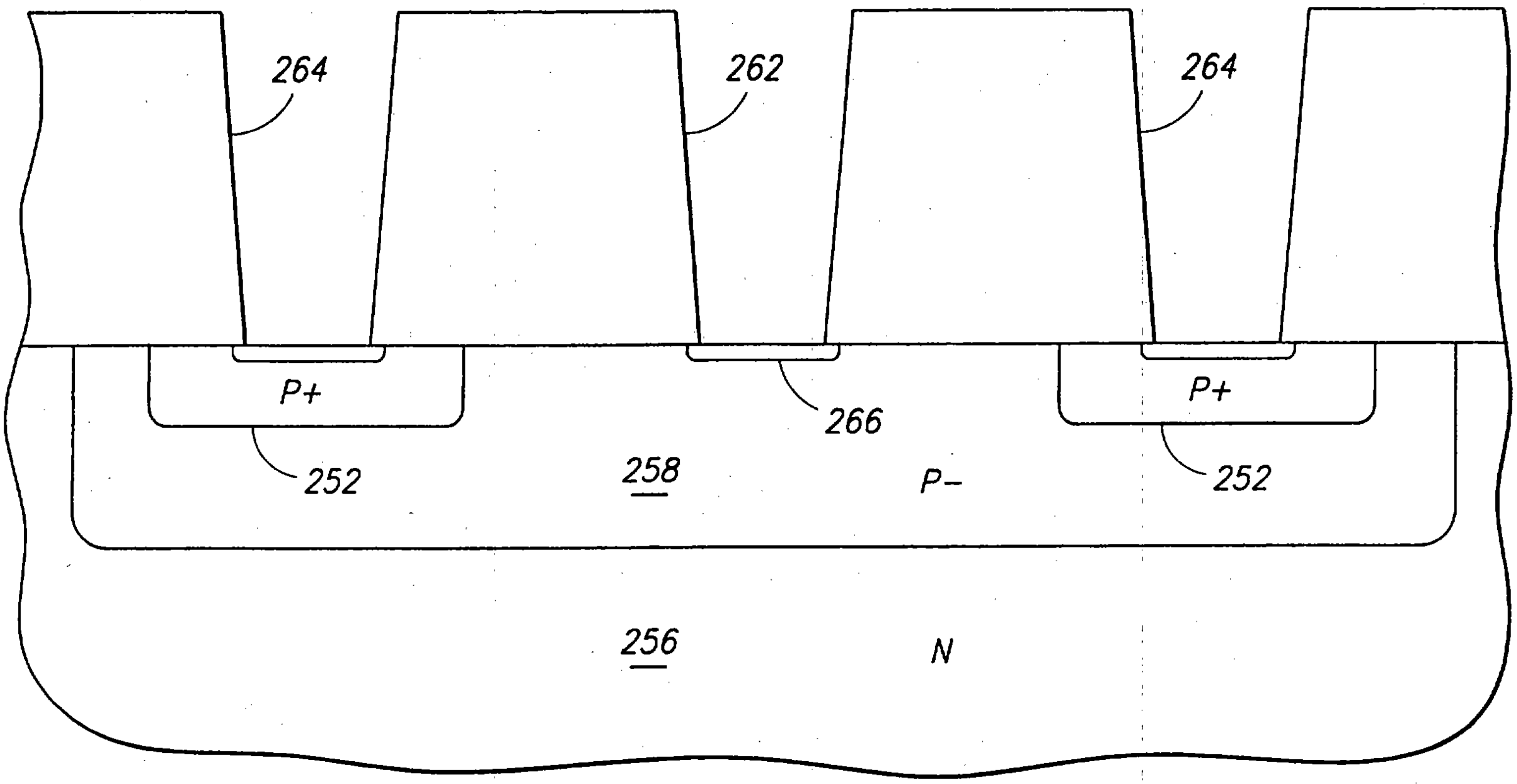


FIG 45

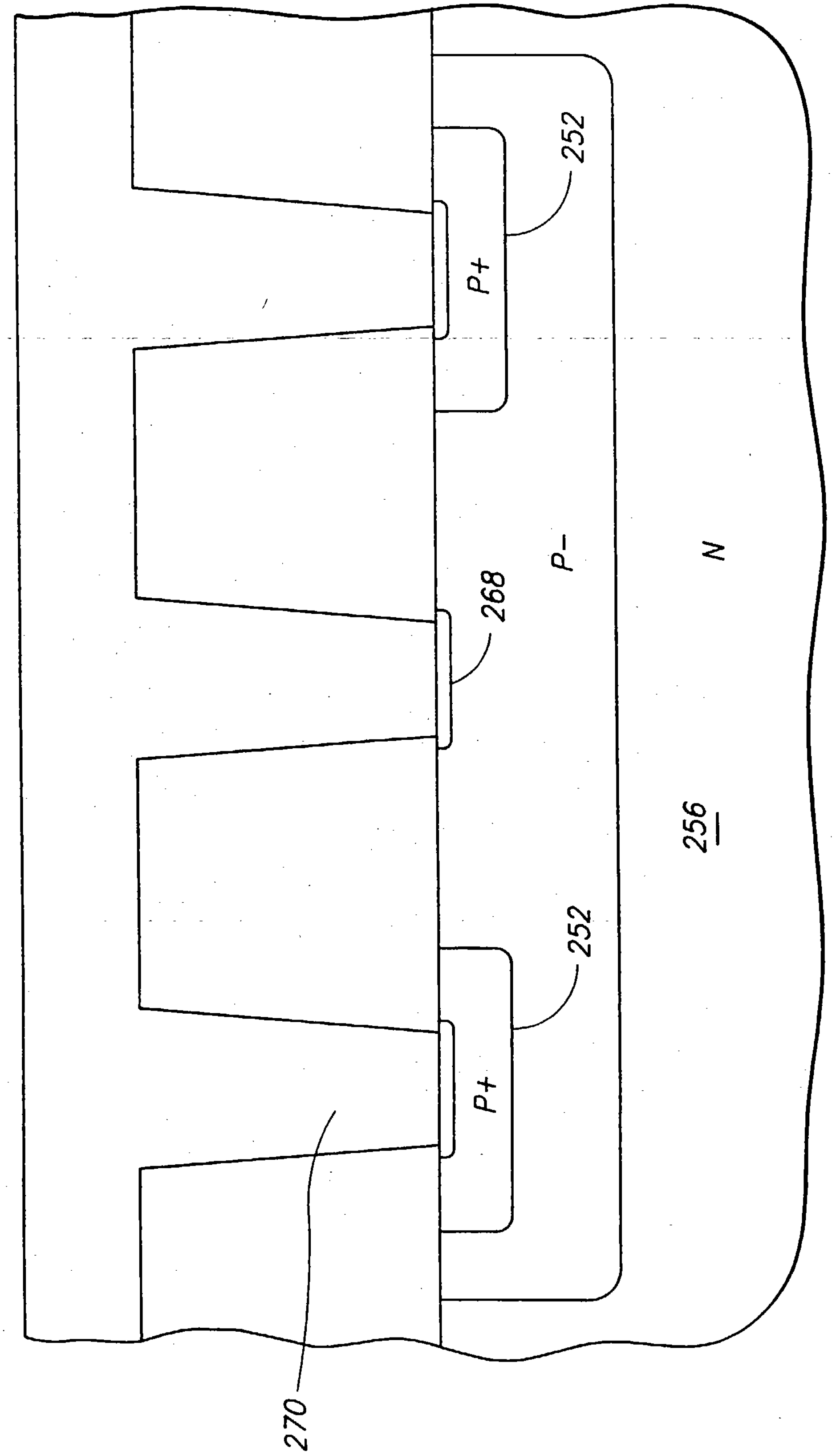


Fig 46

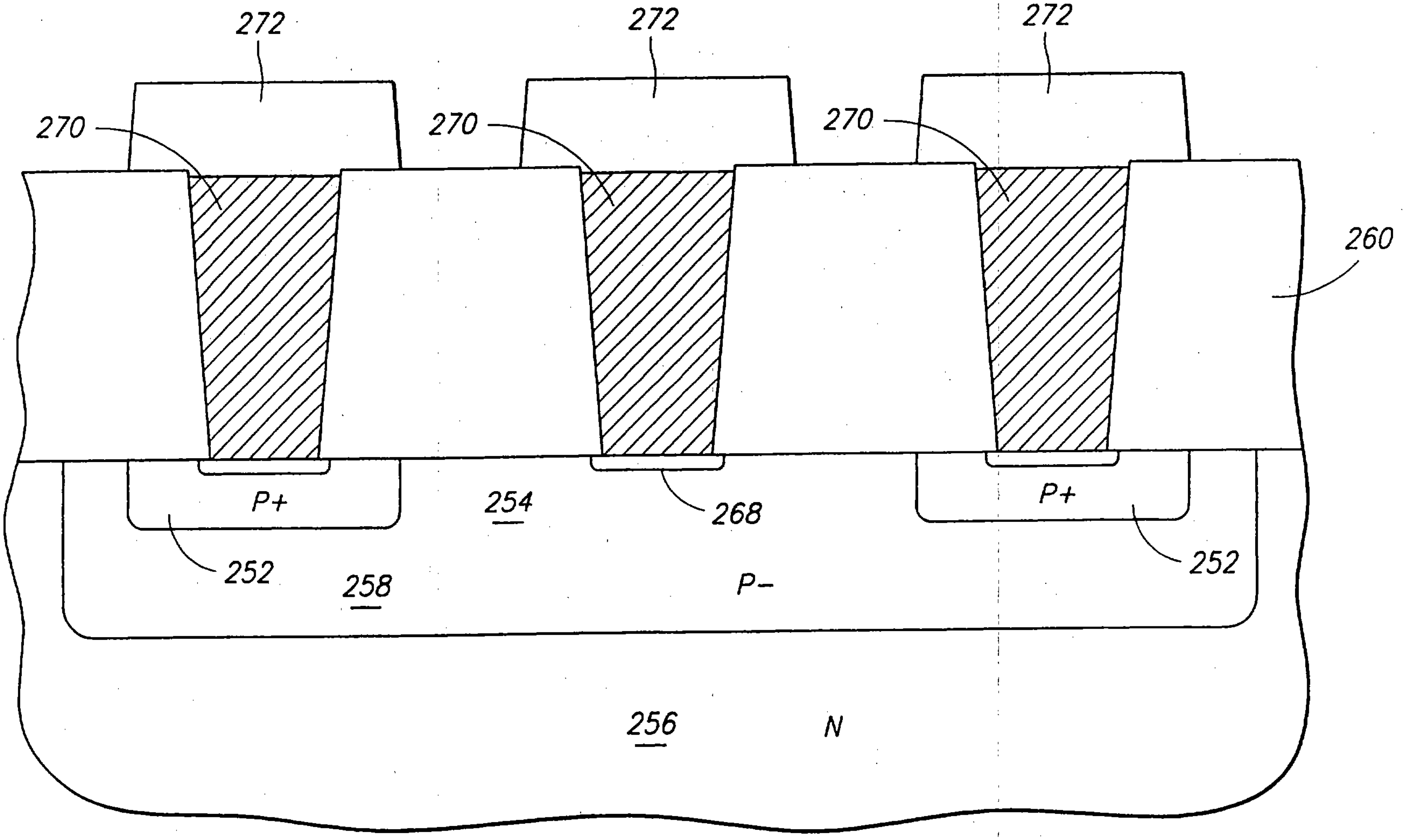


Fig. 41

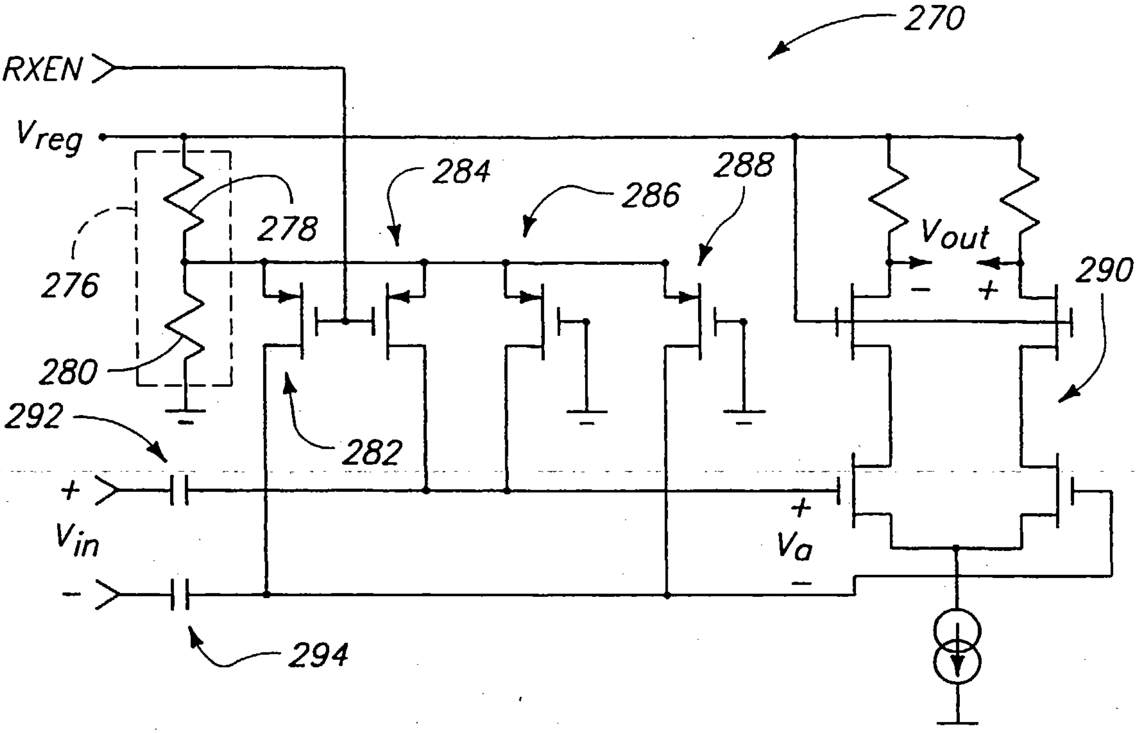

270
RXEN
Vreg
276
278
280
282
284
286
288
290
292
294
Vout
−
+
Vin
Va

Fig 48

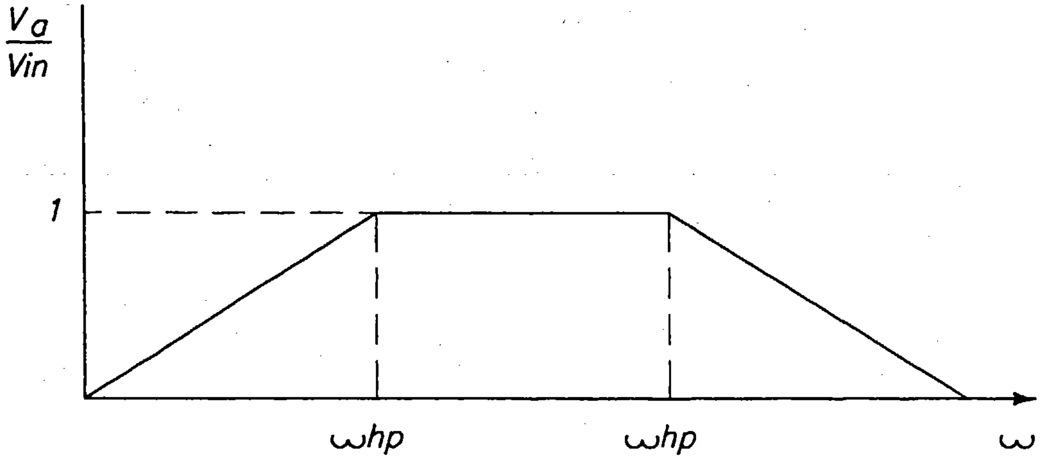

Va/Vin
1
ωhp
ωhp
ω

Fig 49

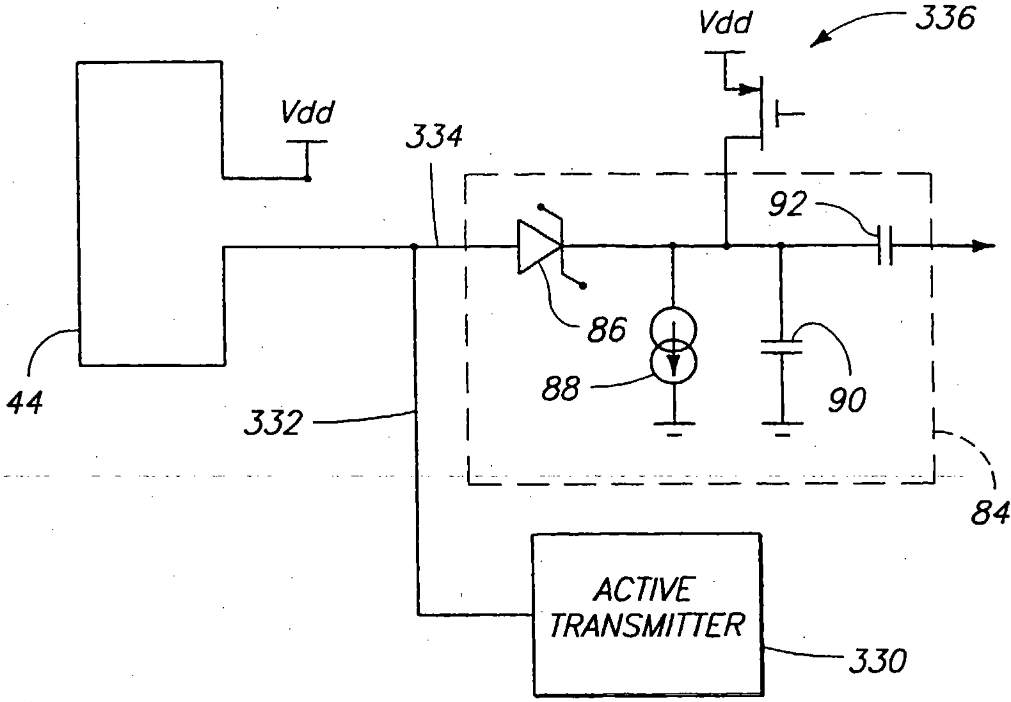

Vdd
336
Vdd
334
92
86
88
90
44
332
84
ACTIVE TRANSMITTER
330

Fig 50

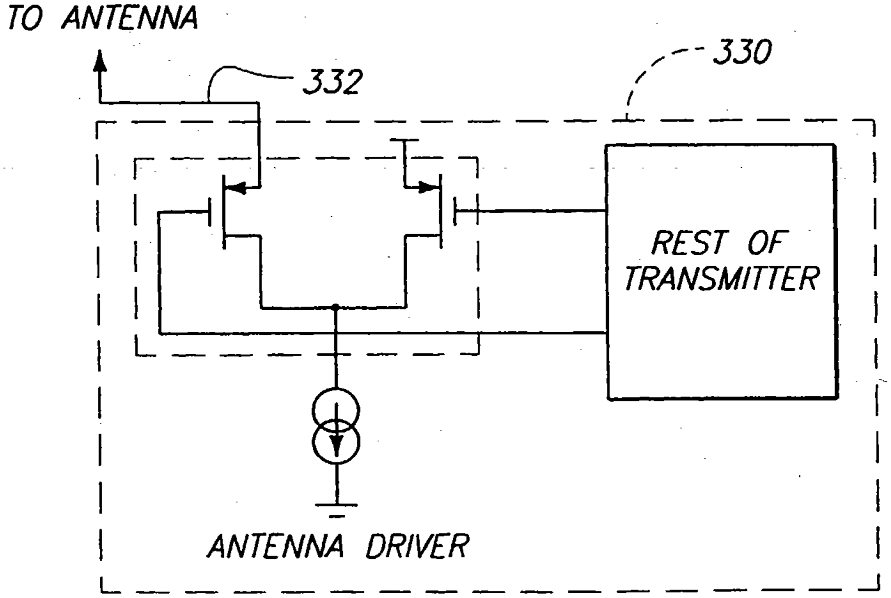

TO ANTENNA
332
330
REST OF TRANSMITTER
ANTENNA DRIVER

Fig 51

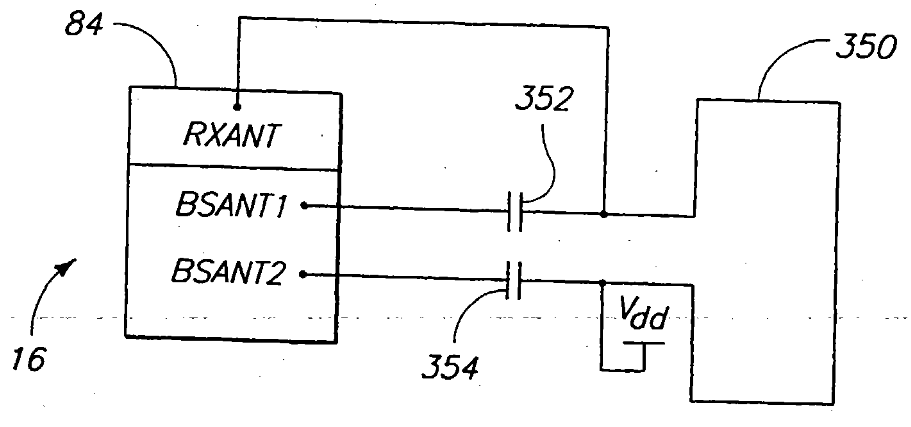

84
RXANT
BSANT1
BSANT2
16
352
354
350
Vdd

Fig 52

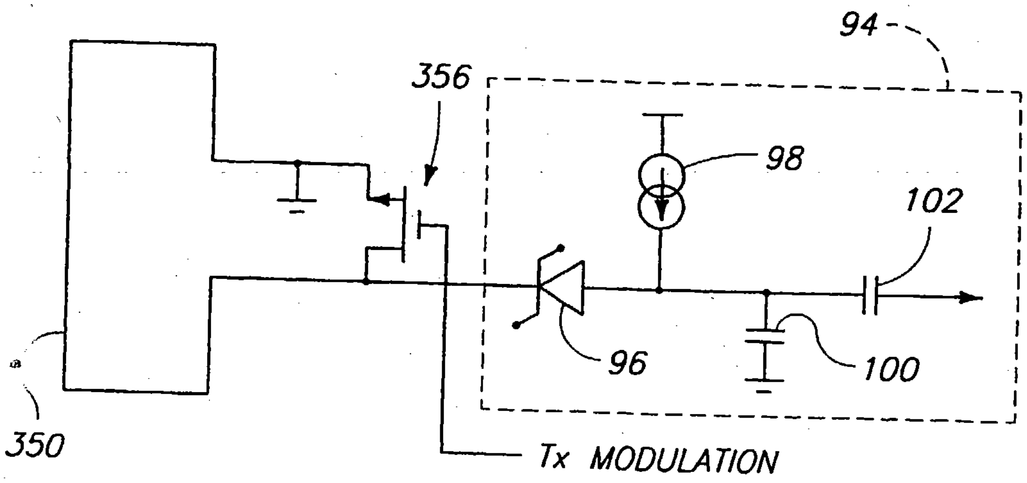

94
356
98
102
96
100
350
Tx MODULATION

Fig 53

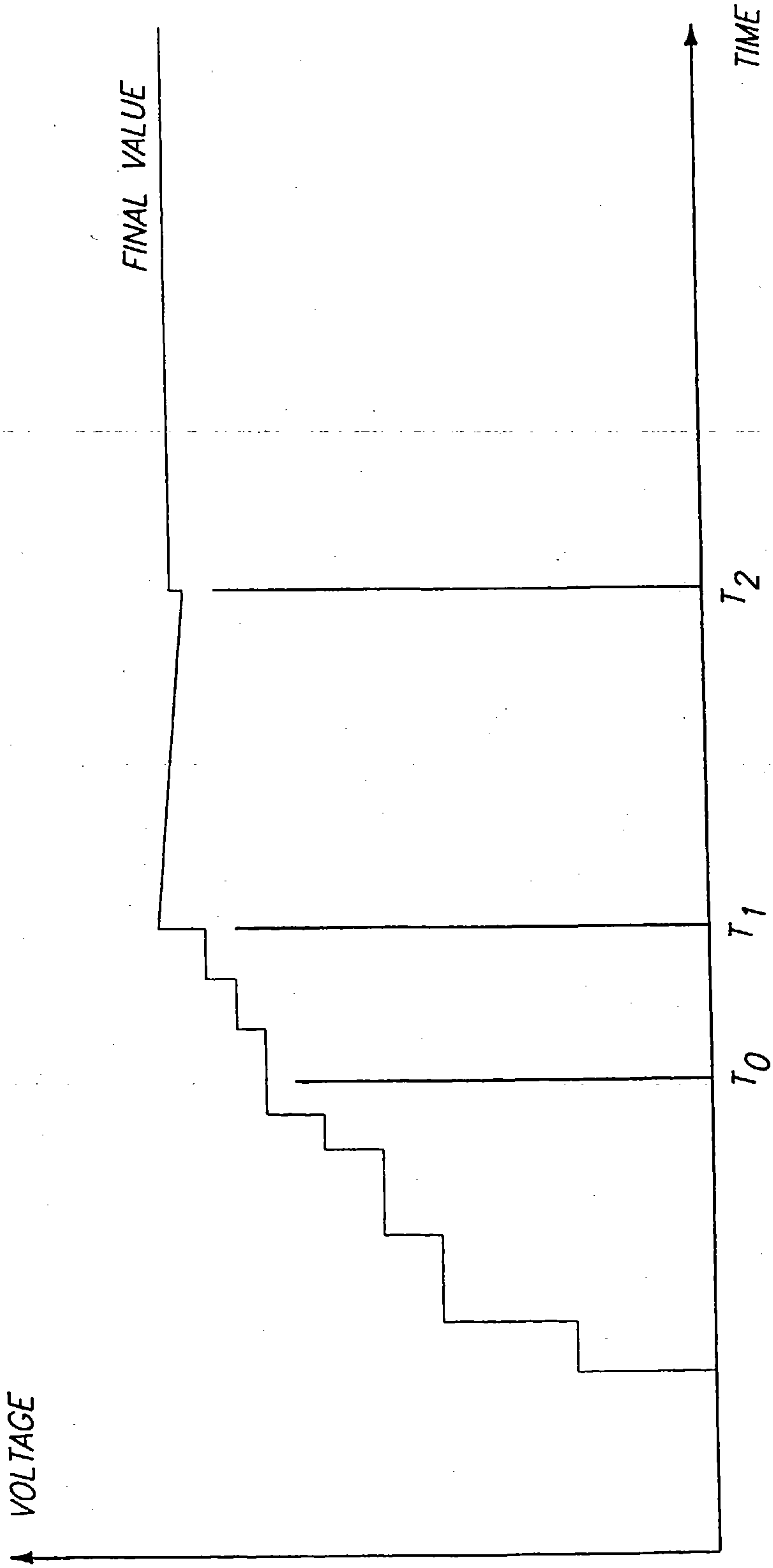
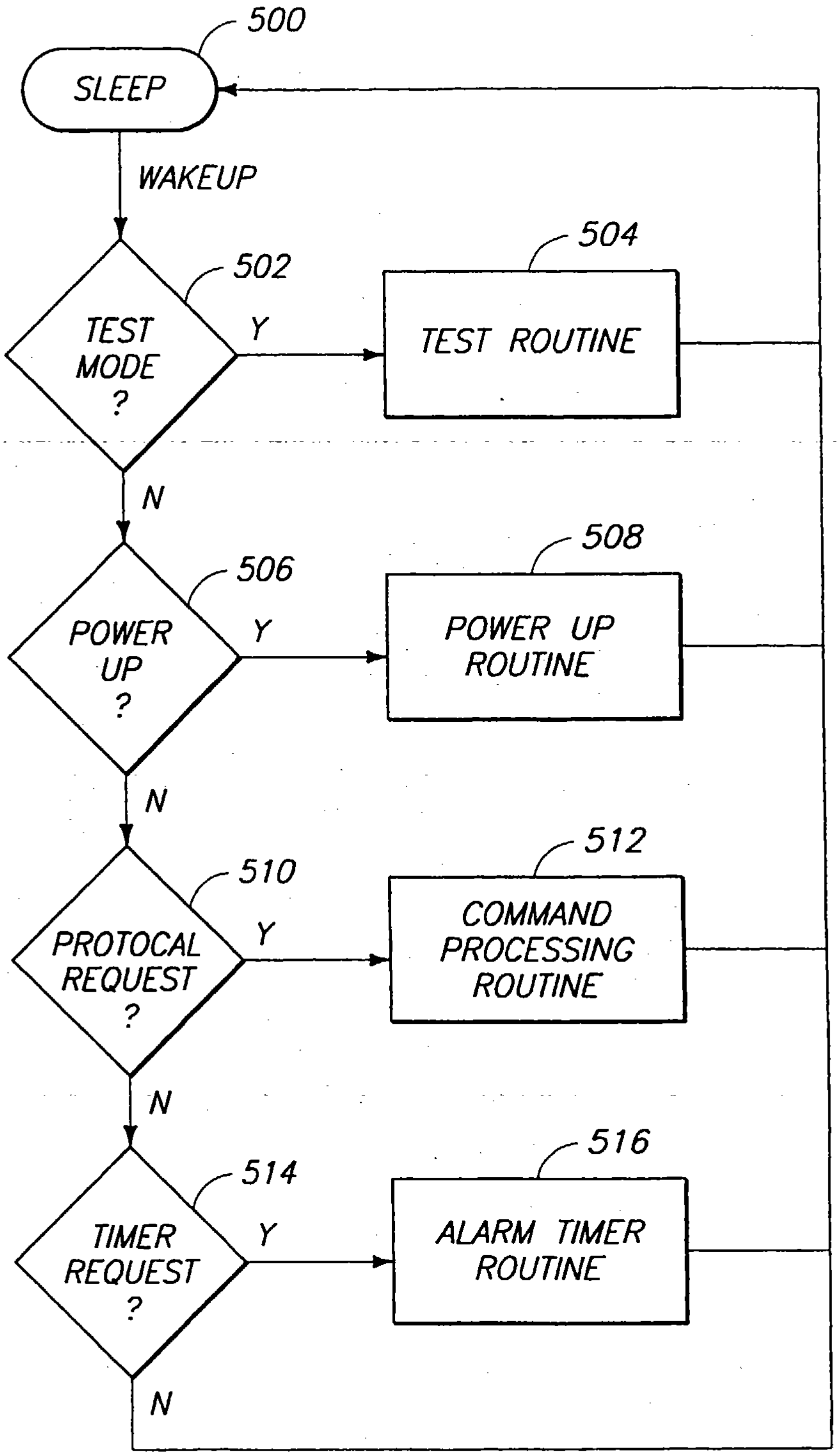


FIG. 5A



500
SLEEP
WAKEUP
502
TEST MODE ?
Y
504
TEST ROUTINE
N
506
POWER UP ?
Y
508
POWER UP ROUTINE
N
510
PROTOCAL REQUEST ?
Y
512
COMMAND PROCESSING ROUTINE
N
514
TIMER REQUEST ?
Y
516
ALARM TIMER ROUTINE
N

Fig 55

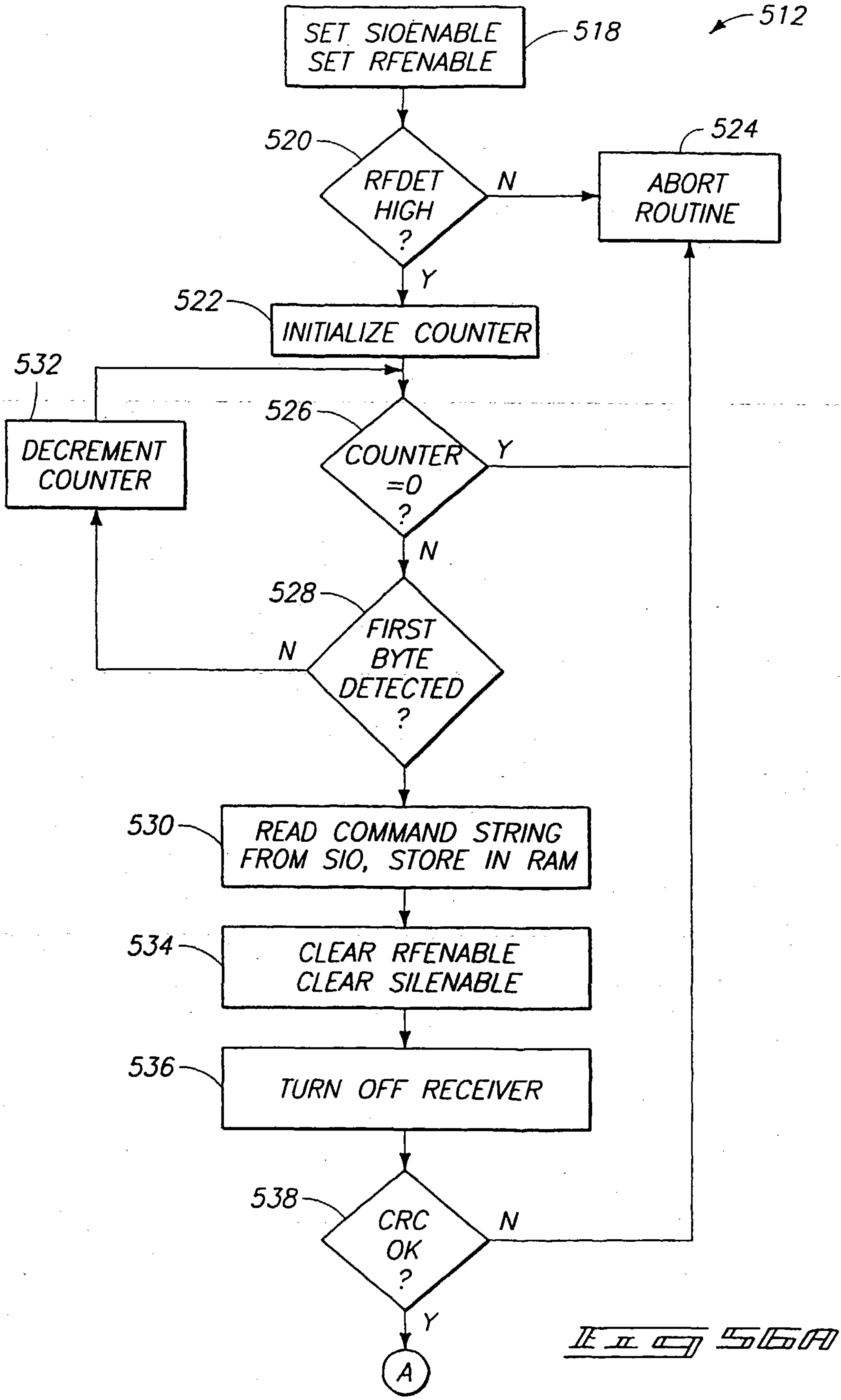
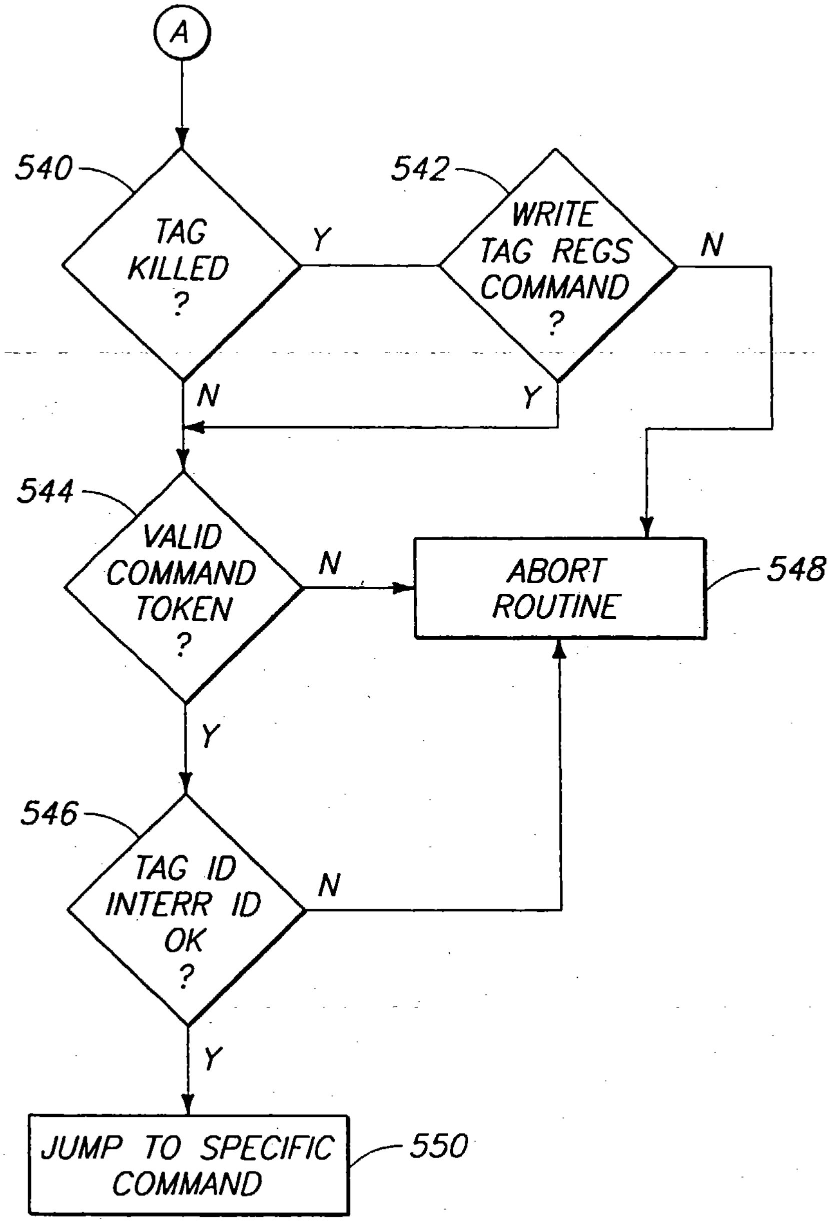

512
SET SIOENABLE
SET RFENABLE
518
520
RFDET HIGH ?
N
Y
ABORT ROUTINE
524
522
INITIALIZE COUNTER
532
DECREMENT COUNTER
526
COUNTER =0 ?
Y
N
528
FIRST BYTE DETECTED ?
N
530
READ COMMAND STRING FROM SIO, STORE IN RAM
534
CLEAR RFENABLE
CLEAR SILENABLE
536
TURN OFF RECEIVER
538
CRC OK ?
N
Y
A

Fig 56A



A
540
TAG KILLED ?
Y
542
WRITE TAG REGS COMMAND ?
N
N
Y
544
VALID COMMAND TOKEN ?
N
ABORT ROUTINE
548
Y
546
TAG ID INTERR ID OK ?
N
Y
JUMP TO SPECIFIC COMMAND
550

Fig 56B

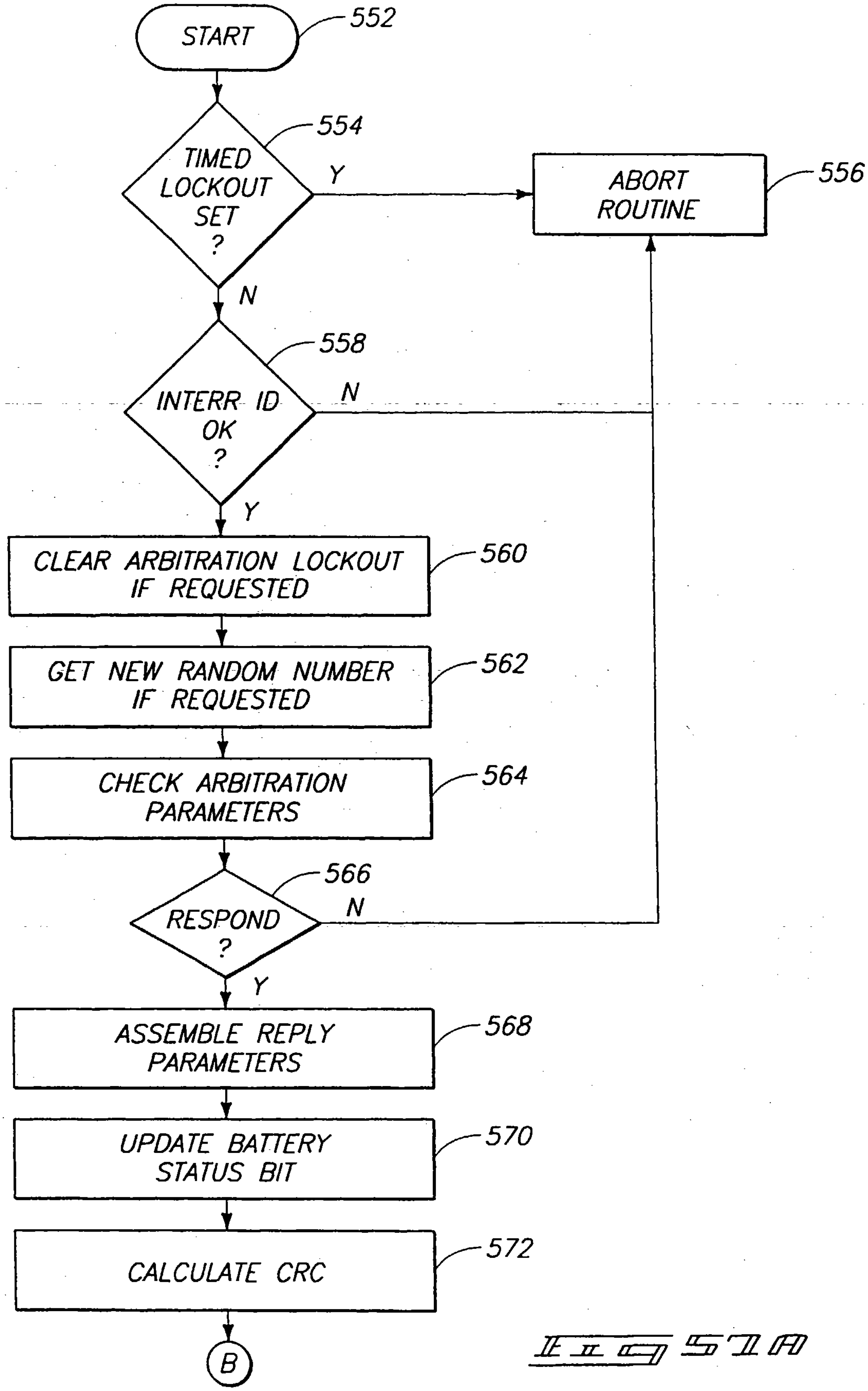

START
552
TIMED LOCKOUT SET ?
554
Y
ABORT ROUTINE
556
N
INTERR ID OK ?
558
N
Y
CLEAR ARBITRATION LOCKOUT IF REQUESTED
560
GET NEW RANDOM NUMBER IF REQUESTED
562
CHECK ARBITRATION PARAMETERS
564
RESPOND ?
566
N
Y
ASSEMBLE REPLY PARAMETERS
568
UPDATE BATTERY STATUS BIT
570
CALCULATE CRC
572
B

Fig. 51A

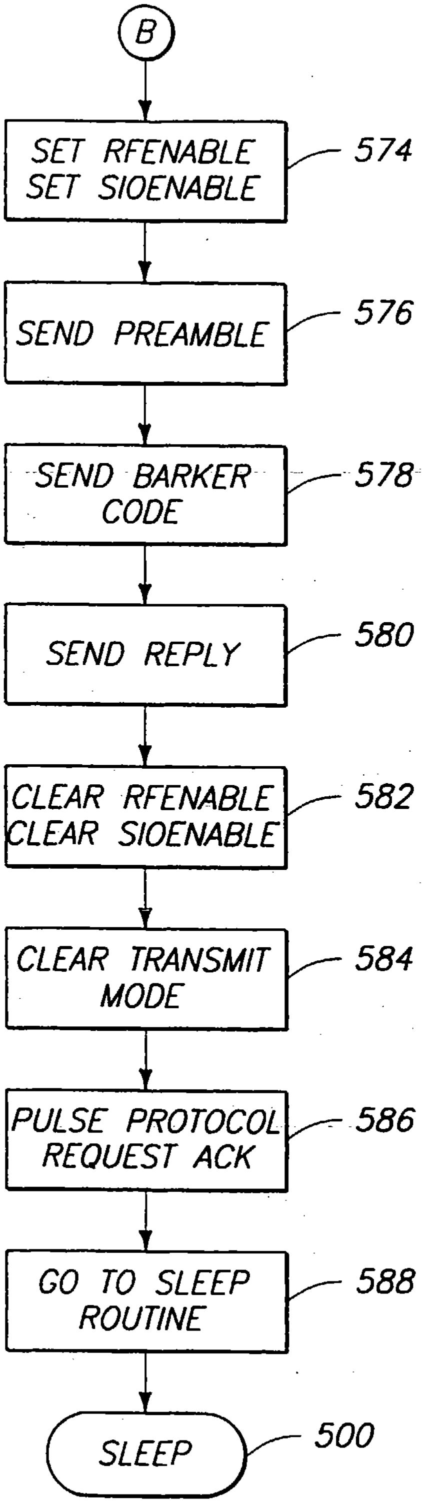

B
SET RFENABLE
SET SIOENABLE
574
SEND PREAMBLE
576
SEND BARKER CODE
578
SEND REPLY
580
CLEAR RFENABLE
CLEAR SIOENABLE
582
CLEAR TRANSMIT MODE
584
PULSE PROTOCOL REQUEST ACK
586
GO TO SLEEP ROUTINE
588
SLEEP
500

Fig 51B

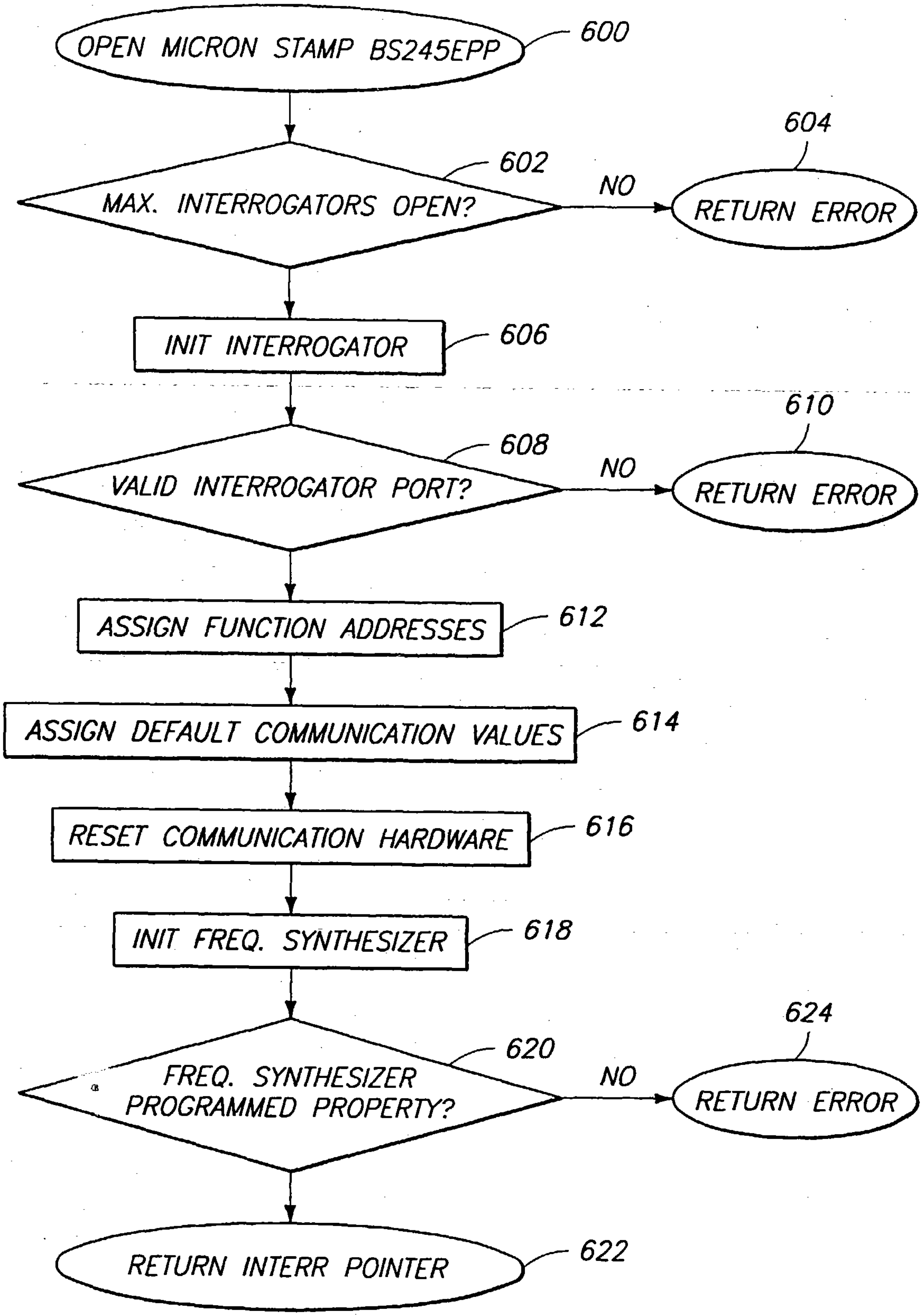

OPEN MICRON STAMP BS245EPP
600
MAX. INTERROGATORS OPEN?
602
NO
RETURN ERROR
604
INIT INTERROGATOR
606
VALID INTERROGATOR PORT?
608
NO
RETURN ERROR
610
ASSIGN FUNCTION ADDRESSES
612
ASSIGN DEFAULT COMMUNICATION VALUES
614
RESET COMMUNICATION HARDWARE
616
INIT FREQ. SYNTHESIZER
618
FREQ. SYNTHESIZER PROGRAMMED PROPERTY?
620
NO
RETURN ERROR
624
RETURN INTERR POINTER
622

FIG 58

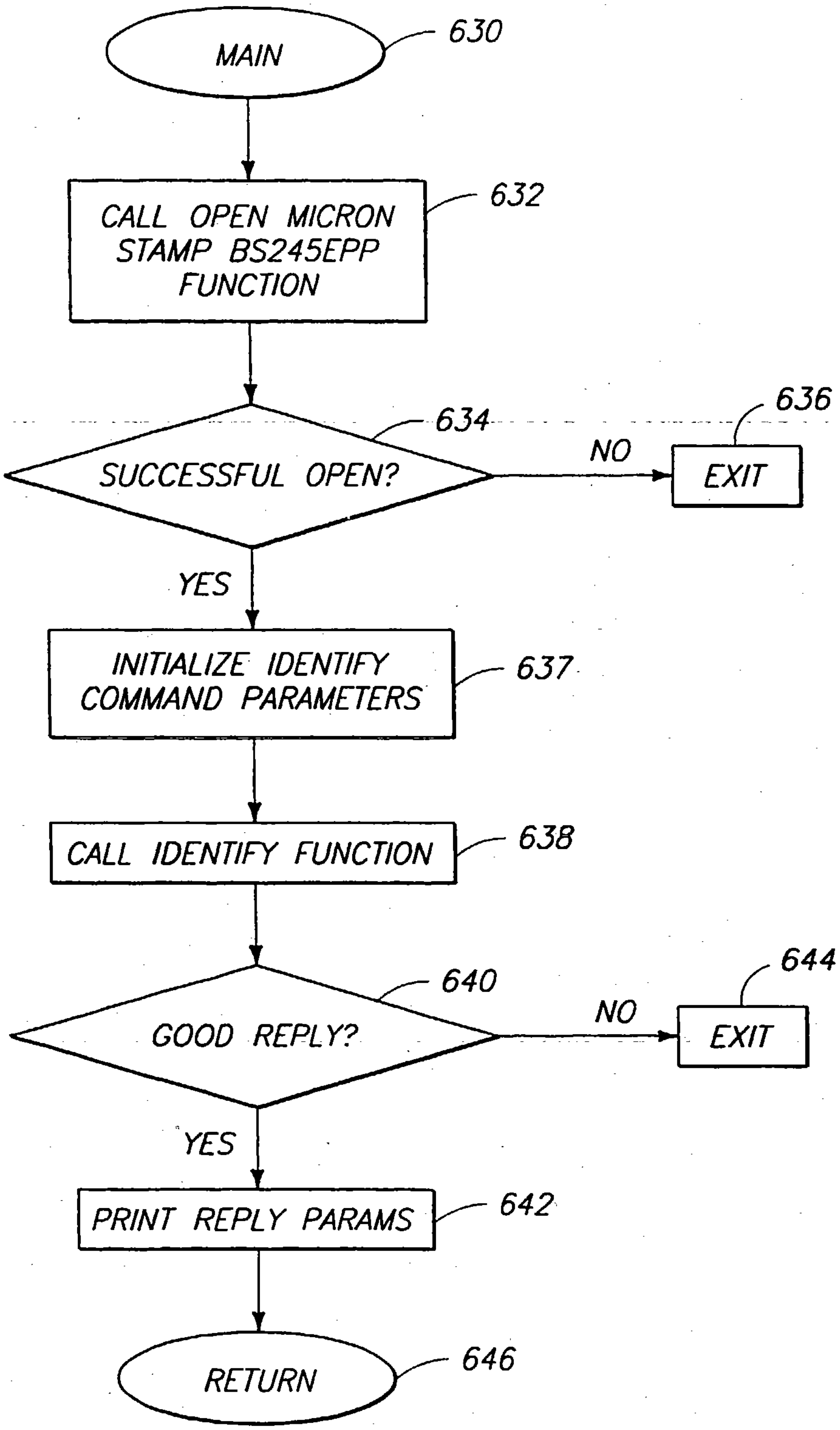

MAIN
630
CALL OPEN MICRON STAMP BS245EPP FUNCTION
632
SUCCESSFUL OPEN?
634
NO
EXIT
636
YES
INITIALIZE IDENTIFY COMMAND PARAMETERS
637
CALL IDENTIFY FUNCTION
638
GOOD REPLY?
640
NO
EXIT
644
YES
PRINT REPLY PARAMS
642
RETURN
646

Fig 59

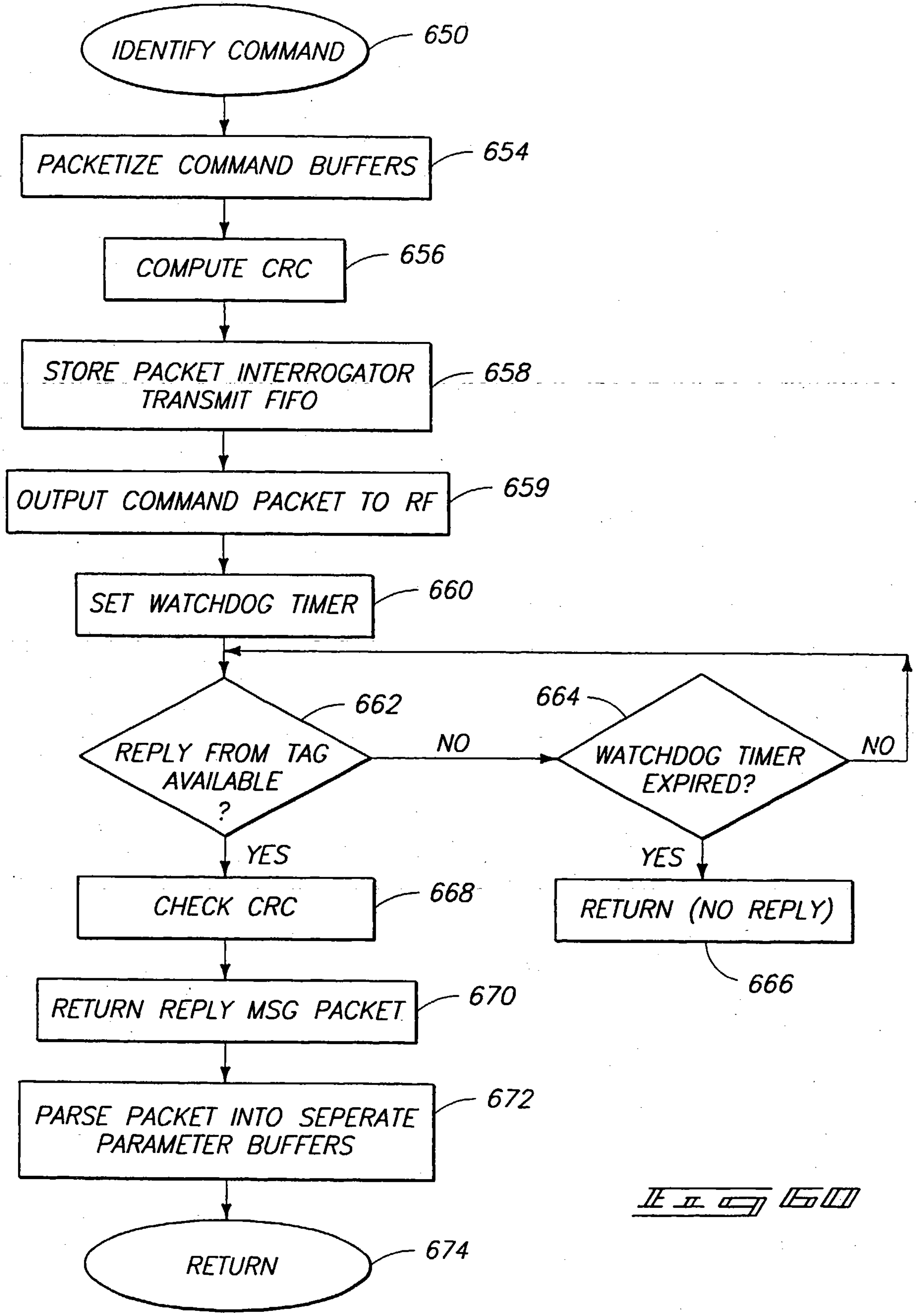

IDENTIFY COMMAND
650
PACKETIZE COMMAND BUFFERS
654
COMPUTE CRC
656
STORE PACKET INTERROGATOR TRANSMIT FIFO
658
OUTPUT COMMAND PACKET TO RF
659
SET WATCHDOG TIMER
660
662
REPLY FROM TAG AVAILABLE ?
NO
664
WATCHDOG TIMER EXPIRED?
NO
YES
YES
CHECK CRC
668
RETURN (NO REPLY)
666
RETURN REPLY MSG PACKET
670
PARSE PACKET INTO SEPERATE PARAMETER BUFFERS
672
RETURN
674

Fig 60

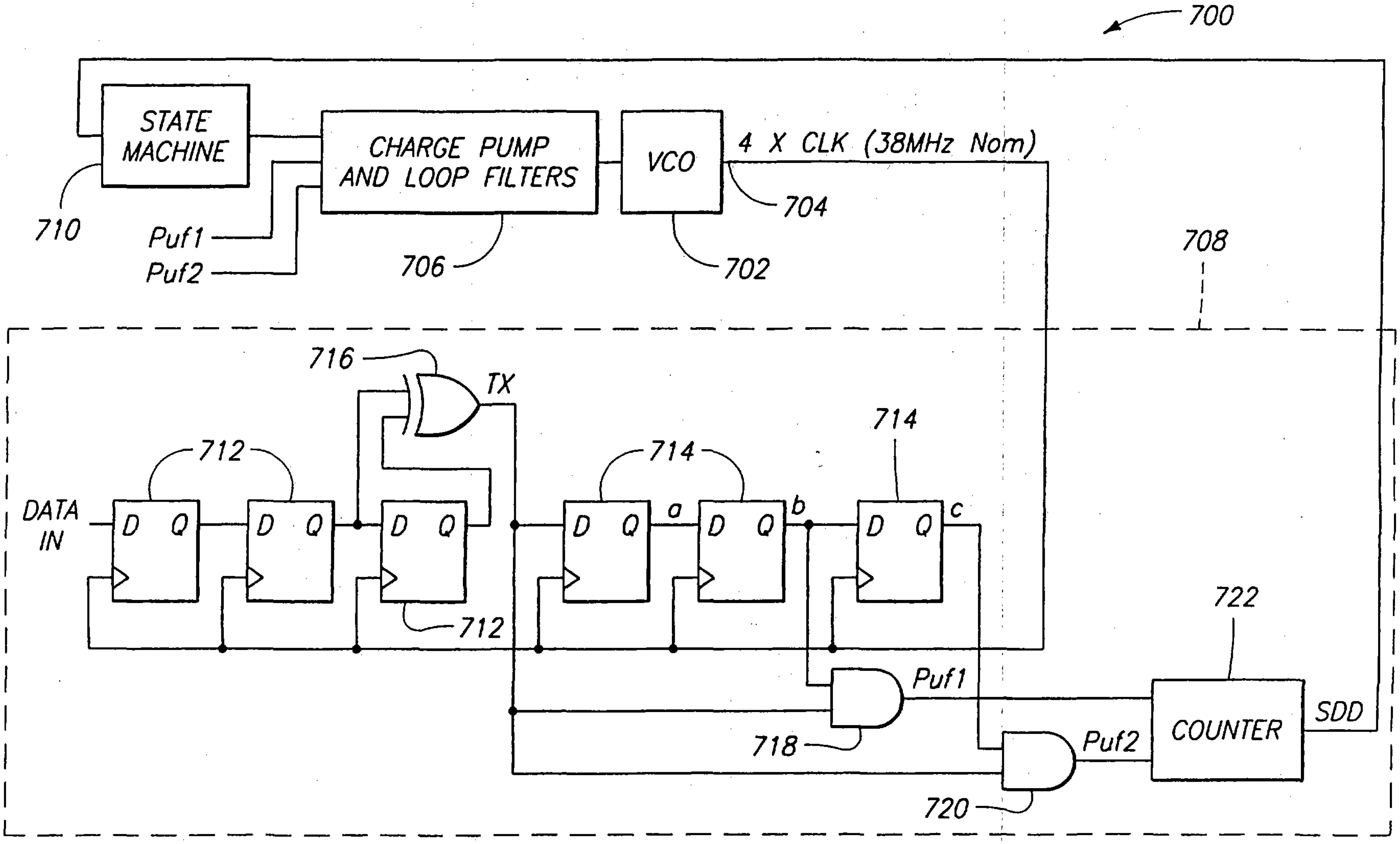

700
STATE MACHINE
CHARGE PUMP AND LOOP FILTERS
VCO
4 X CLK (38MHz Nom)
710
Puf1
Puf2
706
704
702
708
716
TX
712
714
714
DATA IN
D
Q
a
b
c
712
722
Puf1
COUNTER
SDD
Puf2
718
720

Fig 61

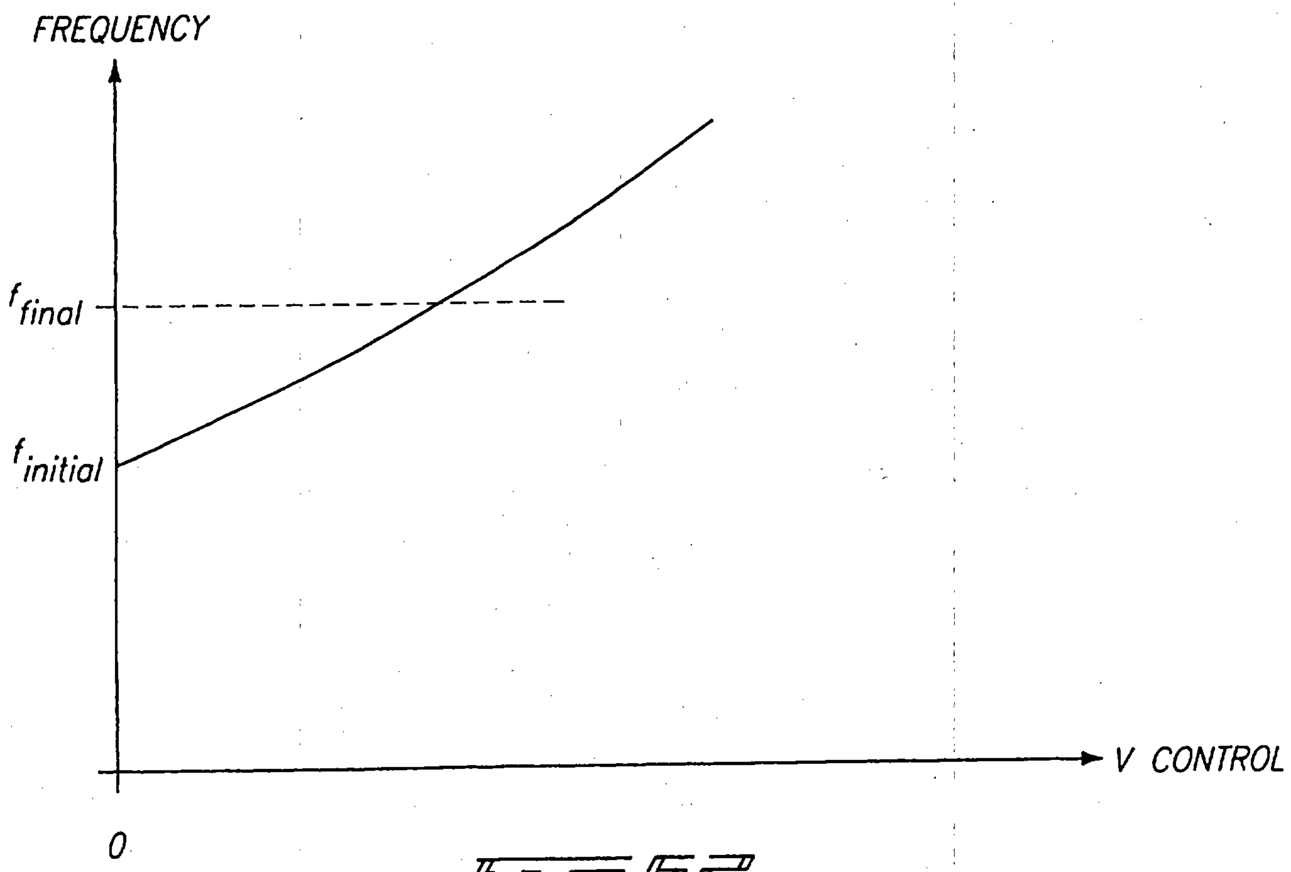


Fig 62

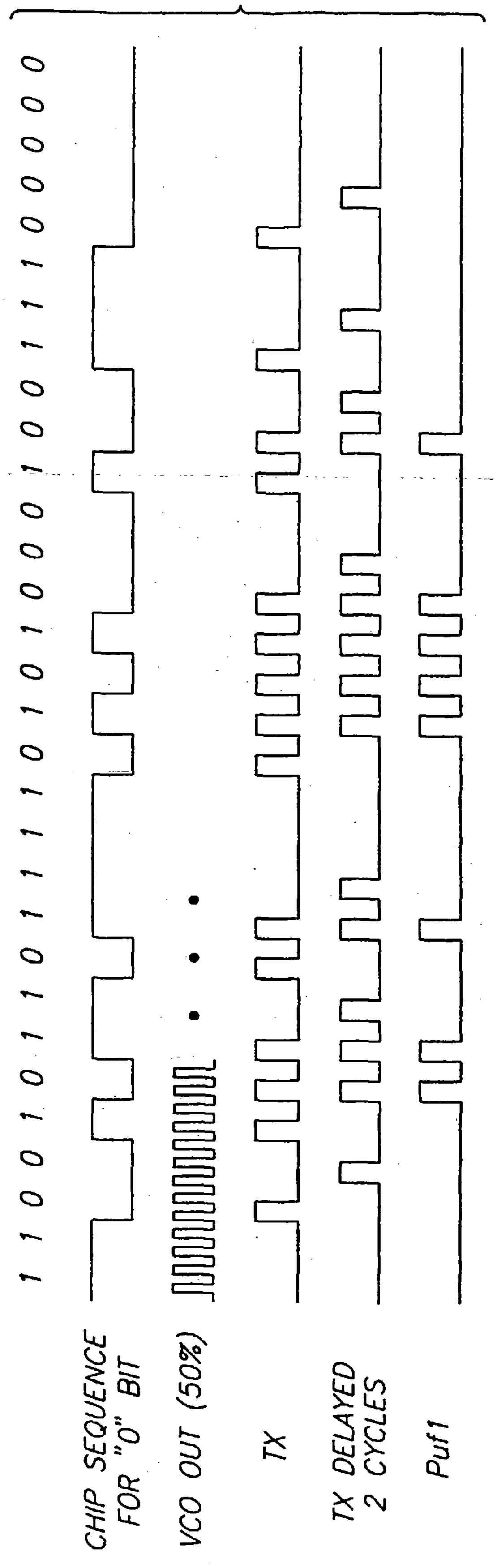

1 1 0 0 1 0 1 1 0 1 1 1 1 1 0 1 0 1 0 1 0 1 0 0 0 1 0 0 1 1 1 0 0 0 0 0
CHIP SEQUENCE FOR "0" BIT
VCO OUT (50%)
TX
TX DELAYED 2 CYCLES
Puf1

Fig. 67

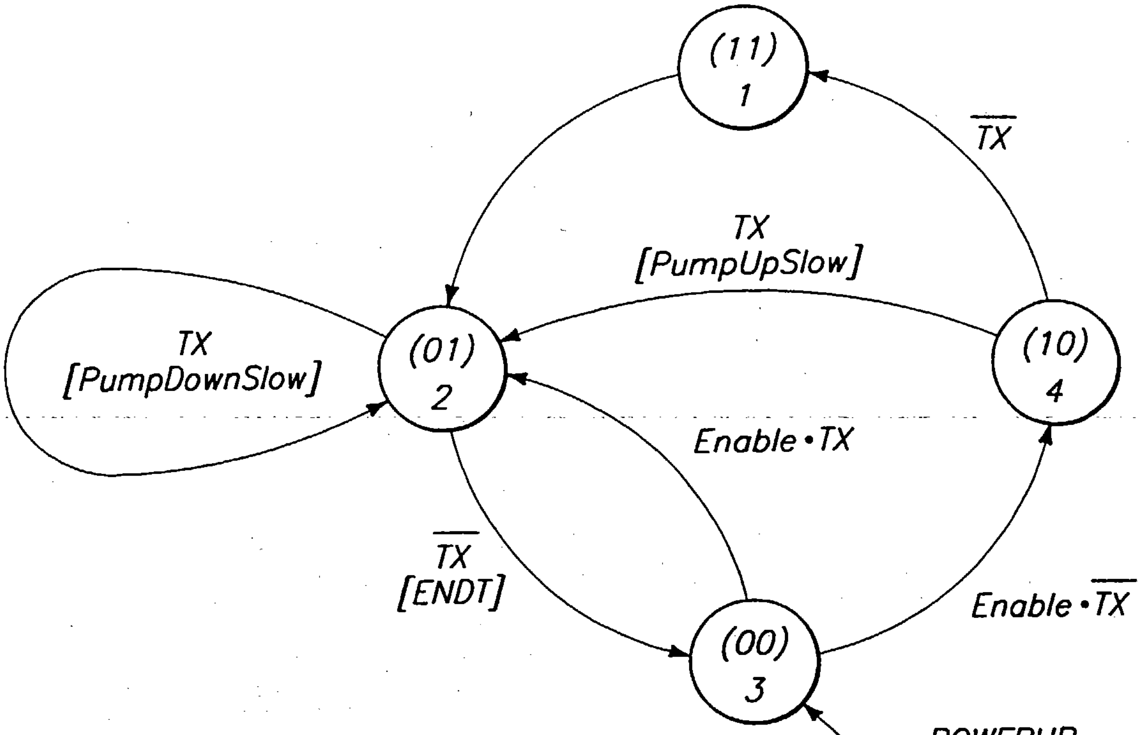

(11)
1
$\overline{TX}$
TX
[PumpUpSlow]
TX
[PumpDownSlow]
(01)
2
(10)
4
Enable • TX
$\overline{TX}$
[ENDT]
Enable • $\overline{TX}$
(00)
3
POWERUP

Fig 64

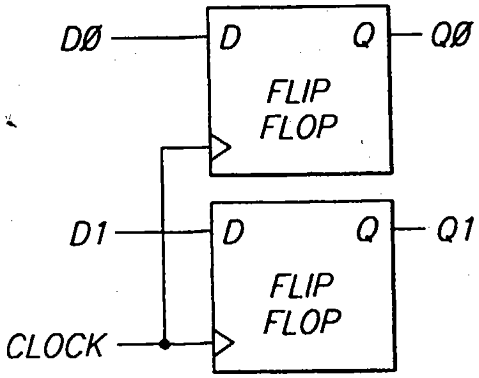
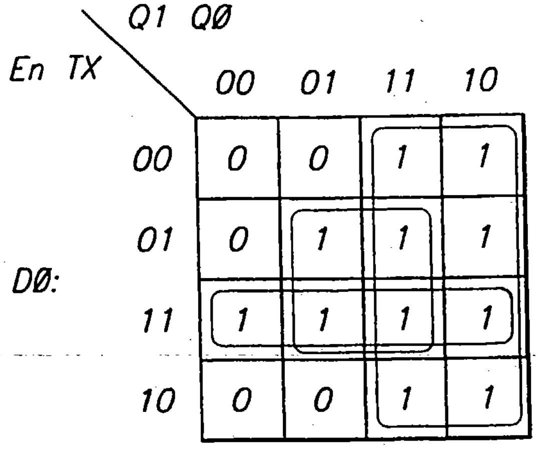

D0
D
Q
Q0
FLIP
FLOP
D1
D
Q
Q1
FLIP
FLOP
CLOCK

Fig 65

		PRESENT STATE		NEXT STATE	
ENABLE	TX	Q1	Q0	D1	D0
0	0	0	0	0	0
0	1	0	0	0	0
1	0	0	0	1	0
1	1	0	0	0	1
X	0	0	1	0	0
X	1	0	1	0	1
X	X	1	1	0	1
X	0	1	0	1	1
X	1	1	0	0	1

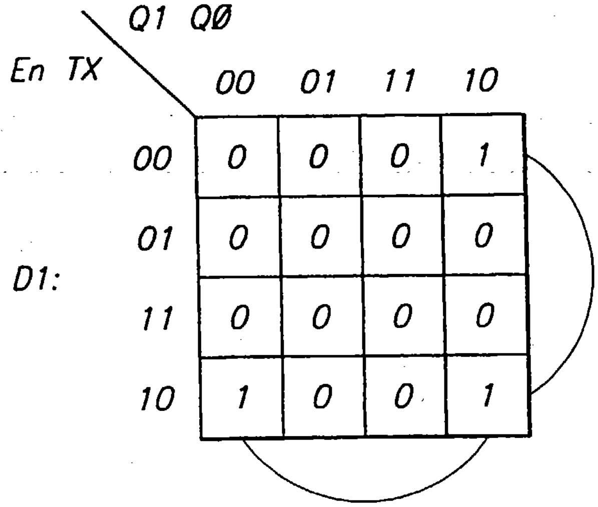
Fig 66



D0:

En TX \ Q1 Q0	00	01	11	10
00	0	0	1	1
01	0	1	1	1
11	1	1	1	1
10	0	0	1	1

Fig 67



D1:

En TX \ Q1 Q0	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	0	0	0	0
10	1	0	0	1

Fig 68

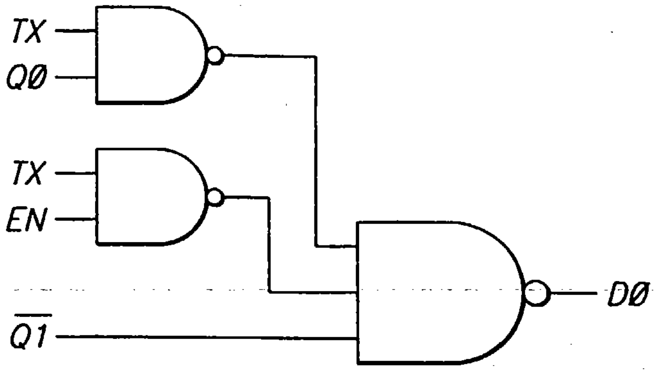

TX
Q0
TX
EN
$\overline{Q1}$
D0

Fig 69

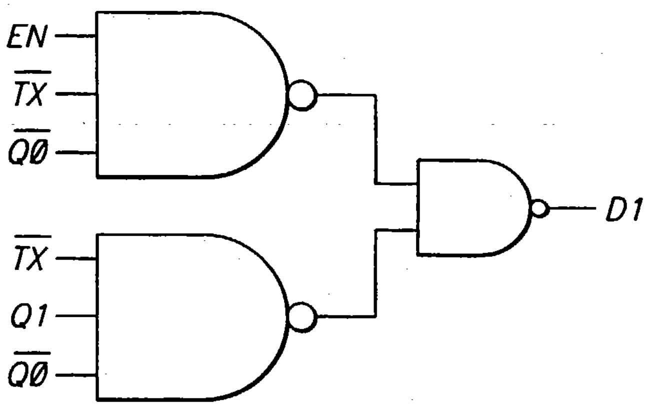

EN
$\overline{TX}$
$\overline{Q0}$
$\overline{TX}$
Q1
$\overline{Q0}$
D1

Fig 70

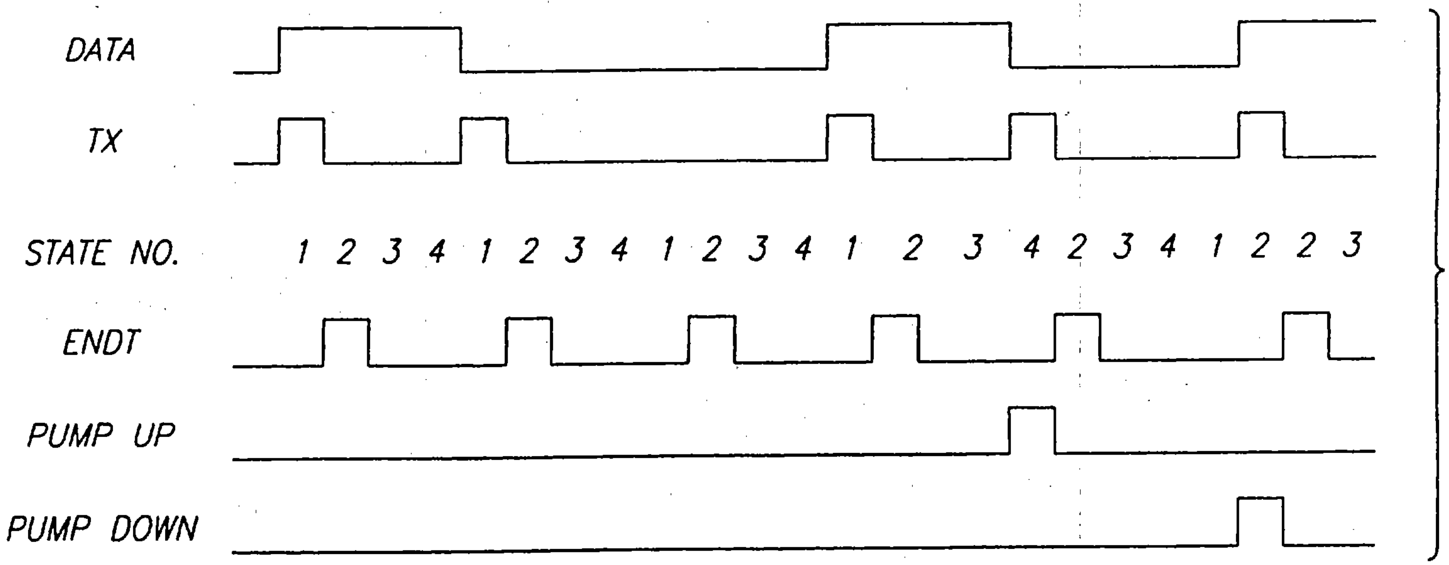

DATA
TX
STATE NO.
1 2 3 4 1 2 3 4 1 2 3 4 1 2 3 4 2 3 4 1 2 2 3
ENDT
PUMP UP
PUMP DOWN

FIG. 21

NAME	CURRENT (μA)	ΔV (mV)	$^{\Delta V}/_{V}$ CONTROL(NOM) X 100
COARSE	40	160	13.3%
MEDIUM	10	40	3.3
MEDIUM FINE	1	2.6	0.22
FINE	0.1	0.26	0.022

Fig 12